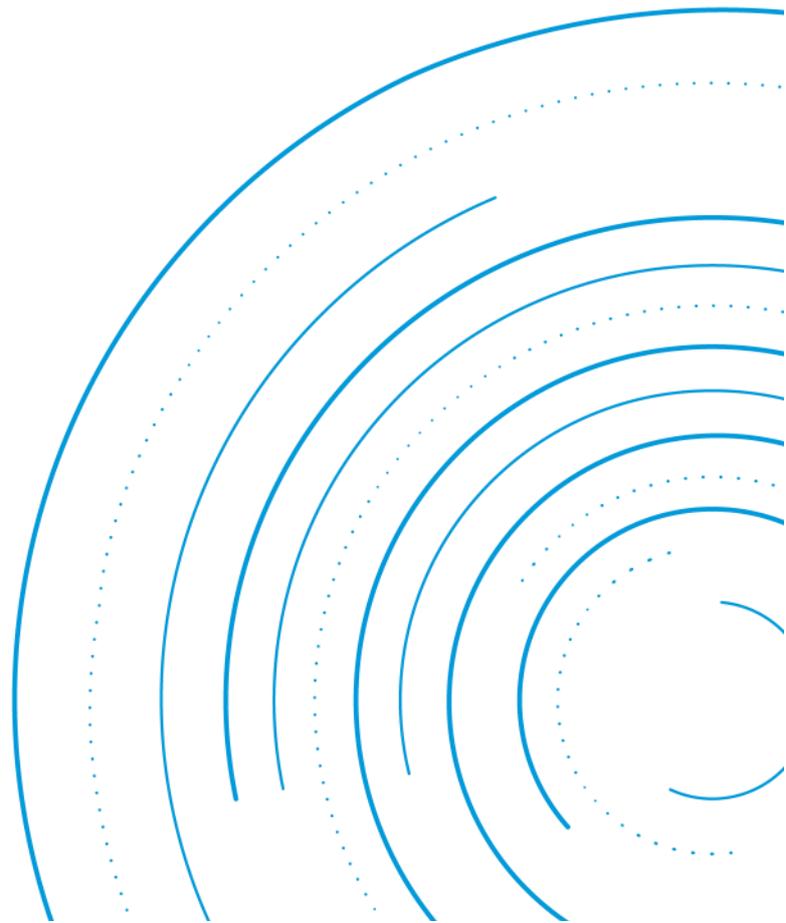


APPLICATION NOTE 307

Paralleling operation with load sharing for digital Point of Load converters



Abstract

The digital products can be configured, controlled and monitored through a digital interface using the PMBus™ power management protocol.

This application note provides information on how to parallel two or more digital PoL regulators.

The most common reason for paralleling board mounted power supplies is either to increase the power output capability above the rating of a single product or to provide redundancy so that a single product failure will not affect the system operation.

Other reasons for using products in parallel include distribution of thermal heat load over a larger board area and reducing the number of different product types used in a system design by implementing higher power requirements using products with lower output power in parallel.

A current sharing group is two or more phases/modules operating in parallel at the same frequency by sharing a synchronized clock, and their outputs are interconnected together, switching phases were interleaved to multiply the ripple frequency by the number of paralleled devices. Paralleling modules in this manner has the added benefits of reducing the input filter stress, distributing the converter thermal load, reducing volume and weight and many other advantages.

This application note applies to the following products:

BMR 463

BMR 464

BMR 465 (dual phase)

BMR 466

BMR 467 (dual phase)

BMR 469 (dual phase)

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Paralleling features & philosophy

Operation of modules in parallel requires reconfiguration using the PMBus (see Note 1 below). During parallel operation of the modules, the PMBus is not used for current sharing related communication, but only for other control functions or monitoring.

Note 1: [BMR469](#) has 2 phases in a module, it can be pin strap configured as 2 phases in parallel. It is referred as 'single output mode' in the datasheet.

2* BMR469 modules can be pin strap configured as 4 phases in parallel.

3* BMR469 can be configured as 6 phases in parallel by PMBUS. It does not support pin strap setting.

4* BMR469 can be configured as 8 phases in parallel by PMBUS. It does not support pin strap setting.

Main and secondary over the GCB bus

Introducing the GCB (Global Communication Bus)

Some Flex Power Modules' products have a dedicated single wire serial bus (GCB bus) to synchronize and communicate real-time events. This is an internal bus which is only connected across modules and not to the PMBus system host. GCB addresses are assigned on a rail level, i.e. modules within the same current sharing group share the same GCB address. Addressing rails across the GCB is done with a 5 bit GCB ID, yielding a theoretical total of 32 rails that can be shared with a single GCB bus. Ensure that the GCB signal integrity is maintained when using a large product count, see rise time formula in the product's Technical Specification.

During GCB events, all modules will receive messages; however, only those modules configured to respond will do so. GCB products can also transmit events if their programmed algorithm requires inter product communication. Some examples include current sharing, fault spreading, sequencing, broadcast margin and broadcast enable. Multiple current sharing groups and power rails can communicate over the same GCB bus.

Pull up of the GCB signal

As a BUS, the GCB signal only need a pull up resistor to the pull up voltage. To make products easier to use, some products are designed with internal pull up resistors and with internal pull up voltage source. For those products, customers can directly connect the GCB signal to the BUS, without using external pull up circuitry.

No internal pull up	BMR463, BMR464, BMR466
Built-in pull up	BMR465, BMR467, BMR469

Main and secondary

At a high level, current sharing is a group of modules with their outputs tied together to form a single rail. The modules, acting as shared phases, require one device to act as a main to continuously broadcast its output current to the other secondary devices over the GCB bus.

The main device is the module with assigned position 1, whereas the secondary devices are assigned positions 2, 3, 4... etc. When a secondary device receives the output current from the main, it trims its output voltage up or down until all devices in the group supply the same current to the load.

Each device in a current sharing group must be of the same product model. See each product's Technical Specification for the maximum number of modules in a current sharing group.

Active droop current sharing

Current sharing with digital power has its unique advantages, but to understand this it is worth revisiting the fundamentals of current sharing and droop.

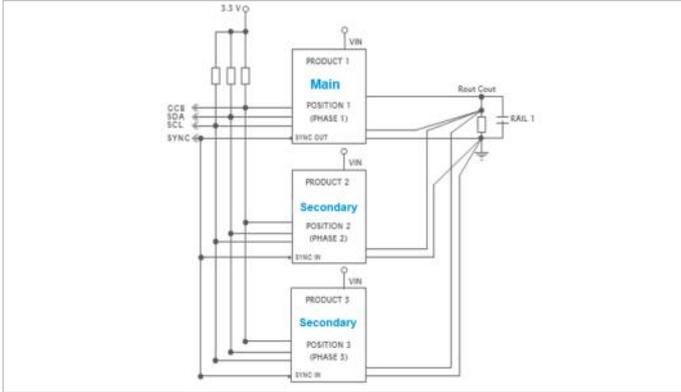


Figure 1. A three-phase current sharing group. The GCB line is common across all phases, and the common Sync clock is generated by the main phase.

Understanding droop

In most load-sharing applications, the voltages across phases would operate at exactly the same voltage at all times. In practice though, manufacturing variations and the board design can lead to small differences in the actual output voltage. These small differences, when applied to regulators operating in parallel, creates current loss where a regulator with a higher voltage is supplying current to the other regulator(s).

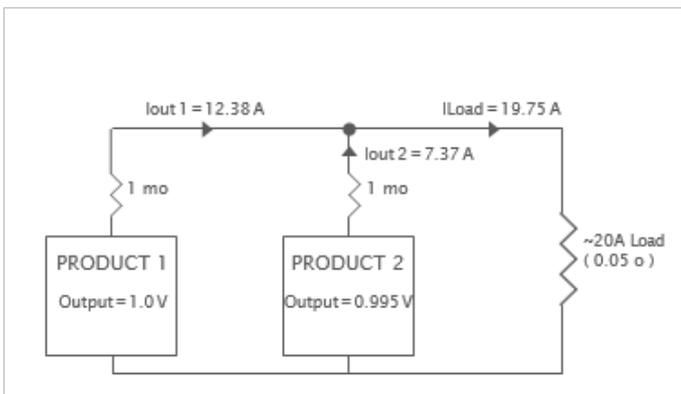


Figure 2: One scenario of current imbalance due to voltage differences

Figure 2 shows a simple example where one voltage source has a slightly different voltage by 5 mV, which causes a current imbalance of over 4 Amps.

Even if the regulators themselves are outputting the same voltage, there could be component variations between the regulator and the load that create variations of the 'loadline resistance', which also create a current imbalance. This can be due to the board layout, current-sense resistor differences, etc.

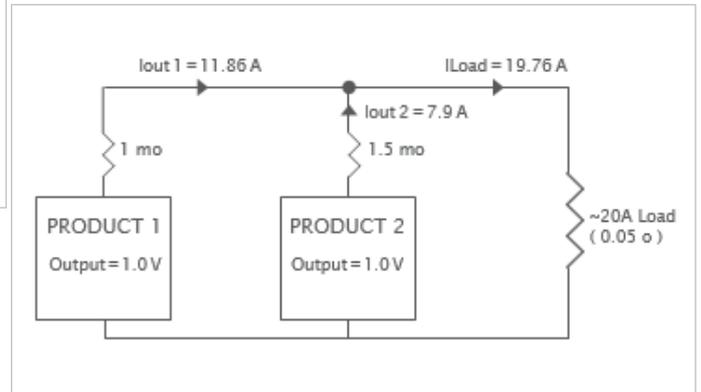


Figure 3: Another scenario where loadline imbalances can also cause current imbalance

Figure 3 shows another simple example where a small difference in the loadline creates a current imbalance of nearly 4 Amps.

Across a range of loads, these imbalances change and can be visualized by plotting the individual loadlines (or droop) of each phase.

This effect is shown in [Figure 5](#). Notice in this case the main initially sourced the majority of the load current. Each secondary's reference voltage was trimmed in the positive direction until all phases source equal current to the load.

The modules can sense their output voltage and output current while communicating with each other over the GCB bus, thus they can dynamically trim the output to reduce current imbalances, leading us to "Active Droop Current Sharing".

Current sharing algorithm

A specific droop is set based on the application. The droop is set to the same value for each device in the group. Figure 4 shows an example where each device's droop, was set to 1 mV/A.

Note that the graphs and the x-axis represent the individual loadline of each device. Due to differences in layout and component variances the actual loadlines contain slope differences and lead to a current imbalance; they are exaggerated in this example

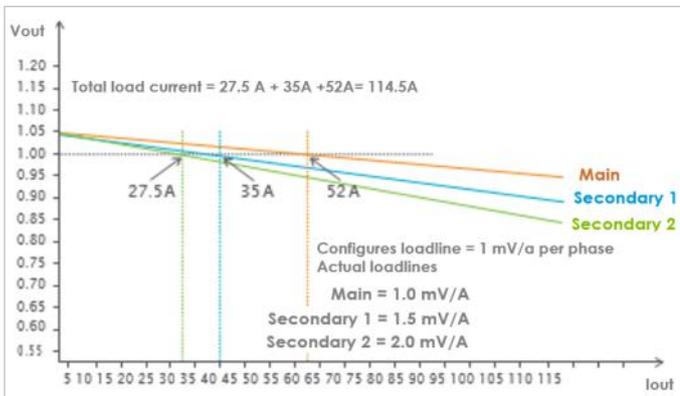


Figure 4: Unbalanced phase currents due to slope error

The minor imbalance results in each phase contributing an unequal portion of the load current. With Active Droop Current Sharing, the imbalance is detected as the main's load current is broadcast and each secondary's reference voltage is trimmed up or down until all products in the group carry an equal portion of the load current:

$$V_{Member} = V_{OUT} + Droop_{Phase} \times (I_{Reference} - I_{Member})$$

This effect is shown in Figure 5. Notice in this case the main initially sourced the majority of the load current. Each secondary's reference voltage was trimmed in the positive direction until all phases source equal current to the load.

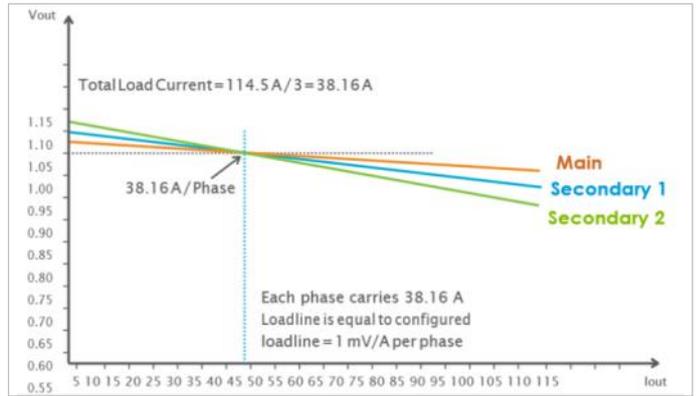


Figure 5: Balanced phase currents. Secondary reference voltage(s) is trimmed until all products' currents equalize.

Current sharing equilibrium is shown in Figure 6 with a singular loadline being plotted that represents the actual static response for the sharing group. This loadline is maintained even when phases are added or dropped.

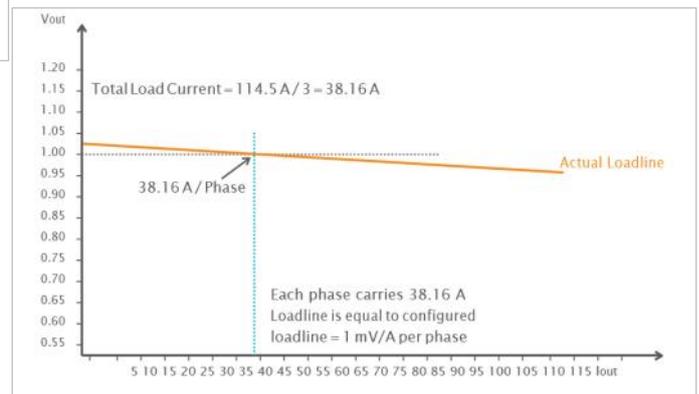


Figure 6: Current sharing phase balance is achieved

Current balance accuracy

The actual current supplied by each module in a sharing group in steady state will not always be equal due to the current monitoring accuracy. The current monitoring accuracy (see Technical Specification for each product) in turn will depend on the trimming of each device in production as well as varying with operating conditions such as input voltage, output voltage and temperature.

Product used Smart Power Stage rather than MOSFET, will have better current sensing accuracy, for example [BMR465](#) and [BMR469](#).

The products have been designed to operate beyond rated output current in order to support 100% of rated output current from each device in a sharing group (e.g. three 40 A devices in parallel support 120 A output current). However, the current monitoring accuracy should be taken into account when considering the thermal operating conditions of a current sharing group.

Automatic phase distribution

Common SYNC clock

As mentioned earlier, a current sharing group requires a common SYNC clock across all phases, as shown in [Figure 1](#). This SYNC clock can be provided internally by one of the devices in the group (typically the main device but can also be one of the secondary devices) or by an external source. For some products the SYNC output can be configured as open-drain as an option (otherwise push-pull). All other devices connected to the SYNC source must be configured as SYNC inputs. If using an external source, the switching frequency of each device must be configured to the same nominal value as the external source.

Phase distribution

A current sharing group's phases are autonomously distributed evenly over a maximum phase offset of 360°. By default the phase offset of the main is 0°. For example, if we evenly distribute the phase offsets of a 3-phase current sharing group (shown in [Figure 1](#)), the offset of the phases

will ideally be 0°, 120° and 240°.

The actual phase offset is represented by a 4 bit binary number, which provides 16 possible offset values in 22.5° steps. The real phase displacement will be rounded to the closest 22.5° increment. The actual offsets for the 3-phase rail are in Table 1, and all possible phase displacements are shown in Figure 7.

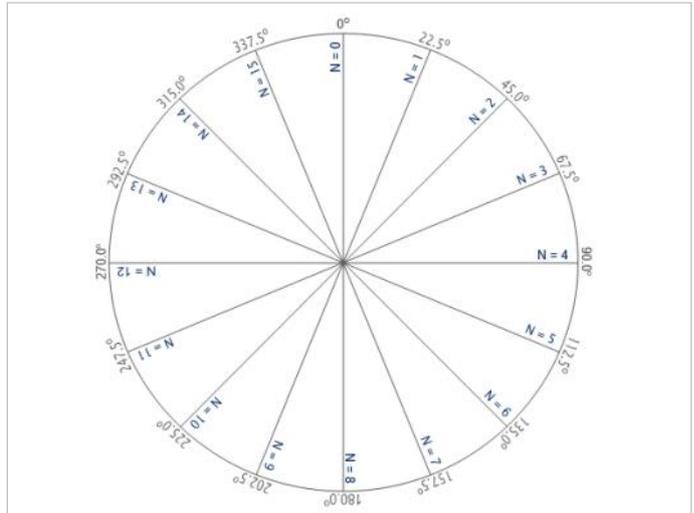


Figure 7: Phase offset resolution wheel

In cases where a parallel rail shares the SYNC clock with other rails (single or parallel), one may want to customize the default phase offsets by using the INTERLEAVE command. [Flex Power Designer](#) makes phase spreading easy to customize and visualize. See [Application Note 309](#) for more details.

	Ideal offset	Actual offset
Position 1	0°	0°
Position 2	120°	112.5°
Position 3	240°	247.5°

Table 1: Ideal vs actual phase offset

Turn-on and turn-off

Turn-on and turn-off of a current sharing group can be controlled in two ways.

- 1) CTRL pin. The CTRL pin of all devices in the current sharing group should be connected and be controlled from the same source.
- 2) PMBus enable. Sending a PMBus Enable or Margining command (OPERATION) to any of the devices in the group will enable the whole group, as the device will 'broadcast' an enable signal to the other devices over the GCB bus as shown in Figure 8.

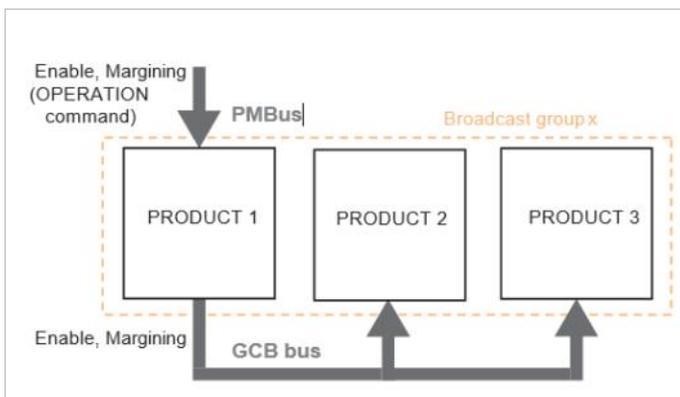


Figure 8. Enable or margining signal will broadcast on the GCB bus

For PMBus enable and margining, the devices must be set to Broadcast Enable and Margining (registers MISC_CONFIG/GCB_CONFIG or GCB_GROUP command depending on product), which is automatically set when using the Flex Power Designer software.

Ramp synchronization

During turn-on and turn-off the voltage ramps of each phase are synchronized to start at the same time. This ensures that inter-phase circulating currents are minimized. Each module contains a separate digital controller that executes firmware. The individual controller firmware requires synchronization prior to ramp events.

This is accomplished by forcing the main device to wait at least one additional firmware cycle during ramping events by configuring it to have additional TON_DELAY time and TOFF_DELAY relative to the group secondary. This additional delay is automatically set when using [Flex Power Designer](#).

Note: The BMR465/BMR467/BMR469 products do not require these additional TON/OFF_DELAY times. (The main and secondary will still be synchronized.)

When the sharing group receives a CTRL pin or PMBus enable, the secondary initialize their registers but wait for the main to send a message before enabling. Once the main phase completes it transmits a GCB Ramp Flag and all products of the group produce a sequenced PWM and begin their soft-start. Timing diagram shown in Figure 9.

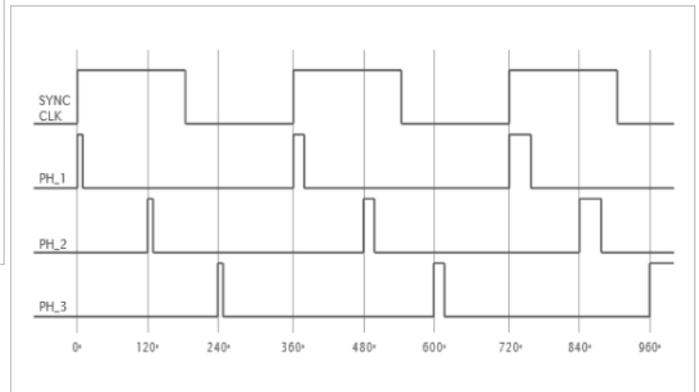


Figure 9. Start-up synchronization of 3 phases

Minimum duty cycle

Each module contains its own controller. To ensure that each controller produces an identical pulse width at turn-on the products must be configured for minimum duty cycle (register USER_CONFIG). This starts each device in the group with the same initial pulse width.

The actual configured rise time is conserved as shown in Figure 10.

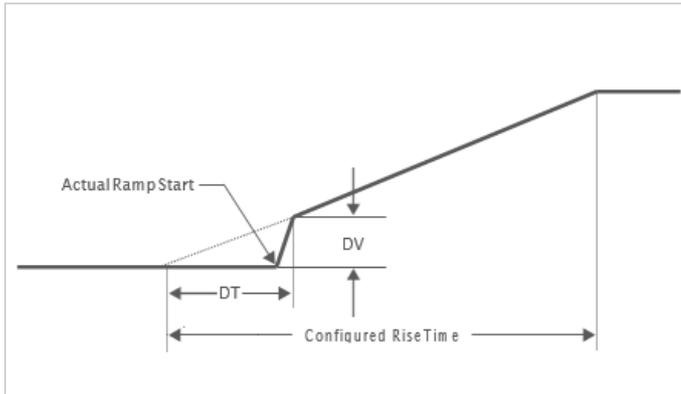


Figure 10: Turn-on rise time profile

The magnitude DV in the beginning of the ramp caused by the minimum duty cycle will increase with input voltage and switch frequency. The inrush current through the inductors may in some applications cause a small distortion in the beginning of the ramp as shown in Figure 11.

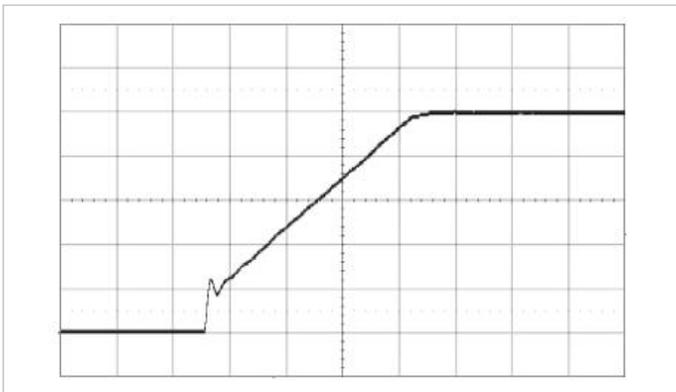


Figure 11: Effect of minimum duty cycle at ramp-up

Ramp behavior

The products use a unique ramping algorithm in current sharing configuration that results in near perfect current sharing while ramping. This is accomplished by deriving different control loop settings for ramping than those used for steady-state operation. The settings for ramps are not user configurable. The ramp control loop settings are derived from the configured rise/fall time, input voltage, output voltage and switching frequency. During ramp the loop bandwidth is intentionally set to a very low value so response to transients will be limited. The user should limit dynamic loading while ramping.

The devices will switch to the configured control loop settings at the moment when the PG (power good) signal is asserted. The user has control over the switchover by configuring the PG delay. While

ramping down, the switchover takes place just before the TOFF delay timer starts.

For BMR 463/464/466 products variants which have DLC (Dynamic Loop Compensation) measurement after ramp-up completed, the resulting compensation solution will be transmitted over the GCB bus so that each product in the group has the same compensation settings.

Ramp time accuracy

The unique ramping algorithm used in current sharing restricts the rise and fall times to a maximum value. The low bandwidth ramp technique also limits the resolution of the rise and fall times. The maximum limit and the resolution will depend on the configured switch frequency, input voltage and output voltage.

When using the [Flex Power Designer](#), the rise and fall time maximum limits are automatically handled and the resolution is calculated. Figure 12 shows how the actual ramp time due to the limited resolution is displayed, based on the desired set value entered by the user.



Figure 12: Soft on/off configuration of a parallel rail in Flex Power Designer

Fault handling

Faults and main/secondary (BMR463/464/466)

If one or more devices in a current sharing group fault, the remaining devices will continue to operate, and the device with the next lowest position becomes the new main. Automatically adding back faulted devices into the group, i.e. restarting of individual devices in the group due to a fault, is not supported. If the devices in the group have one or more fault responses configured for restart (which is the default setting), a synchronized restart of the whole group will occur only after all devices have shut down due to faults.

If the main device faults and shuts down, a time of approximately 30 ms must pass after PG de-assertion of the failed main devices, before the remaining devices can be disabled. If the remaining devices are disabled too quickly, they would stay active despite enable signal set to disable (if they can support the current). This is due to a secondary device being in a wait state when transitioning from being a secondary device to becoming the new main device.

Faults and main/secondary (BMR465/BMR467/BMR469)

If one or more devices in a current sharing group get a fault, all the devices in the group will shut down automatically through GCB communication. A common connection of the FAULT pin of all devices in the group ensures a fast shutdown of each device's power stage, overcoming the latency related to the GCB communication.

Note that automatic restart after fault ("hiccup" mode) is not supported for BMR465/BMR467/BMR469 current sharing groups. The fault response will be immediate and definite shutdown regardless of the response settings used.

Faults and SYNC clock

A device (either current sharing main or secondary) that is configured to source the SYNC clock will continue to supply the clock if it faults, even though its output has become inactive.

Phase add/drop (BMR 463/464/466 only)

When devices are configured in a current sharing group, individual phases are capable of (dynamically) dropping out and adding back to the group. Phases are typically dropped or added to improve efficiency or to process a fault. Phases can be added or dropped on the fly using a separate power management host controller by invoking the PHASE_CONTROL command (and setting Phase Control Select in the MISC_CONFIG command to use the PHASE_CONTROL command).

Even though a dropped device stops switching the operation status of the device will be Enabled and the duty cycle read (command READ_DUTY_CYCLE) will be unchanged.

Phase drop

If the dropped device was the group main a new main will be reassigned based on the lowest sharing group position number of the existing operational devices. If the dropped device was supplying the SYNC clock it will continue to do so. The angular offset relative to the SYNC clock is defined by the group position and will autonomously redistribute based on the standing phases.

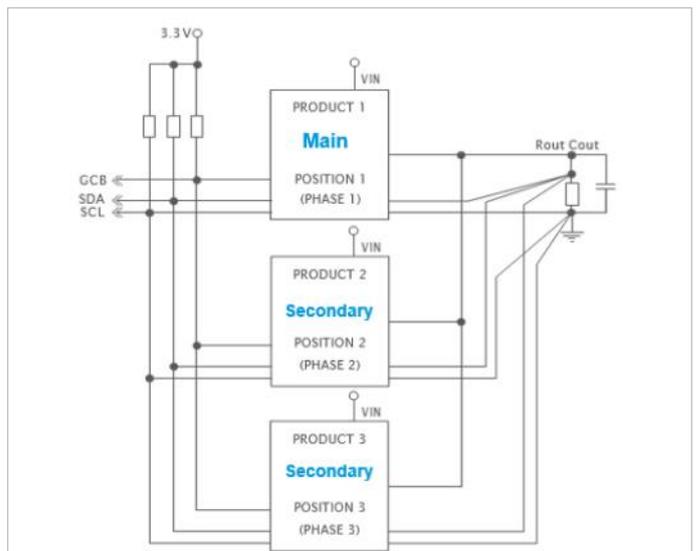


Figure 13: 3 phase converter showing main, secondary and position number

Figure 13 shows an example of a functional 3-phase current sharing group prior to the dropping of the main (Product 1). Figure 14 illustrates the new 2-phase configuration after the main phase is dropped. Product 2 becomes the new main for current sharing. Product 1 supplying the SYNC clock continues to do so. The timing diagram is shown in Figure 15.

After the main phase is dropped the remaining two phases are redistributed and the phase displacement changes from 120° to 180°.

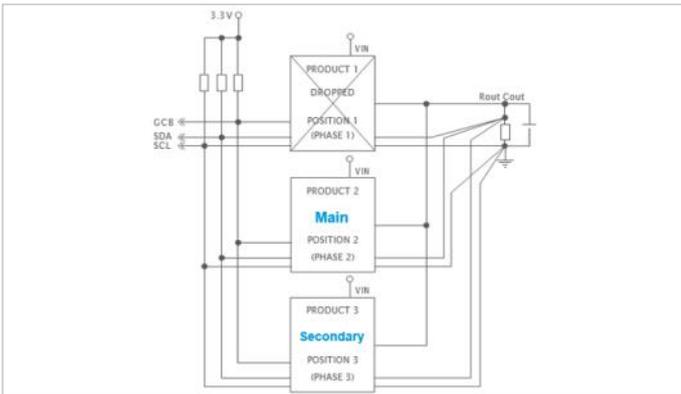


Figure 14: 3-phase converter after main phase is dropped

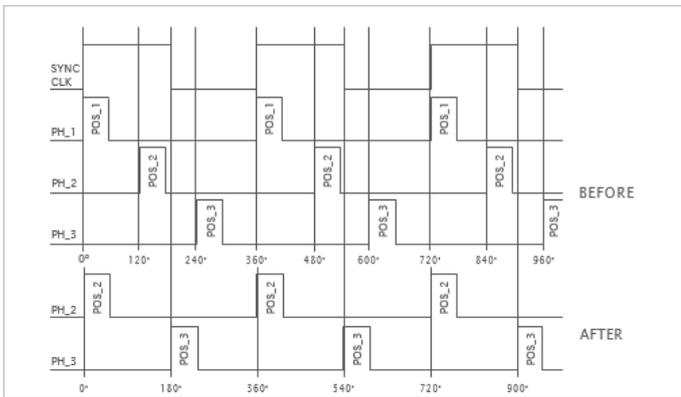


Figure 15: 3-phase converter after main phase is dropped

Phase add

The phase that was previously dropped may be added back into the group as determined by the power management host. When the adding is performed, the event is coordinated with the active group products over the GCB bus and the previously inactive product is added back into the group. In this example, Product 1 (from figure 13) was made active and resumed the role of being

main. The phase offset of each group product was automatically redistributed from 180° to 120° - essentially the reverse action of Figure 14.

Dropped phase and SYNC clock

If the dropped device was supplying the SYNC clock it will continue to do so even though it has become inactive. If the device supplying the SYNC clock dropped from the group and is no longer capable of supplying the clock, the remaining members will detect the absence of SYNC and respond according to their fault spreading configuration. If a host or power system manager is monitoring SALERT, the PMBus can be read and the devices will respond with the appropriate fault management alarm as described in the PMBus Power System Mgt Protocol Specification – Part II.

Output voltage at phase add/drop

When adding or dropping a phase there will be a small deviation to the output voltage due to the droop change. Since the effective droop value for the whole group is maintained the individual droop of each phase must change. For example in a sharing group of four phases and an effective droop of 0.25 mΩ, each phase has an individual droop of 1 mΩ. When dropping one of the phases the individual droop of the still active products is maintained at 1 mΩ for a short period of time, resulting in an actual effective droop of 0.33 mΩ. Figure 16 shows the example when the output current is 100 A, giving a deviation of 8 mV. When adding a phase back to the group there will be a deviation due to the same reason but in that case the output voltage will increase instead of decrease. In any case, the deviation will always be within the voltage drop range defined by the configured total droop.

Note: The output voltage is also affected by the load step that occurs for active devices during a phase add or drop.

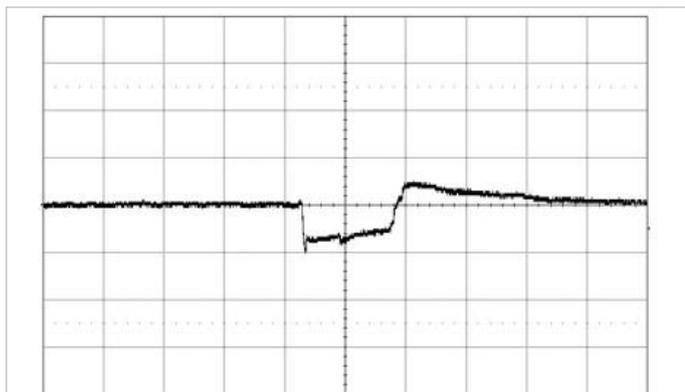


Figure 16: Example of output voltage deviation during drop (10mV/div, 10 ms/div)

Voltage tracking (BMR463/464/466 only)

For current sharing groups voltage tracking is emulated by configuring the output ramp to match the ramp of the VTRK voltage. Doing this affects how the rise/fall times should be set along with the power-up delay times. [See application note AN310](#) for more details.

Note: Voltage tracking with a pre-bias voltage at the output is not recommended since there is risk of phase currents to drift apart.

Note: Voltage tracking is not supported for BMR465/ BMR467 devices in parallel operation.

Adaptive deadtime (BMR463/464/466 only)

The controllers of the products utilize a closed loop algorithm to optimize the dead-time applied between the drive signals for the power stage. In parallel operation several other algorithms are also running, i.e. local droop, rail droop, voltage regulation, and current balance algorithms. In order to avoid the possibility of these algorithms interfering with each other, the adaptive deadtime algorithm must be disabled while current sharing, i.e. fixed deadtimes must be used.

NLR threshold scaling (BMR463/464/466 only)

When multiple devices are configured in a current sharing group, the effective output ripple is (ideally) divided by the number of active group devices. This means when all devices in the group are operating, the NLR (Non Linear Response) thresholds can be set to a smaller value just above the ripple amplitude. When a phase is dropped the ripple amplitude will increase.

In order to avoid spurious NLR activity the devices automatically adjust the NLR thresholds according to the ratio of active phases to total phases of the group:

$$Threshold_{Drop} = Threshold_{Config} \times \frac{N_{All}}{N_{Active}}$$

where $Threshold_{Drop}$ is the NLR inner threshold setting used when some group products are dropped.

$Threshold_{Config}$ is the NLR inner threshold setting configured for the group products.

N_{All} is the total number of phases in the sharing group. N_{Active} is the number of phases active in the group (devices not faulted or intentionally deactivated).

N_{All} and N_{Active} are determined automatically from the group configuration parameters. No additional programming or configuration is required. Since the available thresholds are quantized to multiples of 0.5% of the configured output voltage, the next higher available threshold is used if the result of the above formula is fractional.

DLC result scaling (BMR463/464/466 only)

For BMR 463/464/466 products variants which have DLC (Dynamic Loop Compensation) enabled, the result from the DLC algorithm should be scaled down based on the number of phases in the current sharing group. This is due to the output ripple levels being lower at parallel operation, which will cause the DLC algorithm to set a higher gain for the control loop.

See command `AUTO_COMP_CONFIG` in [Appendix 2](#) for suggested scale levels.

Control loop design

When doing control loop analysis for a parallel rail, for example in Flex Power Designer tool, the total (external) output capacitance of the rail shall be divided by the number of devices. Consider the 3-phase example shown in Figure 17. This schematic is drawn symmetrically with identical phase filters. The number of capacitors to be entered in the Output Filter view of [Flex Power Designer](#) for this configuration should be according to Figure 18. Thus the total capacitance of the rail is divided by three in this case.

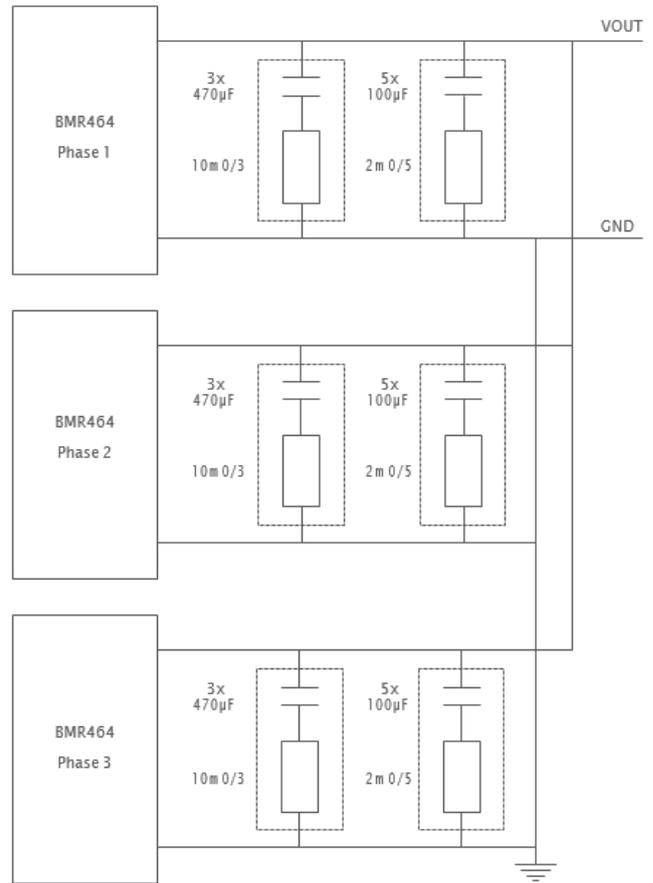


Figure 17: 3-phase current sharing example

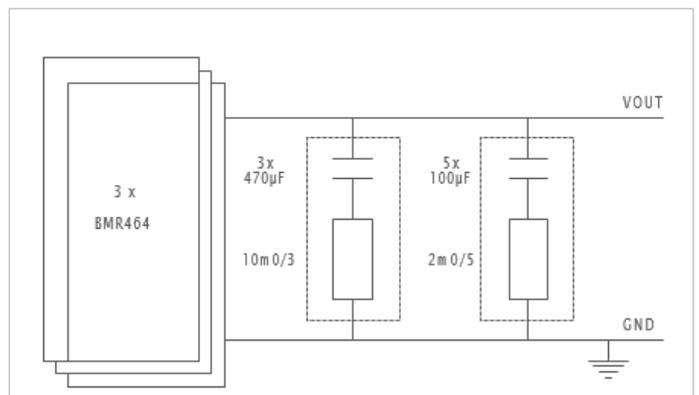


Figure 18: Output filter entered in Flex Power Designer tool for current sharing with 3 phases in figure 17

Paralleling with Flex Power Designer

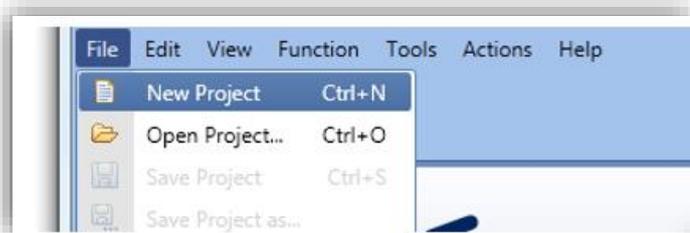
Introduction

Paralleling modules requires setting up a number of parameters. While this can be done manually by setting individual commands, it is significantly easier to use the Flex Power Designer software to quickly create parallel rails. The software is available for download at flexpowermodules.com.

Creating a parallel rail

This section walks through creating a parallel rail using the Flex Power Designer. No hardware is required, but this walkthrough project can be loaded onto two BMR 463s using the PoL paralleling test board (ROA 128 5077).

Step 1. Open the Flex Power Designer and create a new project



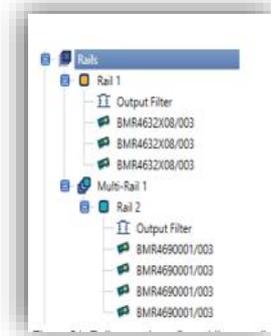
Step 2: Select rails from 'Configuration browser' and pick target product from right window or select the picture or key in the product number the



rails item in the configuration browser.

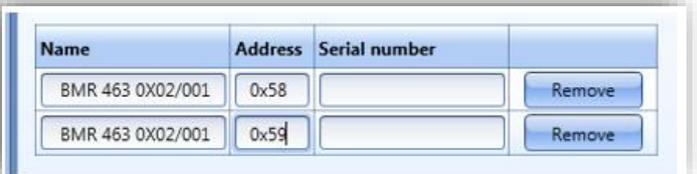
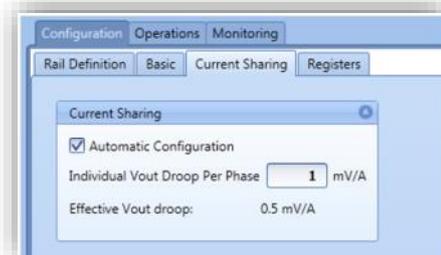
Right click, then the user will be prompted how many units will be paralleled.

If a BMR469 product is added, the rail will be list as "multi-rail". All other products will be list as normal rail



After adding the parallel devices, your rail's configuration should look as shown below.

Step 3: Now that the parallel rail is defined, we just need to configure its settings. First, while droop is usually configured automatically, you may optionally change the droop, which is automatically calculated evenly across phases and adjusted during phase add/ drop events.



Step 4. Outside of the optional droop setting, all we need to set in this example is the Rail's VSET resistor, which is 3.3V (the POL parallel board default across all phases). The setting is found on the 'Basic' configuration tab as shown in picture below. You may also configure custom voltages, timing, and fault settings here as well.

Step 5. If you are going through this walkthrough with a PoL parallel test board, you can load the project onto the devices. Setup the board as shown in picture 19 below, then power it and connect the USB-PMBus Adapter to the board.

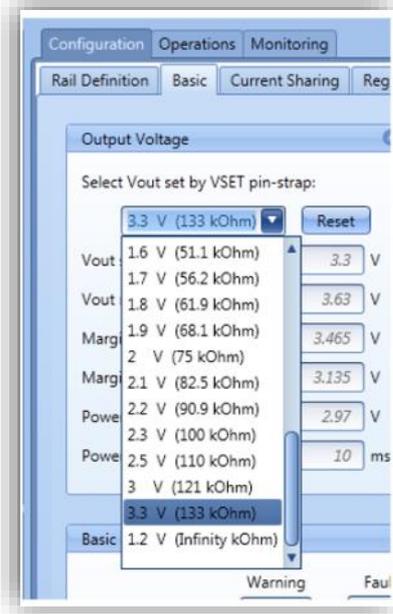


Figure 19: PoL parallel test board setup for this example—two BMR463 modules at addresses 0x58 and 0x59

After the board is powered and connected, ensure that the CTRL switch is off before loading configuration. To load the project configuration to devices, use the 'Write Project to RAM & Store to NVM' button in the toolbar.

Paralleling made simple

The previous example only took a few steps with an entirely new project. This is because the software automatically sets the commands required for parallel operation. You can see which commands have been automatically set by either going to the registers tab, or by going to the export menu and previewing the commands sent to the parallel rail.

A full explanation of the automatically set commands is provided in [Appendix I](#).

Layout considerations

The PWB layout and placement of input and output capacitances should be made as symmetrical as possible between the products in a current sharing group, as illustrated in Figure 26. This is to minimize loadline differences, improve ripple cancelation and even-up the control loop response of each phase. For the same reason VIN, VOUT and GND connections should be as low impedance as possible.

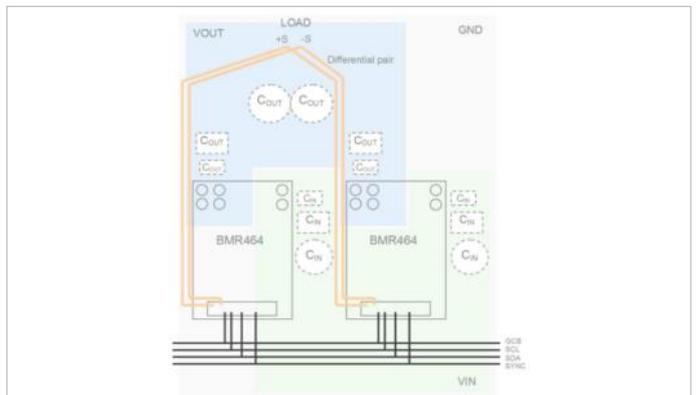


Figure 20: Layout principles, two products

Each product in a current sharing group must use the same point of output voltage remote sense. It is recommended that the traces for the voltage sense lines are routed as a differential pair in order to minimize the sensitivity to disturbances.

Appendix 1: Parallel settings automatically configured by Flex Power Designer

The [Flex Power Designer](#) software automatically does the following steps when setting up a parallel rail. These steps are done across all devices in the parallel rail unless otherwise noted.

If one is configuring modules without Flex Power Designer, these steps should serve as a checklist.

BMR463, 464 and 466

More details regarding the steps below are provided in [Appendix 2](#).

1. Enable ramp-down during disable (i.e. Set bit 0 in ON_OFF_CONFIG to 0).
2. Disable crowbar from occurring during an OV FAULT (i.e. Set bit 7 in OVUV_CONFIG to 0).
3. Enable Alternate Ramp Control (i.e. Set bit 2 in MFR_CONFIG to 1).
4. Enable a Minimum Duty Cycle of FSW/256 (i.e. In USER_CONFIG, set bit 13 to 1, and set bits 15:14 to 00).
5. Designate and configure SYNC source for the group. By default, the software configures the main phase to output SYNC, and secondary phases to be SYNC inputs (affects MFR_CONFIG bit 0, USER_CONFIG bits 6:5).
6. Disable Precise Ramp Up Delay (if applicable to the product model used, i.e. set bit 7 MISC_CONFIG to 1).
7. In ISHARE_CONFIG,
 - Assign the same "group number" setting.Enumerate the member position across phases, the main phase will be set to Member Position 1.
 - Assign the same "number of devices" setting.
8. Ensure that the TON_DELAY and TOFF_DELAY times for the main are at least 10 ms greater than the corresponding delay parameters of each secondary, with a minimum required delay of 15ms. Delay parameters must be greater than 5 ms. Delay parameters should be the same value across all secondary phases. If using tracking, please see [AN310](#) for more information on how TON_DELAY and TOFF_DELAY should be set.
9. Set Broadcast Enable and Broadcast Margin to both be enabled (i.e. Set bits 15 & 14 in MISC_CONFIG to 1).
10. Ensure that the GCB_ID (set in GCB_CONFIG) and IShare GCB ID (set in ISHARE_CONFIG) is set to the same value across all devices.
11. Set INTERLEAVE to all 0's. In cases where custom phase-spreading is needed, this value should be changed as described in AN309.
12. Disable adaptive deadtime algorithm and set a fixed deadtime (DEADTIME, DEADTIME_CONFIG).
13. If it is a current sharing rail, scale down DLC result in AUTO_COMP_CONFIG according to Appendix 2.
14. Ensure that the following values are the same across all phases. The software ensures these values are the same by restricting the user from changing values on individual phases.
 - Ramp Timing (TON_RISE & TOFF_FALL).
 - Fault Thresholds and Responses.
 - Droop/Loadline resistance settings (VOUT_DROOP).
 - Compensation-related parameters (PID_TAPS, NLR_CONFIG, AUTO_COMP_CONFIG).
 - Broadcast Group (GCB_CONFIG).
 - INTERLEAVE.
 - Switching Frequency (FREQUENCY_SWITCH).

BMR465 and BMR467

1. For each device, disable ramp-down during disable (`ON_OFF_CONFIG[0] = 1`).
2. For each device, ensure output OV fault crowbar function is disabled (`OVUV_CONFIG[7] = 0`).
3. Designate and configure SYNC source for the group. By default, the software configures the main product to output SYNC (`MFR_USER_CONFIG[2:1] = 01`) and secondary products to be SYNC inputs (`MFR_USER_CONFIG[2:1] = 10`).
4. In `GCB_CONFIG`:
 - For each device, ensure that the GCB ID by `GCB_CONFIG[12:8]` is set to the same value.
 - Enumerate the phase ID across products according to `GCB_CONFIG[15:13] = Position - 1`. The main's position shall be equal to 1 (hence for the main `GCB_CONFIG[15:13] = 1 - 1 = 0`). The Position of the secondary devices shall be 2, 3, .. and so on.
 - For each device, assign the total number of phases according to `GCB_CONFIG[3:0] = (2 x number of devices) - 1`.
5. For each device, enable broadcast OPERATION function by `GCB_GROUP[13] = 1`. Also ensure that broadcast OPERATION Group ID by `GCB_GROUP[12:8]` is set to the same value across all devices in the current sharing group.
6. For each device, enable broadcast `VOUT_COMMAND` function by `GCB_GROUP[21] = 1`. Also ensure that broadcast `VOUT_COMMAND` Group ID by `GCB_GROUP[20:16]` is set to the same value across all devices in the current sharing group.
7. For each device, set INTERLEAVE to all 0's. In cases where custom phase-spreading is needed, this value should be changed as described in AN309.
8. For each device, set all fault response commands to 0x80, i.e. function "disable, no retry". This change is not required, but recommended in order to have command values that reflects the actual functionality.
9. Ensure that the following values are the same across all devices. (The [Flex Power Designer](#) ensures these values are the same by restricting the user from changing values on individual devices):
 - Delay times (`TON_DELAY`, `TOFF_DELAY`)
 - Ramp times (`TON_RISE`, `TOFF_FALL`)
 - Fault thresholds and responses
 - Droop/Loadline resistance settings (`VOUT_DROOP`)
 - Control loop parameters (`ASCR_CONFIG`)
 - Switching Frequency (`FREQUENCY_SWITCH`)

Because in parallel operation the response function "disable, no retry" will always be used, regardless of the settings of the response commands.

BMR469

1. For each device (and each PAGE) , disable ramp-down during disable (ON_OFF_CONFIG [0] = 1).
2. For each device, ensure output OV fault crowbar function is disabled (OVUV_CONFIG [7] = 0).
3. Designate and configure SYNC source for the group. By default, the software configures the 1st product as main output SYNC (USER_GLOBAL_CONFIG[2:1] = 01) and rest products to be SYNC inputs (USER_GLOBAL_CONFIG[2:1] = 10).
4. In GCB_CONFIG:
 - For each device, ensure that the GCB ID by GCB_CONFIG[12:8] is set to the same value.
 - Enumerate the phase ID across products according to GCB_CONFIG[15:13] = phase / 45o And always put 180o between the 2 phases of same module.
 - For each device, assign the total number of phases according to GCB_CONFIG[2:0] = (2 x number of devices) - 1.
5. For each device, enable broadcast OPERATION function by GCB_GROUP[13] = 1, enable broadcast VOUT_COMMAND by GCB_GROUP[21] = 1, and enable fault spreading function by GCB_GROUP[5] = 1. Also ensure that broadcast OPERATION Group ID by GCB_GROUP[12:8], fault spreading Group ID by GCB_GROUP[4:0], and broadcast VOUT_COMMAND Group ID by GCB_GROUP[20:16] ID is set to the same value across all devices in the current sharing group.
6. For each device, set INTERLEAVE to all 0's. In cases where custom phase-spreading is needed, this value should be changed as described in [AN309](#).
7. For each device, set all fault response commands (except UT_FAULT) to 0x80, i.e. function "disable, no retry". This change is not required, but recommended in order to have command values that reflects the actual functionality. Because in parallel operation the response function "disable, no retry" will always be used, regardless of the settings of the response commands.
8. Ensure that the following values are the same across all devices. (The Flex Power Designer ensures these values are the same by restricting the user from changing values on individual devices):
 - Delay times (TON_DELAY, TOFF_DELAY)
 - Ramp times (TON_RISE, TOFF_FALL)
 - Fault thresholds and responses
 - Droop/Loadline resistance settings (VOUT_DROOP)
 - Control loop parameters (ASCR_CONFIG)
 - Switching Frequency (FREQUENCY_SWITCH)
 - Startup rise time factor (MULTI_PHASE_RAMP_GAIN)

Appendix 2: Parallel Command Reference for BMR463/464/466

The tables below give a detailed description of the configurations required by or related to current sharing modules. Refer to [AN302](#) for a detailed specification of each command.

GCB_CONFIG

Bits	Purpose	Configuration
15:13	Reserved	These bits are not used and should be set to 0.
12:8	Broadcast Group	Typically set to 0 for all devices. For a current sharing group that shall be enabled by the PMBus, the Broadcast Group value must be set the same of each product in the group. If there are other products connected to the same GCB bus, they must also have the same Broadcast Group if any sequencing of fault-spreading functions are used. For more information, see section Broadcast Enable and Margining.
7:6	Reserved	These bits are not used and should be set to 0.
5	GCB TX Inhibit	Set this bit to 0 (default value) for each product in the group to enable GCB communication.
4:0	GCB ID	Sets the rail's GCB ID for sequencing and fault spreading. Assign the same rail GCB ID to each product in the current sharing group. If there are other non-current sharing products connected to the same GCB bus, make sure that those rails have a unique rail GCB ID. This ID value must be the same as the IShare GCB ID set in ISHARE_CONFIG.

Examples:

GCB_CONFIG = 0x0000 GCB_ID = 0, Broadcast Group = 0

GCB_CONFIG = 0x0407 GCB_ID = 7, Broadcast Group = 4

ISHARE_CONFIG

Examples:

Bits	Purpose	Configuration
15:8	IShare GCB ID	Set to the same GCB ID as in GCB_CONFIG for each product in the current sharing group.
7:5	Number of Member	For each product in the current sharing group, set to the number of products in the group - 1. Example: 3 products in the group use 3 - 1 = 2.
4:2	Member position	Defines position of product in the group. The main with position 1 is assigned value 0 and the secondaries are assigned values 1, 2, 3, ...
1	Reserved	This bit is not used and should be set to 0.
0	IShare control	Set this bit to 1 for each product in the current sharing group. This enables current sharing.

ISHARE_CONFIG = 0x0721 GCB_ID = 7, Position 1 in a group of 2 products

ISHARE_CONFIG = 0x0725 GCB_ID = 7, Position 2 in a group of 2 products

MFR_CONFIG

Bits	Purpose	Configuration
15:11	Current Sense Blanking Delay	This delay parameter controls the blanking time (ns) after switching the top or bottom FET, preventing switch noise from disturbing the current measurement circuit. Normally the default value used for each product will be enough but in some applications an increased value might be needed.
10:8	Current Sense Fault Count	Set according to system design requirements. Normally the default values shall be used for each product in the current sharing group.
7:6	Reserved	
5:4	Current Sense Control	
3	NLR During Ramp	Shall be set to 0 (default) for each product in the current group.
2	Alternate Ramp Control	Shall be set to 1 (alternate ramp enabled) for each product in the current sharing group.
1	PG Pin Output Control	Set according to system design requirements.
0	SYNC Pin Output Control	Set according to system requirements (open drain or push-pull output) for products in the group that is configured to output sync clock. For products using the SYNC pin as input this bit can be set to either 0 or 1.

Examples:

MFR_CONFIG = 0x8F14 SYNC pin output as open-drain

MFR_CONFIG = 0x8F15 SYNC pin output as push-pull

USER_CONFIG

Bits	Purpose	Configuration
15:13	Minimum Duty Cycle	The minimum allowable duty cycle must be enabled to ensure that each phase starts the turn-on ramp with the same pulse width. For each product in the group, enable a minimum duty cycle of FSW / 256, i.e. bits 15:13 = 001.
12	Alternate Ramp Down	Set according to system design requirements. Normally set to 0 for each product in the current group (default value).
11	SYNC Time-out Enable	
10	Reserved	
9	PID Feed-forward Control	
8	Fault spreading mode	If fault spreading shall be used for the current sharing rail, set this bit to 1 for each product in the current sharing group.
7	Reserved	This bit is not used and should be set to 0.
6	Sync Input Mode	For each product in the current sharing group, except the one that possibly will be used to generate sync clock, this bit shall be set to 1 (force the SYNC pin to be input). For a product that shall be used to output sync clock this bit shall be set to 0.
5	Sync Output Control	Set to 1 for products in the current sharing group that shall be used to output sync clock from the SYNC pin. Make sure the SYNC Output Mode bit in MFR_CONFIG is set according to the system design requirements for these products. For each product in the group that uses the SYNC pin as an input the Sync Output Control bit shall be set to 0 (default).
4:3	Reserved	Set to 0 for each product in the current group (default value).
2	OFF low-side control	
1:0	Standby Mode	Monitoring must be enabled for all products in the current sharing group (bits 1:0 = 01 = default value). This ensures that the firmware is initialized prior to enabling the output voltage.

Examples:

USER_CONFIG = 0x2031 SYNC pin as clock output, fault spreading disabled

USER_CONFIG = 0x2051 SYNC pin as clock input, fault spreading disabled

USER_CONFIG = 0x2151 SYNC pin as clock input, fault spreading enabled

If the Current Sense Blanking Delay, BlankDelay, is increased the read READ_IOUT value will be affected by a small offset. To compensate for this the existing IOUT_CAL_OFFSET value can be changed according to the approximate formula below (it is assumed that bits 5:4 Current Sense Control is unchanged = down slope sense).

Where L = Output inductor value of the product (model dependent).

MISC_CONFIG

Bits	Purpose	Configuration
15	Broadcast Margin	If broadcast margining or enable shall be used (see GCB_CONFIG) for the current sharing group these bits must be set accordingly. The same setting must be used for each product in the group. Note that Broadcast Enable can be used only when PMBus on/off control is used. If using on/off control by the CTRL pin, the CTRL pin of each product in the group must be connected to the enable signal.
14	Broadcast Enable	
13	Phase Enable Select	Shall be set to 1 (= phase add/drop by PHASE_CONTROL command) for each product in the current sharing group.
12:9	Reserved	Set according to system design requirements. Normally set to 0 for each product in the current group (default value).
8 *	IOUT_OMEGA_OFFSET calibration	
7 *	Precise Ramp-Up Delay	If Precise Ramp-Up Delay is supported by the product used, this bit shall be set to 1 (=Precise Ramp-up Delay disabled) for each product in the current sharing group.
6	Diode Emulation	Set according to system design requirements. Normally the default values shall be used for each product in the current sharing group. Diode Emulation and Adaptive Frequency is not supported with current sharing and shall be disabled.
5:3	Reserved	
2	Minimum GL Pulse	
1	Snapshot	
0 *	Adaptive Frequency	

* These bits are not supported by some product models, see [AN302](#) or Flex Power Designer.

Examples:

MISC_CONFIG = 0x2082	No broadcast functions
MISC_CONFIG = 0x6082	Broadcast Enable activated
MISC_CONFIG = 0xA082	Broadcast Margining activated

DEADTIME_CONFIG

Bits	Purpose	Configuration
15	H-L Deadtime Mode	Set to 1 in order to disable the adaptive deadtime algorithm.
14:8	Min Deadtime H-L	Not applicable when the adaptive deadtime algorithm is disabled.
7	L-H Deadtime Mode	Set to 1 in order to disable the adaptive deadtime algorithm.
6:0	Min Deadtime L-H	Not applicable when the adaptive deadtime algorithm is disabled.

Example:

DEADTIME_CONFIG = 0x8080 Adaptive deadtime algorithm disabled for both H-L and L-H deadtimes

DEADTIME

Product	H-L Deadtime (Bits 15:8)	L-H Deadtime (Bits 7:0)	DEADTIME
BMR 463 xxx2 / xxx BMR 463 xxx6 / xxx	30 ns	12 ns	0x1E0C
BMR 463 xxx8 / xxx BMR 463 xxx9 / xxx	24 ns	12 ns	0x180C
BMR 464 xxx2 / xxx	30 ns	20 ns	0x1E14
BMR 464 xxx8 / xxx	24 ns	20 ns	0x1814
BMR 466 8x04 / xxx	24 ns	20 ns	0x1814

Example:

DEADTIME = 0x1E0C H-L deadtime = 30 ns, L-H deadtime = 12 ns

VOUT_COMMAND

Each current sharing phase must be set to the same output voltage. Since the droop/current sharing algorithm will need headroom to adjust the output voltage, it is recommended to keep VOUT_COMMAND below $0.96 \times VOUT_MAX$.

The user might want to increase the nominal output voltage by an offset in order to compensate for the load-line droop. Typically an offset magnitude of

$0.5 \times I_{MAX} \times RDROOP$ would be used.

VOUT_TRIM

Writing this command will have no effect for products in a current sharing group since the command is used by the current sharing algorithm. The main phase will always retain a zero VOUT_TRIM value, while each secondary phase will adjust its VOUT_TRIM value until all phases carry equal load current.

VOUT_CAL_OFFSET

The VOUT_CAL_OFFSET parameter contains a calibration value from production and should not be changed. If an offset voltage is desired to overcome the effects of droop, the value of VOUT_COMMAND should be adjusted.

VOUT_DROOP

Droop resistance is used as part of the current sharing algorithm. Each product in the group shall be assigned the same VOUT_DROOP value, which will be the effective droop (or loadline) of the whole group. Since the total current is shared between the products in the group, the droop of each individual phase will be set higher than the configured VOUT_DROOP value.

Example for a current sharing group with four products:

VOUT_DROOP value assigned to all four products	0.25 mV/A
Effective Vout droop (loadline of the group output)	0.25 mV/A
Individual Vout droop per phase (when all phases active)	$0.25 \times 4 = 1.0 \text{ mV/A}$

The assigned effective droop is maintained even when phases are added or dropped which means the individual droop of each phase is automatically adjusted.

It is recommended to assign a VOUT_DROOP value that gives an individual droop between 0.5 and 1.5 mV/A per phase. In general current sharing balance is improved with higher droop. A too high droop may cause instability at high loads. The highest possible droop for stable operation decreases as temperature and output load increases. The graphs in Figure A1 and Figure A2 show the recommended maximum individual droop per phase vs output voltage and maximum output current, assuming operation at a maximum temperature of +95°C.

In order not to affect the configured over current protection (OCP) threshold; the maximum output current used when defining maximum droop should be equal to the configured OCP threshold.

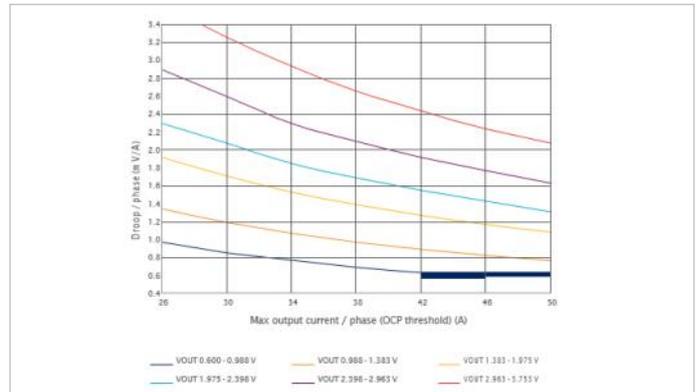


Figure A1: Recommended max individual droop per phase vs Vout and max Iout for BMR464

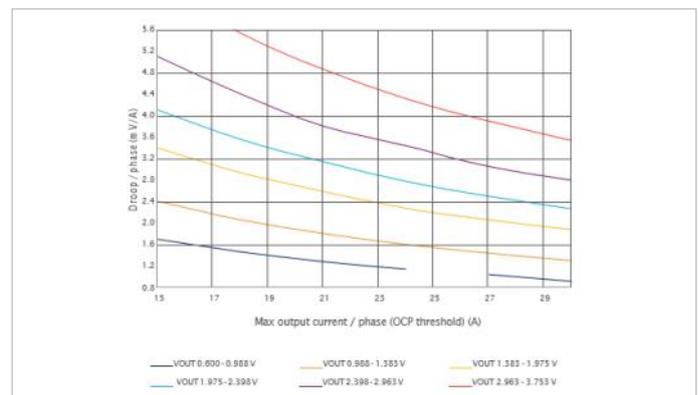


Figure A2: Recommended max individual droop per phase vs Vout and max Iout for BMR463

TON_DELAY

For each secondary phase the TON_DELAY parameter shall be set equal to 5 ms or higher. For the main phase TON_DELAY shall be set at least 10 ms higher than the TON_DELAY value used for each secondary phase. The resulting delay times used for the common output will be the one set for the main phase.

TOFF_DELAY

Same configurations rules as for TON_DELAY.

TON_RISE, TON_FALL

The TON_RISE and TON_FALL values must be equal for each phase in the group. For a current sharing group there is an upper limit to the ramp time that can be used. The limit will depend on the used switch frequency, input voltage and output voltage. Figure A3 shows the approximate maximum ramp time when considering the whole input voltage range 4.5-14 V. It is recommended to use ramp times in the range 5 to 10 ms.

FREQUENCY_SWITCH

If the current sharing group uses an external clock, the FREQUENCY_SWITCH value shall be set to the frequency value of the external clock.

The FREQUENCY_SWITCH value shall be equal for each product in a current sharing group.

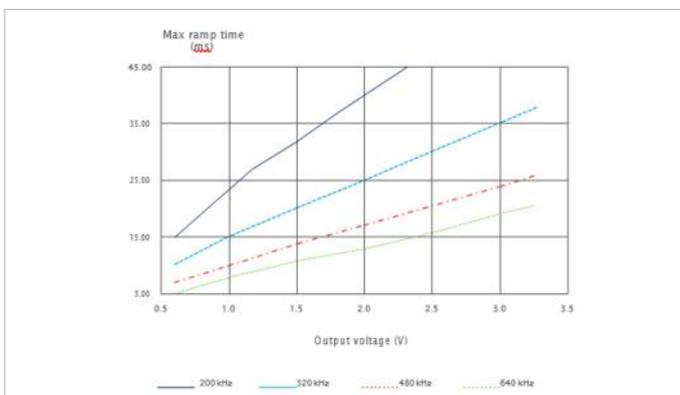


Figure A3: Max ramp time vs output voltage and switch frequency

ON_OFF_CONFIG

The configuration of ON_OFF_CONFIG must be

equal for each product in a current sharing group. Ramping down the output at turn-off is mandatory which means bit 0 in ON_OFF_CONFIG must be set to 0.

Note that if enabling by the PMBus is used, Broadcast Enable must be activated in MISC_CONFIG and GCB_CONFIG

Examples:

ON_OFF_CONFIG = 0x16 Enable by CTRL pin, active high polarity, ramp down at turn-off

ON_OFF_CONFIG = 0x14 Enable by CTRL pin, active low polarity, ramp down at turn-off

ON_OFF_CONFIG = 0x1A Enable by PMBus command OPERATION, ramp down at turn-off

OVUV_CONFIG

For products in a current sharing group the crowbar function must be turned off, i.e. bit 7 in OVUV_CONFIG must be cleared.

Example: OVUV_CONFIG = 0x0F

POWER_GOOD_DELAY

In order for the transition of compensator coefficients (see section Ramp Behavior) to not occur before ramp-up has finished, the POWER_GOOD_DELAY value should fulfill the equation below

$$POWER_GOOD_DELAY > 1.3 \times TON_RISE \times \frac{(VOUT_COMMAND - POWER_GOOD_ON)}{VOUT_COMMAND}$$

The POWER_GOOD_DELAY value shall be equal for each product in the group.

AUTO_COMP_CONFIG

The AUTO_COMP_CONFIG value shall be equal for each product in the current sharing group.

Bits	Purpose	Configuration
7:4	DLC Result Scaling	Set according to system design requirements. For current sharing rails, as a start value the following scaling levels are suggested: phases: 40% phases: 30% or 5 phases: 20% 6, 7 or 8 phases: 10%
3	Power Good Assertion	Set according to system design requirements. It is recommended to set this bit to 1 (default), i.e. assert PG after DLC algorithm has finished, due to the variation of the time the DLC algorithm takes.
2	DLC Result Store	Set according to system design requirements.
1:0	DLC Mode	Set to 00 (DLC disabled) or 01 (DLC algorithm once after ramp). Repetition of DLC algorithm every second or minute shall not be used for current sharing groups.

Example:

AUTO_COMP_CONFIG = 0x49

50% DLC scaling, Assert PG after DLC,
Do not store DLC to RAM, Perform DLC algorithm
after ramp



Flex Power Modules, a business line of Flex, is a leading manufacturer and solution provider of scalable DC/DC power converters primarily serving the data processing, communications, industrial and transportation markets. Offering a wide range of both isolated and non-isolated solutions, its digitally-enabled DC/DC converters include PMBus compatibility supported by the powerful [Flex Power Designer](#).

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