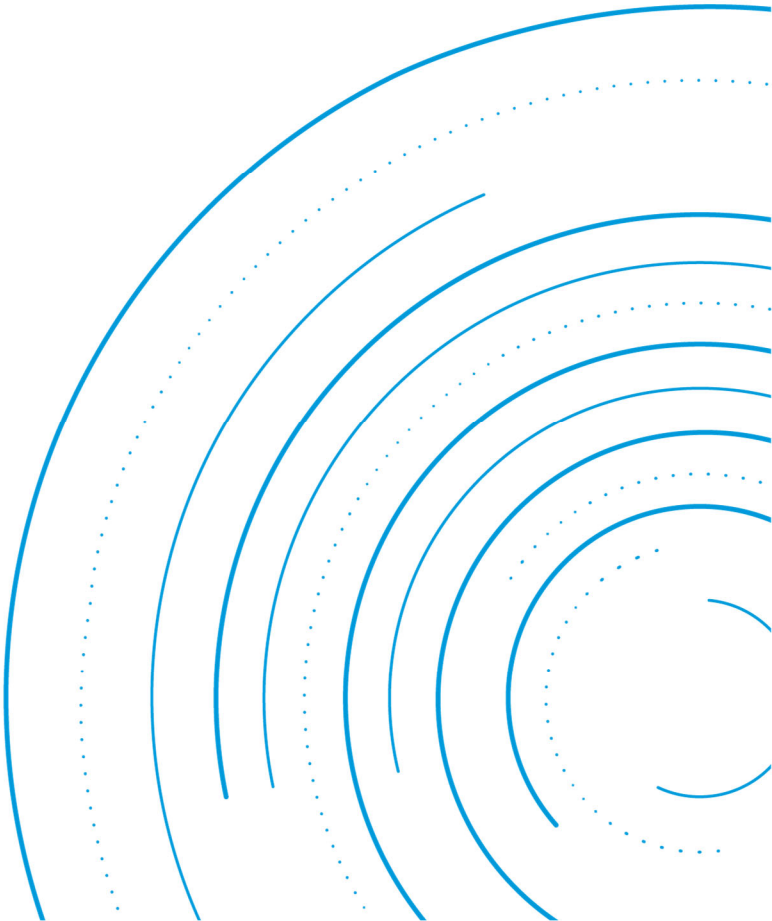
flex Power Modules

APPLICATION NOTE 328

Voltage Regulator Modules



Abstract

This application note provides information how to use voltage regulator modules.

This application note applies to the following products:

- **BMR510**
- **BMR511**

Contents

Introduction

PoLs (point of load converters) are placed closest to the load to reduce the impedance "R" of the PCB copper layer and to decrease the power loss (I^2R) caused by high currents.
In recent years, modules that add digital voltage regulation function but may require an external controller are called VRMs (voltage regulator modules). A circuit composed of discrete components is often called a VR (voltage regulator).
The typical payload of a POL/VRM are high-frequency multi-core processing/memory chips such as CPUs, GPUs, FPGAs, ASICs, and DRAM. As applications continue to increase in performance, the requirements for the main frequency are getting higher and higher. While maintaining the same power level, the voltage is getting lower and lower (but due to the limit of semiconductors, the minimum voltage of 0.5V should not be exceeded), the current is getting higher, and a single module output exceeding 100 A or even 1000 A has become the norm.

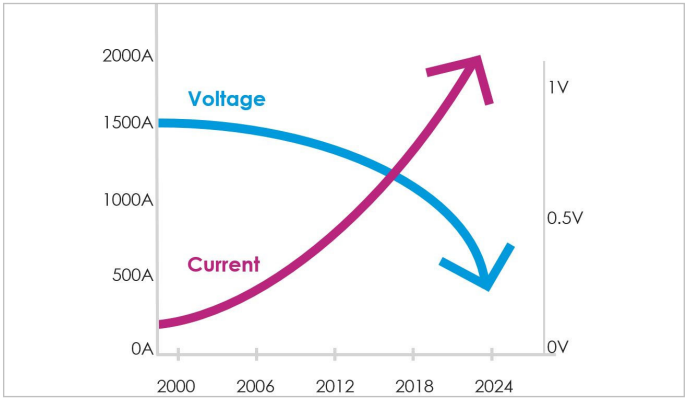


Figure 1: Progression of xPU, ASIC, FPGA peak current requirements

On the other hand, due to the characteristics of semiconductors, when the main frequency increases to 5 GHz or higher, the physical characteristics will change, and the cost will increase exponentially.
In this case, the solution of increasing the main frequency of a single core reverts to adding a number of physical cores/logical threads, and the corresponding multi-phase parallel connection of the power supply becomes the optimal solution. In addition, multi-phase solutions can also make thermal design easier.

Although control technology has become more complex and more efficient in recent decades, the basic buck topology is still chosen as the mainstream solution because of its simplicity and reliable architecture at the lowest price.
The most striking feature in the buck circuit is that each phase has a large output inductor. The neatly arranged output inductors on both sides of the CPU have become the hallmark of this type of power supply, as can be seen in the example below.

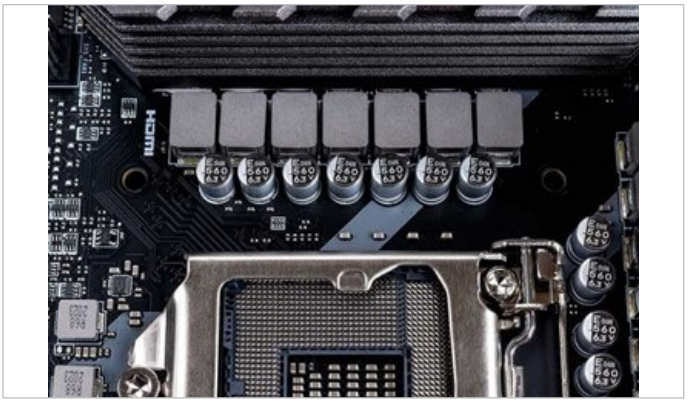


Figure 2: Output inductors

The typical input voltage of a PoL is 12 V, which is the output voltage derived from the AC/DC first level power supply of the system. The earliest computer systems used the 12 V bus which is still used today. This 12 V voltage can be stepped down by the buck circuit to numerous required power supply voltages, which facilitates the system design.
As the total power of the system continues to increase, the current of the 12 V bus has also become much larger. At this time, the power dissipated on the bus has gradually become more important.
There is a trend to use higher voltage bus systems, such as 48 V. When the bus voltage is increased to 48 V, which is 4 times the previous level, the power dissipated on the bus becomes 1/16th of the original 12 V bus. This advantage becomes more obvious.

This trend of bus voltage increase is not only seen in the field of microprocessors, but even automotive electronics has begun to evolve in this direction for the same reason.

The main functions of a PoL include start-up sequence control, status monitoring, parallel with interleave-phase current sharing, and load line regulation.

The main performance requirements of a PoL are board area, output power (including thermal derating), output voltage accuracy (DC), ripple (AC), and transient response.

Application Environment

Temperature

Usually, this type of application is defined as a general industrial application, and the temperature range is -40 °C to +85 °C. This only describes the operating environment temperature of the basic system. It can start and run normally, but it does not mean that the product can run at full load for a long time. Specifically thermal derating requires reference to the following:

- specific application power
- thermal derating reference curve of power supply products (preliminary simulation in design-in stage)
- actual measurement of the key components' temperature during stable operation vs. upper limit of critical operating temperature (real measurement of sample in actual thermal environment)

Altitude and isolation

Generally, by default, PoL and VRM products are non-isolated applications. However, there are also specific products that provide input and output isolation, such as the BMR482 products for example.
Products that provide isolation characteristics need to pay attention to the isolation voltage and applicable altitude range.

Monitoring, digital control and black box recording

Most of Flex Power Modules' current products are based on digital control technology. Through the digital interface of PMBus, the customer's host computer can poll the status of the running product (input voltage, output voltage, output current, internal temperature).

It also provides a triggerable level output SALERT, which can set a mask for the specific fault/warning preset for each power module. Once a specific fault/warning occurs, the SALERT level pull-down is triggered. Combined with the use of early warning, the host computer can be informed before a substantial failure occurs and intervention can be carried out in advance. For example, after an over -temperature warning occurs, the host computer can increase the speed of the cooling fan to prevent over-temperature protection from occurring. Once the temperature is normal, the host computer can command the fan to reduce to normal speed to extend the service life of the fan.

The event data recorder or "black box" recording function can record key information at the time when unexpected shutdown or failure occurs for subsequent diagnostic analysis. This data is stored in the NVM memory, and the information can be read through the Flex Power Designer (FPD) software.

Due to the fact that the black box function needs to be activated before each use and will occupy some storage space, our factory products do not have this function turned on by default. If it is necessary to use it, it should be activated using the customer's host computer program.

The storage space of some products is physically write-once One Time Programmable (OTP) but uses logical space management so that users can write multiple times, but the remaining space will become less and less. When using this type of product, you should note that once the number of black box recordings reaches the upper limit, subsequent data will not be recorded.

Data format conversion

There are three most common types of defined data when converting a 16-bit WORD to decimal:

Linear

In the Flex Power Designer software, this format is called Linear11. This is because in 16-bit when reading data, the high-order 5 bits represent the exponent of the data, and the low-order 11 bit represents the mantissa of the data.

This format is used for floating point data other than VOUT, such as VIN, IOUT

Figure 3: Linear11 format

For example, the above 96.5

96.5 $=2^{-3} * 772$, = 0xEB04

$2^{-2} * 386$, = 0xF182

$2^{-1} * 193$, = 0xF8C1

The FPD software comes with a format conversion tool.

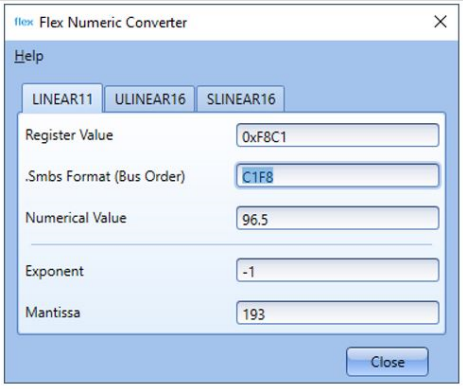


Figure 4: Flex Power Designer numeric converter

The register value in the first line is in the logical order of high byte first and low byte last. The SMBS value in the second line is the low byte first and the high byte last. This is in the time order of the physical waveform. The reason for this is that when the computer industry upgraded from 8-bit machines to 16-bit machines a long time ago, there was no place reserved for the high byte in advance, so the high byte could only be placed at the back. Please refer to the description of the PEC chapter on the next page.

Vout Linear

This format is used for floating point data of VOUT. In the Flex Power Designer software, this format is called Linear16. This is because in 16-bit it is all data, and the exponent of the data is placed in the 0x20 VOUT_ MODE register. This index is read-only and does not change.

Figure 5: Linear16 format

DIRECT

This format is used for other types of data. To convert the 16-bit data, it also needs three other coefficients m, b and R for further conversion

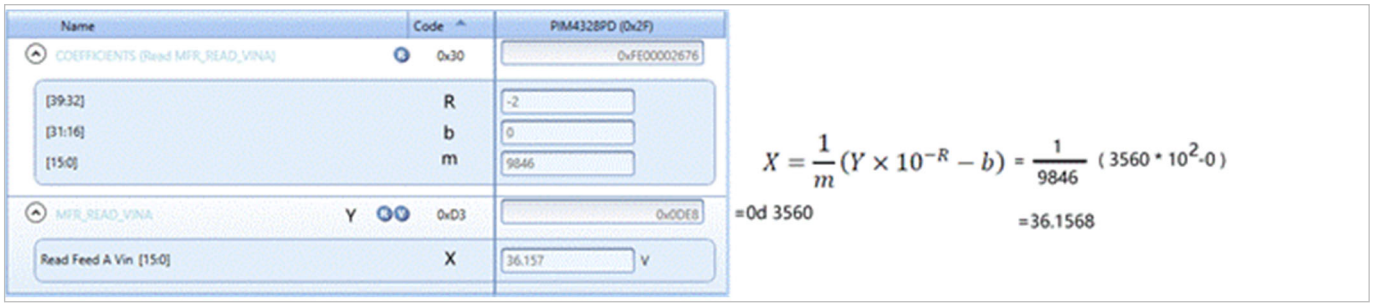


Figure 6: Direct format

Although m, b, R changes according to the scene, the most commonly used set of values is, m =1, b=0, R=0. At this time, X=Y, that is to say, just convert the 16-bit value directly into decimal. This is why this format is called DIRECT.
The advantage of using this format is that when the program processes physical values, it can directly use integer instead of use floating point calculations, saving calculation time and resources.

PEC

PMBus is based on the I2C physical communication protocol. The advantage of this protocol is that the minimum number of lines is used: GND, SDA and SCL, and those do not require shielding. The disadvantage of this protocol is that communication can be easily susceptible to interference, especially when used in switching power supplies. Because there is a large switching voltage jump on the switching node which even affects the ground level, this physical noise is difficult to avoid.

It is recommended to use logical calculations CRC value to verify that the content of the communication is correct. The calculation of PEC is based on the 8-bit cyclic check calculation of each byte. At this time, the PMBus 7-bit address needs to be added with R = 1 / W = 0 to make 8-bits for calculation.

The flag bits of the frame do not need to be included in the calculation of PEC, such as START, ACK, NACK, and STOP.

As shown in the following example, when reading the 0x21 register VOUT_COMMAND at the 0x41 address to the value 0xA000, according to the timing frame structure defined by SMBus, it should be

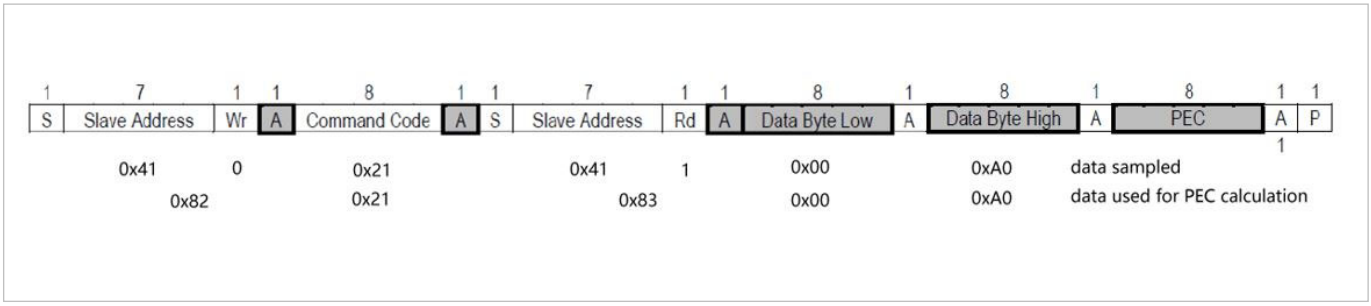


Figure 7: SMBUS frame structure

PEC adopts cyclic check that is each byte of a string of data, from front to back, first performs a CRC 8 operation, and then performs an XOR calculation with the next byte. The new result then performs a CRC 8 operation, and then performs an XOR calculation with the next byte, and so on, until the last byte. CRC 8 has different algorithms and parameters in different fields. The parameter group used by PEC is:
polynomial formula x8+x2+x+1, bit width 8 bit, Polynomial: 0x07, initial value 0x 00, final value 0x00.
The most convenient and fast calculation of CRC 8 is to check table method

	0x*0	0x*1	0x*2	0x*3	0x*4	0x*5	0x*6	0x*7	0x*8	0x*9	0x*A	0x*B	0x*C	0x*D	0x*E	0x*F
0x0*	0x00	0x07	0x0E	0x09	0x1C	0x1B	0x12	0x15	0x38	0x3F	0x36	0x31	0x24	0x23	0x2A	0x2D
0x1*	0x70	0x77	0x7E	0x79	0x6C	0x6B	0x62	0x65	0x48	0x4F	0x46	0x41	0x54	0x53	0x5A	0x5D
0x2*	0xE0	0xE7	0xEE	0xE9	0xFC	0xFB	0xF2	0xF5	0xD8	0xDF	0xD6	0xD1	0xC4	0xC3	0xCA	0xCD
0x3*	0x90	0x97	0x9E	0x99	0x8C	0x8B	0x82	0x85	0xA8	0xAF	0xA6	0xA1	0xB4	0xB3	0xBA	0xBD
0x4*	0xC7	0xC0	0xC9	0xCE	0xDB	0xDC	0xD5	0xD2	0xFF	0xF8	0xF1	0xF6	0xE3	0xE4	0xED	0xEA
0x5*	0xB7	0xB0	0xB9	0xBE	0xAB	0xAC	0xA5	0xA2	0x8F	0x88	0x81	0x86	0x93	0x94	0x9D	0x9A
0x6*	0x27	0x20	0x29	0x2E	0x3B	0x3C	0x35	0x32	0x1F	0x18	0x11	0x16	0x03	0x04	0x0D	0x0A
0x7*	0x57	0x50	0x59	0x5E	0x4B	0x4C	0x45	0x42	0x6F	0x68	0x61	0x66	0x73	0x74	0x7D	0x7A
0x8*	0x89	0x8E	0x87	0x80	0x95	0x92	0x9B	0x9C	0xB1	0xB6	0xBF	0xB8	0xAD	0xAA	0xA3	0xA4
0x9*	0xF9	0xFE	0xF7	0xF0	0xE5	0xE2	0xEB	0xEC	0xC1	0xC6	0xCF	0xC8	0xDD	0xDA	0xD3	0xD4
0xA*	0x69	0x6E	0x67	0x60	0x75	0x72	0x7B	0x7C	0x51	0x56	0x5F	0x58	0x4D	0x4A	0x43	0x44
0xB*	0x19	0x1E	0x17	0x10	0x05	0x02	0x0B	0x0C	0x21	0x26	0x2F	0x28	0x3D	0x3A	0x33	0x34
0xC*	0x4E	0x49	0x40	0x47	0x52	0x55	0x5C	0x5B	0x76	0x71	0x78	0x7F	0x6A	0x6D	0x64	0x63
0xD*	0x3E	0x39	0x30	0x37	0x22	0x25	0x2C	0x2B	0x06	0x01	0x08	0x0F	0x1A	0x1D	0x14	0x13
0xE*	0xAE	0xA9	0xA0	0xA7	0xB2	0xB5	0xBC	0xBB	0x96	0x91	0x98	0x9F	0x8A	0x8D	0x84	0x83
0xF*	0xDE	0xD9	0xD0	0xD7	0xC2	0xC5	0xCC	0xCB	0xE6	0xE1	0xE8	0xEF	0xFA	0xFD	0xF4	0xF3

Figure 8: CRC 8 look up table

For example, you can find from the above table that the calculation of CRC8(0x 82)=0x87
XOR is the value obtained by performing XOR operation on each corresponding bit of the two bytes . XOR(1,1)=0, XOR(0,0)=0, XOR(0,1)=1, XOR (1,0)=1,
To calculate the PEC of 0x82, 0x21,0x83,0x00,0xA0

CRC8(0x82) =0x87
0x87 XOR 0x21 =0xA6
CRC8(0xA6) =0x7B
0x7B XOR 0x83 =0xF8
CRC8(0xF8) =0xE6
0xE6 XOR 0x00 =0xE6
CRC8(0xE6) =0xBC
0xBC XOR 0xA0 =0x1C
CRC8(0x1C) =0x54 - this is the final PEC result.

Save after reconfiguration

When reconfiguring the product using the PMBus interface, be sure to turn off the Vout by ENABLE / RC before saving. It is dangerous to change the configuration of the working module. After executing the save command, you should wait for 500 ms and then turn off the input voltage. It is recommended to turn on PEC during the configuration process to prevent communication errors.

Voltage stabilization

The output voltage of most products is fully regulated. However, there are some first level power supply products that are exceptions. When selecting, you need to confirm based on the voltage range required by the load characteristics.

Compared with products whose output voltage is fully regulated under full input voltage conditions, there is a type of first level power supply HRR product, which is designed to operate under the most common operating conditions (such as telecommunications applications, where the input voltage is 53 V for almost 99 % of the working time). The efficiency is maximized at the expense of the output voltage value under a certain input voltage range (for example, 36~40 V). The characteristic curve of this output voltage is described in the product specification. This product focuses on providing maximum bus power and conversion efficiency. The bus post-stage also has regulated PoL/VRM products to drive real loads, so it generally does not cause problems for applications.

Due to the characteristics of certain topologies, the function of some products is to provide isolation and voltage fixed ratio conversion. Such products tend to be very efficient. When selecting these products, you also need to pay attention to the fact that the output voltage follows the input voltage, rather than being a fixed voltage regulation value. Another potential problem with this type of product is that it does not have an input voltage transient following function. Please refer to the relevant chapters to select this type of product, which requires a compromise between efficiency and performance.

The second level power supply needs to be regulated.

Output voltage adjustment

The traditional PoL is a constant voltage power supply with stable voltage output. Because current processor loads face different computing loads, the operating frequency is often not a fixed value. When the amount of calculation is large or overclocking is required, a higher voltage is required.
At this time, the processor will use a special control bus to inform and command the power supply to quickly change the output voltage to the required value through communication. In actual applications, the voltage is constantly changing. This type of advanced PoL is called a VRM. The control signal is called VID. If the control signal has multiple lines > 4, PVID form is often used. If the control signal is for very few lines < 4, the SVID form is often used.

Intel's dedicated control bus is called VR, and the current highest version has evolved to VR14. The earliest CPU used a parallel bus, using 5/6 parallel control lines (older version Pentium Xeon/newer version CPU).

Traditional among the 5 lines, VID 4 is MSB and VID 0 is LSB = 25 mV.
Among the 6 lines of the new version, the newly added VID 5 is used to improve accuracy, and the LSB is smaller than VID 0 =12.5 mV. The highest signal frequency of the parallel VID bus is 200 KHz. It has many signal lines, occupies a large board area, and is susceptible to interference. Intel later used the serial SVID (serial voltage-identifier) bus that can communicate in both directions. It is physically composed of three data lines VCLK, VDIO, ALERT # plus ground wire and constitutes a 4-wire system. This data bus has a speed of 25 MHz and is a high-speed circuit. During layout, it is necessary to isolate the MOSFET switching noise from the switch node. The wiring cannot be close to or placed on the back of the switch node (MOSFET and output inductor). The wiring requirements are in accordance with the specifications of the RF signal. The line spacing should be such that the impedance of the signal to the ground plane is 50 Ohm.

AMD's dedicated control bus is called SVI. The current version has evolved to SVI3. The main communication lines that make up SVI3 are SVC (clock) and SVD (data). Its data structure is similar to SMBUS. The maximum rate is 50MHz. During the board layout It is also required to pay attention to preventing noise interference and impedance matching.

In addition to Intel and AMD, the industry-wide control bus is called AVSBUS, and the current version is PMBus 1.3 part 3. Its data structure is similar to SPI. AVS BUS has three lines besides GND: AVS_ MDATA; AVS_SDATA; and AVS_CLOCK. When the SLAVE device does not need to actively communicate with the MASTER device, the AVS_SDATA line may also be missing. The speed of the AVSBUS bus is 5 - 50 MHz.

Output voltage ripple and output capacitor selection

DC/DC conversion is achieved through AC conversion, and the residual AC signal on the output voltage is ripple. The amplitude of this ripple is related to the inductance of the last stage inductor and the output capacitance. When designing customer applications, please refer to the capacitance used when testing ripple in our specifications. Because the source of this residual ripple comes from the transient square wave on the switching node, its high-frequency harmonics are very rich. When configuring capacitors, capacitance value is not the only factor, better to mix different types and capacitance values with various capacitors. The purpose of this is that different capacitors have different ESRs, and these different capacitors will suppress the high-frequency harmonics of the output ripple at each frequency. If the client cannot adopt the capacitance range recommended in our specification due to actual conditions, then it is necessary to consider the actual ripple amplitude, the hold-up time required by the payload circuit, and whether the stability of the feedback loop needs to be re-evaluated.

Input capacitor selection

The function of the VRM input capacitor is to filter the ripple of the input voltage, provide energy to the power stage when the output is dynamically transient, and stabilize the input voltage to prevent oscillation.

When selecting the capacitor, in order to filter ripple:
$C = (I * \Delta V) / (f * \Delta Vr)$
Where: C = Required input capacitance (Farads)
I = Maximum load current (Amperes)
ΔV = Maximum allowable input voltage ripple (Volts)
f = Switching frequency of the VRM (Hertz)
ΔVr = Voltage ripple reduction factor (typically 0.1 to 0.2)

Capacitors are selected to provide transient energy:
C = (ΔV * I * T) / (ΔVr * Vr)
Where: C = Required input capacitance (Farads)
ΔV = Maximum allowable output voltage deviation during load change (Volts)
I = Load current change rate (Amperes per second)
T = Time required to recover from the load change (seconds)
ΔVr = Voltage ripple reduction factor (typically 0.1 to 0.2)
Vr = Output voltage ripple (Volts)

Under the premise that the capacitance value has been determined, the smallest possible ESR/ESL capacitor should be selected, such as MLCC. At the same time, it is also necessary to consider the sufficient withstand voltage and the derating of the capacitor value due to the applied voltage.

Output dynamic load transients

A common scenario in PoL/VRM applications is that when the load current changes instantaneously, the voltage drop caused by the large current will cause the output voltage to change in the opposite direction of current. In order to correct this change, the VRM controller will adjust the control signal PWM at this time to return the output voltage to normal as soon as possible. This capability is evaluated by measuring the amplitude of the voltage overshoot, undershoot, and recovery time. For VRM, undershoot is often more demanding. For an analog control loop, the implementation method is to use an operational amplifier. The positive and negative input terminals of the operational amplifier are connected to the output voltage and the reference voltage respectively. By adjusting the RC network parameters between the output terminal and the input terminal of the operational amplifier, the control loop can be controlled. The amplitude and phase of the different frequency signals of the negative feedback signal are adjusted to ultimately achieve the minimum overshoot and undershoot and the shortest recovery time.

For digital control ICs, when implementing the feedback loop, the amplitude and phase response adjustment in the frequency domain is converted to the time domain. The error signal is sampled by the ADC at each clock cycle to form a continuous array, and processed with 3 coefficients: the current time slot error is superimposed on the P coefficient; the gradually changing integral error signal that exists for several cycles is superimposed on the I parameter; and the differential error signal that suddenly changes rapidly in the last one or two cycles is superimposed on the D parameter, so as to achieve the equivalent compensation results as the analogue control loop.

In addition, because the digital control loop has the flexibility of programmed control, it also adds an enhanced loop to improve performance that cannot be realized at low cost with the traditional analog loop:

Method 1 is that not only the frequency response is used, but also the amplitude of the error signal is introduced into compensation. For larger error signals, the duty cycle change value of the calculated output is directly modulated. In this way, the small signal disturbance does not change, and the large signal disturbance is artificially increased by the correction amount. This method is called NLR (Non-Linear Response).

Method 2 is real-time adjustment. Since the switching frequency of the buck circuit is hundreds of kHz to several thousand kHz, and the common duty cycle is 1:12, which means that adjustment intervals are in the millisecond range, and the adjustment duration is in the 0.1 ms level, there is only a fixed duty cycle value within this adjustment. This adjustment is not near enough for the rapid change rate in the microseconds level, and it often takes dozens of cycles to correct back to the voltage target value.

In response to this demand, digital control circuits can improve the loop by adding additional tiny pulses in real time. This tiny pulse is different from ordinary PWM, in that its width is not modulated but fixed, for example, 1/256th of a switching period, and the quantity of the pulses can be modulated in real time by the amplitude of the error signal, which can be considered as PDM.

This improvement method often requires manual adjustment of the entry and exit conditions and the minimum and maximum number of tiny-pulses. It is a specific improvement for the suppression of special disturbances, which is very suitable for load dynamic transient scenarios.

When testing dynamic transients, the transient speed of the load is an important test condition. PoL/VRM transient testing often requires a level of 100 A/us or even 1000 A/us, which requires dedicated testing equipment. The wiring of this type of test must be the shortest, so as to minimize the parasitic inductance and thus not reduce the transient slew rate.

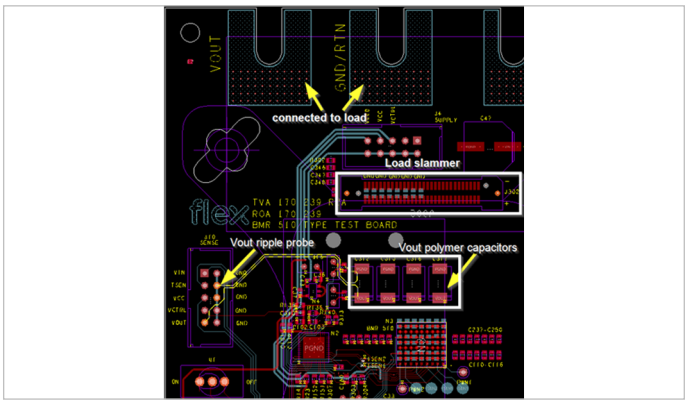


Figure 9: Arrange the load slammer position closest to the power

Transient power

For a regulated power supply, the output current and output power are directly proportional. The overcurrent protection point also corresponds to the maximum output power protection point. However, in PoL/ VRM applications, there can be a burst mode, and the load may need to consume more power than TDP for a slightly longer period of time (for example, some ms or even 1 second), but it is required that OCP cannot be triggered. This time-length related OCP setting is called transient power. This is often a set of OCP settings that correspond to time and output current and are inversely proportional.

Input voltage transient following

In telecommunications applications, the AC/ DC power supply may switch to the backup battery power supply due to an AC power outage. After a period of use, the backup battery energy is exhausted, and it will be forced to switch back to the AC/DC power supply. This switching occurs transiently within a time unit of microseconds, and the change amplitude is also very high, such as 36 V - 60 V. In this case, it is a common requirement that the output voltage of the downstream power supply is not affected.

For general power supplies with switching frequencies of 100-1000 kHz, in order to maintain loop stability, the bandwidth of the negative feedback loop at the output end is often far smaller than the switching frequency. With such a feedback loop bandwidth, there is no way to promptly compensate for changes in the output voltage caused by the input voltage.

The usual solution is to have an additional feed-forward loop at the input that changes the duty cycle in real time specifically for this situation. For an analog feedforward loop, this compensation can be compared to "AND" using the input voltage and the triangle wave that generates the PWM signal, thereby obtaining real-time adjusted feedforward compensation. For digital feedforward loops, due to the delay of the sampling circuit, they cannot achieve the same real-time high-speed compensation as analog circuits. An approximate compensation duty cycle needs to be obtained through calculation.

Output voltage feedback loop stability

As a voltage stabilizing module, the output voltage needs to maintain a consistent and stable output value over time. There are many factors that affect the stable voltage output, such as changes in the characteristics of components caused by temperature changes; voltage fluctuations caused by changes in output current; voltage changes caused by receiving commands from the host computer etc. Inside the control circuit, after sampling the output voltage and comparing it with the reference voltage to obtain the difference, this part of the circuit that changes the duty cycle of the output PWM signal through certain rules is called a feedback loop. Evaluate the characteristics of the feedback loop, including bandwidth in the frequency domain, overall stability of the loop, and transient response in the time domain.

The output inductor with energy storage function in PoL/VRM needs to operate at the optimal switching frequency corresponding to its volume. The time window of each cycle of this frequency is the only possible opportunity to adjust the PWM duty cycle of the output voltage, so if a disturbance occurs at a frequency higher than the switching frequency, this exceeds the adjustment limit of the feedback loop. This type of interference suppression requires the passive component MLCC as the output capacitor, which relies on its very low ESR and a large number of parallel connections to achieve high energy absorption and release of fast charge and discharge implementation. These capacitors should be as close to the load point as possible.

These output capacitors, as part of the control feedback loop, can affect loop stability. Generally speaking, the transient suppression capability and stability of the loop are a pair of conflicting indicators: stronger suppression capability often requires a larger error gain, which is detrimental to stability.

To evaluate whether a feedback loop can achieve stability (convergence) rather than oscillation, the control field has provided operational evaluation methods and theoretical support: Bode plot measurement.

In order to compensate for the line loss voltage caused by outputting large current, the PoL/VRM module will have a +SENSE pin. There is a SENSE resistor of dozens of ohms between this pin and +VOUT, just in case the +SENSE terminal is poorly connected, the control circuit will sample the VOUT value through the internal SENSE resistor. When evaluating loop stability, you need to locate this resistor, disconnect it, and introduce an AC signal to simulate normal operation by connecting it in series to the secondary side of the signal transformer while maintaining the DC level. In practice, the AC signal can also be connected in parallel across the SENSE resistor. The injected signal is connected to a sinusoidal signal generator through a DC blocking 1:1 transformer. The amplitude of the signal is set at the 1 % level of the PoL/VRM output voltage. This is called a small signal. The frequency of the signal is 100 Hz -100 kHz. The low frequency starting from 100 Hz is to ensure the conversion linearity of the injected signal transformer. The high frequency ends at 100 kHz because it is close to the switching frequency. Too high frequency interference is impossible to adjust through the control loop, so a higher test frequency is meaningless.

During the process of testing the loop stability, the signal generator will generate a small interference signal and inject it into the circuit at the SENSE resistor. By comparing the amplitude/phase of this interference signal with the output level of the POL/VRM after the loop has suppressed the interference, it is a bode diagram.

The bode diagram always has the largest amplitude at the starting frequency of 100 Hz. Its physical meaning is that the basic function of a POL/VRM is voltage stabilization, that is, for a DC/low-frequency interference, it must have great negative feedback correction capabilities. The amplitude will gradually decrease as the frequency increases. The amplitude of the highest frequency on the right end of the figure should be very small, which means that the feedback loop cannot feedback signals close to the switching frequency to avoid the occurrence of oscillation. When the amplitude is 1, (the first amplitude crosses 0dB), the frequency value on the horizontal axis is defined as the bandwidth of the feedback loop, also known as the crossover frequency. Its physical meaning is that interference signals with frequencies lower than this bandwidth will be suppressed by the feedback circuit to generate enough negative feedback. A larger loop bandwidth means that the loop has a faster ability to correct for high-frequency disturbances, such as the most common situation is output load transients. However, this bandwidth cannot be designed too high. When it is close to the switching frequency, if there is still a large gain instead of attenuation, the switching signal will be mistaken for noise on the output voltage, thereby generating negative feedback, which can easily cause self-excited oscillation. Empirical values indicate that the optimal loop bandwidth is 1/10th-1/6th of the switching frequency.

In addition to the above-mentioned loop bandwidth as an important performance indicator, there are two other quantitative indicators related to loop stability:

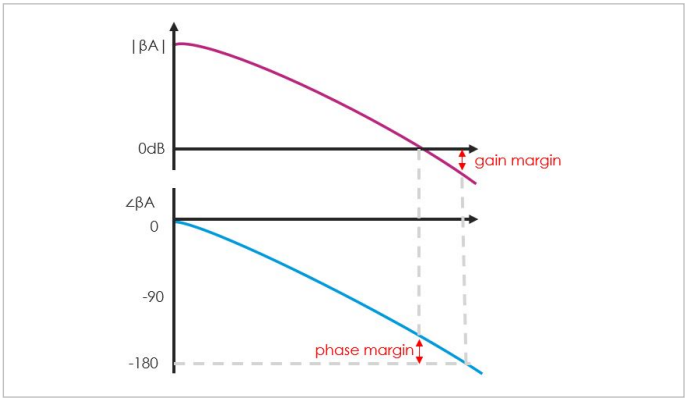


Figure 10: Phase and gain margin

Gain margin: the attenuation value when the phase difference between the feedback signal and the small interference signal is 180°. (Since the feedback circuit is connected to the negative end of the op amp, in order to facilitate the reading of the diagram, the horizontal axis frequency and the vertical axis can intersect at 0° on a bode phase diagram, on most of the bode plot). The attenuation value at this time represents the open loop of the feedback transfer function and generates a negative feedback signal that is exactly in phase with the interfering small signal and is connected to the closed loop. In order to stabilize the final output of the closed loop, the amplitude of this signal must be smaller than the amplitude of the interfering small signal, otherwise the loop will be unstable: Negative feedback is overkill and will produce larger errors that are in inverse phase with the interfering signal. The negative of this attenuation value is defined as the gain margin. Theoretically, this value greater than 0 dB is a necessary condition for system stability. However, because the test conditions are single, taking into account the test parameter variations that cannot be fully covered, such as device parameter changes caused by different ambient temperatures, and long-term degradation of capacitance. The resulting changes in capacitance, derating of device capacitance and inductance caused by different test voltages and load currents, linearity and errors of the test system itself, parasitic parameters introduced by the connection system, individual differences in products etc. In practice, a safe setting is often set with a margin of for example, 6 dB. The larger this value is, the greater the difference the system can tolerate when maintaining loop stability.

Phase margin: The phase angle at which the feedback signal advances the interference signal when crossing the frequency. If the phase of the compensated signal is too late, for example < -180°, the negative feedback will turn into positive feedback. To the left of the crossover frequency, the gain is greater than 0 dB. At this time, it is working as negative feedback. Ensuring that the phase margin is sufficient at the crossover frequency can ensure that this working negative feedback will not cause negative effects due to phase lag. The nature of feedback changes. In practice, the phase margin is generally required to be greater than 45°.

Efficiency

Efficiency is one of the most important indicators for evaluating product performance. Efficiency will lead to different distributions of product heat balance, and heat will in turn affect efficiency testing to a great extent. In order to obtain a stable and repeatable efficiency test result, The effect of heat needs to be minimized as much as possible by measuring the input current quickly.

Among the four factors of measurement efficiency, input voltage and output current can be stably controlled by measuring instruments; the stability of output voltage is the basic function of a PoL/VRM.

When testing the efficiency, set the proper range, accuracy and number of digits of the DVM measurement input current in advance, test the input current immediately after the module works, and ensure that the delay does not exceed 20 ms, so that the temperature inside the module does not rise before the input current value has been obtained. After measuring the input current value, the temperature value can be recorded via PMBUS at the same time as a reference. Next, the input voltage, output current, and output voltage are sampled and measured. These three values are not affected by temperature and efficiency, and finally the efficiency value is calculated.

Mechanical structure

When arranging structural parts such as heatsinks that will come into contact with the product, please note that the capacitors on the product cannot be touched by any material, otherwise stress may be introduced and cause component failure. The number of times our products can be reflowed is limited, please do not exceed the maximum limit in the specification.

Unless the product's datasheet indicates that the module can be installed upside down, please do not solder our products on the backside of the PCB through a reflow oven. Some heavy components may fall off due to remelting of the solder on the pins.

Products with plug-in pins can only be soldered by wave soldering. If this type of product is compatible with reflow soldering, we will indicate pin-in-paste in the product manual.

Layout

The signal +/- SENSE is susceptible to interference, so differential wiring needs to be used and kept away from components that generate electronic noise, such as MOSFETs and inductors. It is recommended to connect to the output's large-value capacitor pin.

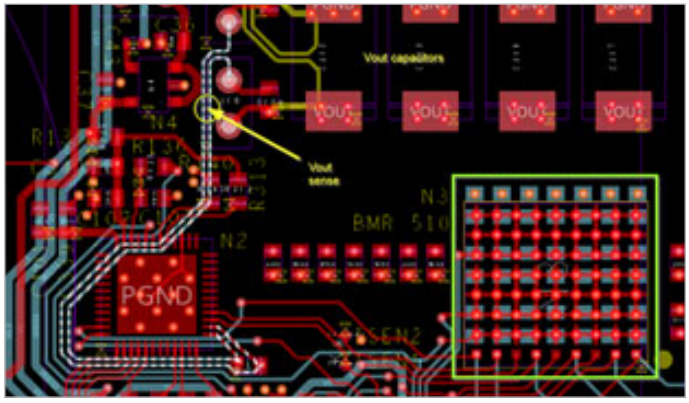


Figure 11: Layout recommendations

Grounding should take into account that the power ground and signal ground where large currents flow need to be separated. SDA, SCL, SALERT, IOUT, and TOUT are all reference signal ground. The signal ground should be away from radio frequency signal interference sources.

The large output capacitor should be placed close to the output pin of the module. Please pay attention to the appropriate withstand voltage value, capacitor type and capacitance value of the capacitor.

PoL/VRM often has multi-phase output in use, such as 16 or even 24 phases. In order to achieve higher efficiency at low power output, control ICs often temporarily turn off certain phases to reduce switching losses.

When turning on and off these phases, the natural numbering of the phases is generally followed. For example, in a 24-phase system, when the output is at half load on average, only phases 1 to 12 will work. In order to achieve heat balance at this time, it is recommended that when placing each phase, the phase that always works is placed on the path with the smallest resistance, and then the even-numbered phase modules are placed on one side, and the odd-numbered phase modules are placed on the other side.

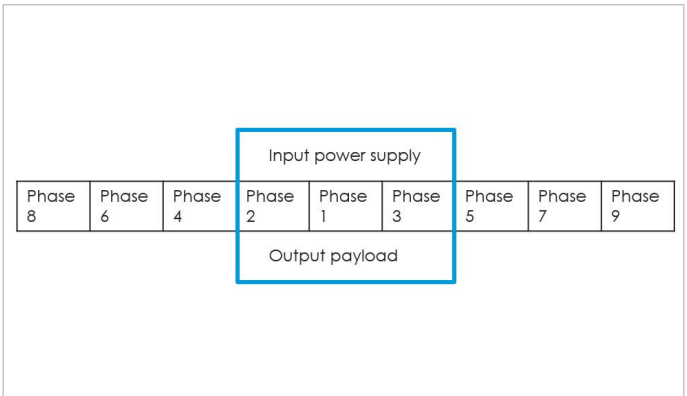


Figure 11: Physical arrangement: phase auto adding/removing

In this way, the shortest path of copper foil is always used during low power output, and the heat distribution is also symmetrical and uniform.

Recommended capacitors

SP-CAP capacitor has the following advantages:

- large capacitance (for example, 560 uF)
- small ESR (3 mΩ)
- small ESL (the three-terminal lead method is better)
- can withstand large ripple current (10.2A rms)
- RoHS compliant and halogen-free

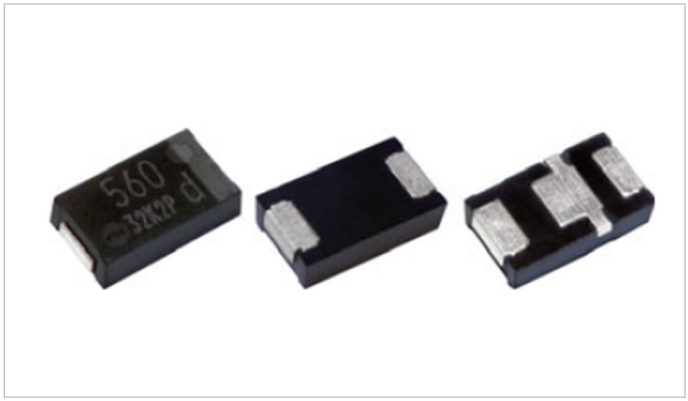


Figure 12: SP-CAP capacitors

OS -CON capacitors have the following advantages:

- large capacitance (e.g. 1000 uF)
- high voltage resistance (e.g. 50 V)
- high temperature resistance (125 °C 1000h)
- RoHS compliance and halogen-free

Figure 13: OS-CON capacitors

Test

When testing product performance, do not use series power supplies to increase the total output voltage to meet the minimum voltage requirement of the load, because series power supplies will introduce noise, affecting communication, efficiency, and output ripple and stability.

- POL/VRMs have very high OCP values, so you need to choose appropriate equipment to measure the OCP value.
- During product testing, in order to prevent OVP from being accidentally triggered, OVP should be set to a higher value.
- CTRL_PIN cannot be left empty
- Make sure each phase of the multi-phase output is functioning properly before applying heavy loads
- Confirm that loop parameters are stable
- Confirm that the capacitance, type and placement of the output capacitor meet the requirements
- Important weak signals such as TSENSE and ISENSE must not have interference

During the thermal test, because the object under test needs to be placed in a heating furnace (or an external liquid cooling pipe needs to be added), a longer connecting wire is required from the load. When the POL/VRM outputs low voltage and high current, the long connecting wire lead to voltage drop on the connecting line and may cause the voltage at the load end to be insufficient for the load to operate. In this case, a power supply can be connected in series with the output to boost the voltage. Please pay attention to the series connection sequence of the series power supply. It is necessary to ensure that the GND of the object under test, the power supply GND, and the load GND are at the same potential. Only in this way can make the communication between the PMBUS and the test equipment. In addition, it is necessary to consider that the OTP may be triggered during the thermal test and cause shutdown. At the moment of shutdown, the load is equivalent to a wire because it is set to high current mode. The output voltage of the series power supply is directly added to the output terminal of the module as a negative voltage. This will cause the module to be damaged. Therefore, when shutting down, be sure to turn off the load or series power supply first, and then turn off the module.

Heat dissipation

Convection and conduction are the two most common forms of heat dissipation in power modules. In terms of conduction, we often use pin forms such as LGA and BGA. On the one hand, using many distributed smaller current loops instead of a single large current loop can reduce electromagnetic interference. On the other hand, the consideration is to use a large number of pins that can dissipate heat through the power layer and ground layer of the PCB through conduction.

When choosing a product, please pay attention to the main heat dissipation method of the product. For example BMR510 and BMR511 have completely different heat dissipation structures. The power device of BMR510 is on the top. The main recommended heat dissipation method is to dissipate heat from the top of the module through a liquid cooling pipe system. The power device of BMR511 is on its own PCB. The top is an inductor, and the corresponding heat dissipation method is forced air cooling.

There is also an immersion liquid cooling method: the entire circuit board is placed in an insulating liquid. The heat generated by the product is transferred to this liquid. The boiling point of this liquid is very low, about 60°C, so it quickly vaporizes, and when it changes from liquid to gas, it releases a lot of heat. This kind of heat conversion relies on phase change phenomena and does not require an additional heat exchanger. It can be equivalent to a thermal conductor with very small thermal resistance, which is a very good thermal conductivity design. This kind of heat dissipation requires high investement since the entire system needs to be strictly sealed without leakage.

Power Modules

Flex Power Modules, a business line of Flex, is a leading manufacturer and solution provider of scalable DC/DC power converters primarily serving the data processing, communications, industrial and transportation markets. Offering a wide range of both isolated and non-isolated solutions, its digitally-enabled DC/DC converters include PMBus compatibility supported by the powerful Flex Power Designer.

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