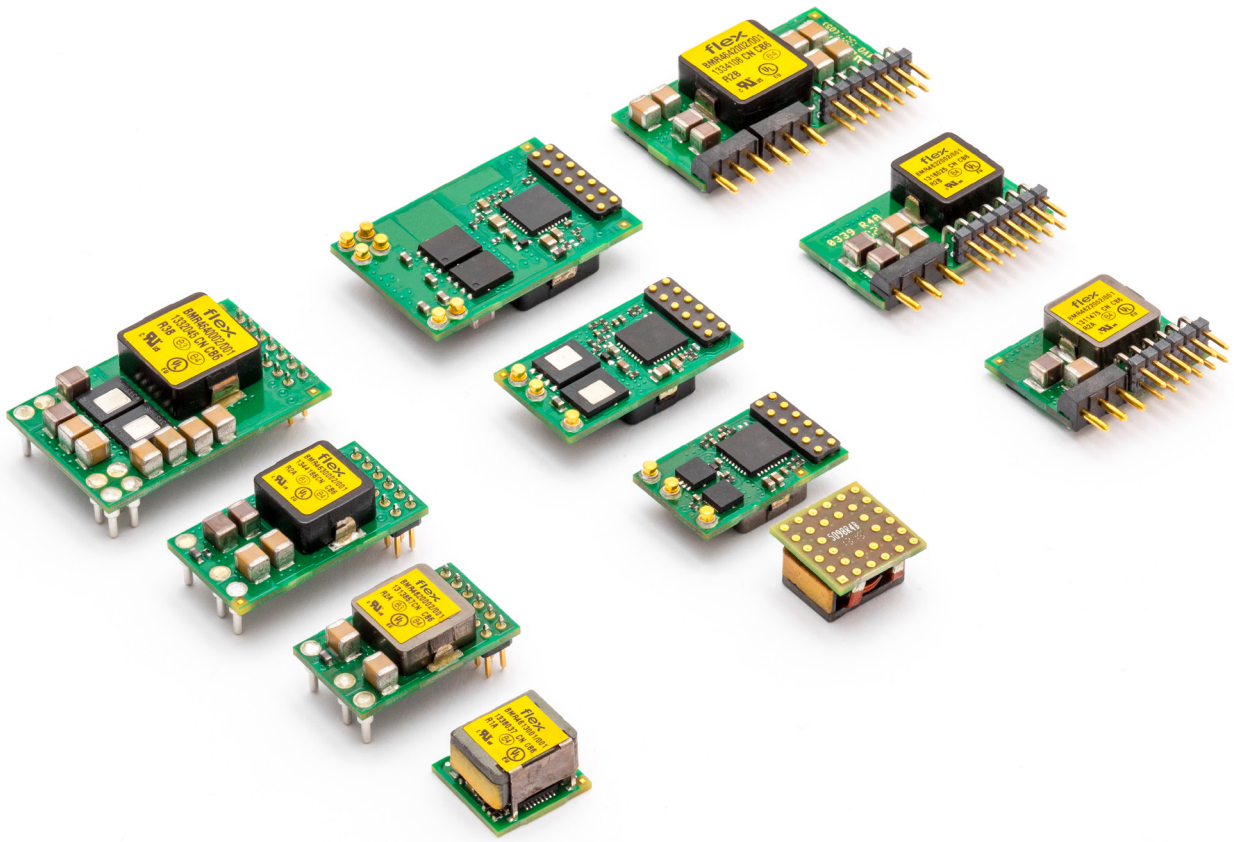
Application Note 309

Flex Power Modules



Synchronization and Phase Spreading - 3E POL Regulators

Abstract

The 3E Digital products can be configured, controlled and monitored through a digital serial interface using the PMBus™ power management protocol.

This application note provides information on how to synchronize the 3E POL regulators and use phase spreading for optimized performance.

This application note applies to the following products:
BMR450
BMR451
BMR461
BMR462
BMR463
BMR464

Introduction

In systems with multiple switching products, the switching phase between products may need a delay to reduce undesired effects in the system. These undesired effects include large peak current drawn from the input voltage and input capacitance and high levels of radiated emissions due to intentionally or unintentionally synchronized edges of the switching frequency. Phase spreading is a method of reducing these effects.

The simplest way of phase spreading is to allow the products to operate individually, from their own internally generated clock. This randomizes the occurrence of the switching frequency edges, which reduces the chances of high peak currents from the input source. However this method produces results that are not repeatable.

A more predictable and effective way of phase spreading involves distributing phase edges of each product in a group by operating them from a common switching clock. A single clock source is used for all products and each product has its phase set to a different value throughout the cycle of the clock. For example in a group of three products the phases can be set 360° / 3 = 120° from each other. This type of phase spreading reduces peak input current and input voltage ripple as well as reduces current stress to input capacitors. It also effectively reduces radiated emissions.

In this app note phase spreading is demonstrated using the Flex Power Designer software. The software is available for download at www.digitalpowerdesigner.com.

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Synchronized Clock Sourcing

Synchronization of products to a single clock source can be realized by one of two methods:

1. External single clock source. The common switching clock is sourced from an external clock source within the system. The SYNC pin of each product in the group is configured as an input. See illustration in Figure 1.

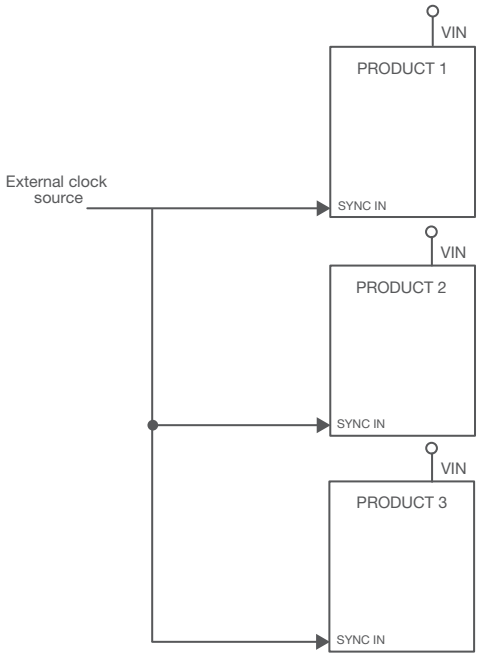


Figure 1. External single clock source.

2. Internal single clock source. One of the products in the group is configured to source the common switching clock by setting the SYNC pin to an output state. The SYNC pin of all other products in the group is configured as an input. See illustration in Figure 2.

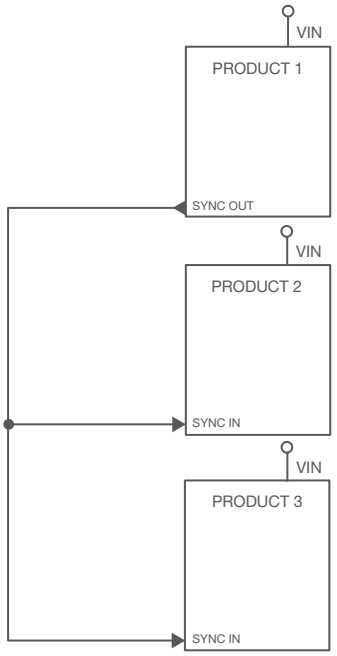


Figure 2. Internal single clock source.

Sync Pin Modes & Frequency

Depending on product, the SYNC pin can be set in different operational modes. The modes apply to the products according to Table 1.

SYNC Disabled

In sync disabled mode the product will use the internal oscillator, independently of the signal at the SYNC pin.

SYNC Input Auto Detect

In auto detect mode the product will automatically check for a clock signal on the SYNC pin when the product is enabled. If a clock signal is present, the internal oscillator will synchronize to it as described in section SYNC Input below. If no incoming clock signal is present or if SYNC is lost during operation, the internal oscillator will be used.

SYNC Input

The product will check for a clock signal on the SYNC pin each time the product is enabled. The internal oscillator will then synchronize with the external clock. The incoming clock must fulfill the frequency and performance requirements as specified in the Technical Specification of the product and must be stable when the product is enabled. In the event of a loss of the external clock signal, the output voltage may show transient over- and undershoots.

Note: If all products (connected to the same clock signal) are configured for SYNC Input and no external clock source is present, the output voltage of products will not ramp-up due to the lack of a clock signal for switching.

SYNC Output

The product will run from its internal oscillator and will drive the resulting internal oscillator signal onto the SYNC pin so that other products can synchronize to it. The signal drive can be either push/pull or open drain. The SYNC pin will not be checked for an incoming clock signal while in this mode.

Note: If more than one product (connected to the same clock signal) is configured for SYNC Output, the clock signal will become distorted, resulting in unstable output voltage of the products using the clock signal.

Setting SYNC Frequency

The SYNC pin's frequency, when configured in any of the modes above, should be set via the FREQUENCY_SWITCH command. This is the same command used by the Flex Power Designer software for its frequency setting commands. If an external clock signal is used (SYNC pin configured as input or auto-detect) the value of the FREQUENCY_SWITCH command should match the frequency of the applied external clock.
More information on the switching frequency's range can be found in the individual product's technical specification. The switching frequency should not be changed during operation.

Note: The switching frequency read back using the PMBus command READ_FREQUENCY could differ slightly from the set value due to hardware quantization error.

Note: Changing a product's default switching frequency will affect dynamic performance and therefore loop compensation and deadtime parameters may need to be adjusted. Changing the default switching frequency will also affect converter efficiency. These factors need to be considered when deciding whether to combine converters with significantly different default switching frequency to a single phase spreading group or use separate groups.

Product	SYNC Disabled	SYNC Input Auto Detect	SYNC Input	SYNC Output
BMR450, BMR451	Yes (default)	No	Yes	No
BMR461	No	Yes (default)	No	No
BMR462, BMR463, BMR464	Yes (default)	No	Yes	Yes

Table 1. Applicable SYNC pin modes.

Phase Spreading

Once the products are on a common clock line, the modules can have their clock phases spread.

Phase Offset

Assuming buck converters supplied from a common input supply, each converter is represented by a phase with a certain magnitude and duration in the switching period, as illustrated in Figure 3. The magnitude of the phase is the current drawn from the input supply, which approximately equals the output current of the rail. The duration of the phase as a fraction of the switching period equals the duty cycle of the rail, which in turn depends on the output voltage and actual efficiency of the converter.

To achieve a phase spread, each phase needs an offset as illustrated in Figure 3. The phase offset is defined as the time from the sync signal edge to the beginning of the phase duration (BMR450, 451, 462, 463, 464), or to the center of the phase duration (BMR461).

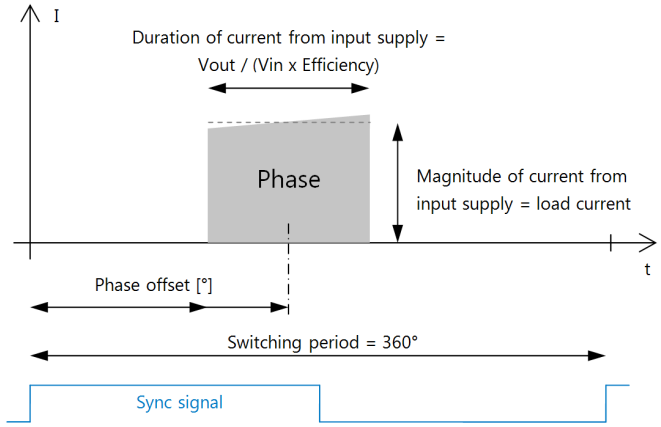


Figure 3. Phase current from input supply.

Offset Configuration

For non-current sharing rails, the phase offset is defined by the INTERLEAVE command by the Number In Group value (1-16) together with the Interleave Order value (0-15). The offset can be expressed in degrees or time according to the formulas below, where $T_{SW} = 1/F_{SW}$ is the switching period.

$$Offset(°) = 360 \times \frac{Interleave\_Order}{Number\_in\_group}$$

$$Offset(s) = T_{SW} \times \frac{Interleave\_Order}{Number\_in\_group}$$

For current sharing rails, the phase offset is defined by the sum of the offset given by the INTERLEAVE command and the formulas above, and the offset given by the automatic phase spread of current sharing units (see AN307). For example four modules operated in parallel are automatically given the phase offsets 0°, 90°, 180° and 270° due to the current sharing. Assigning an INTERLEAVE configuration that corresponds to 45° phase offset to each of these four modules yields the new final offsets 45°, 135°, 225° and 315°.

More details on the INTERLEAVE command can be found in *Appendix 1 - Sync Command Reference* or in AN302.

Offset Resolution

While the equations provide ideal phase offsets, the actual phase offset for the BMR450, BMR451, BMR462, BMR463 and BMR464 is limited to 16 possible values, in 22.5° steps as illustrated in Figure 4. The actual phase offset becomes the ideal calculated value rounded to the closest 22.5° step.

The BMR461 products support a higher offset resolution equivalent to 2.8° steps. Thus, the ideal calculated offset value is rounded to the closest 2.8° step.

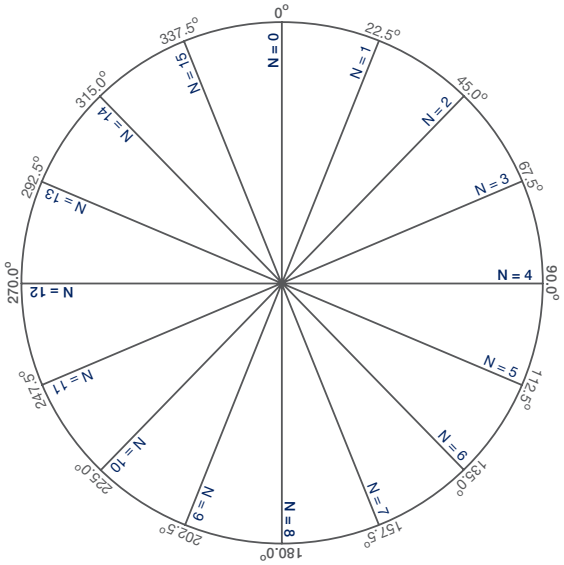


Figure 4. Offset resolution for BMR450, BMR451, BMR462, BMR463 and BMR464.

Example 1

In this example, assume three single-phase rails with a common SYNC clock, similar to Figure 2. Following the equations and using the values in Table 2, the ideal phase offsets can be calculated (also shown in Table 2). Then, by using the phase offset resolution wheel in Figure 4, we end up with our actual phase offsets.

Product	Number in Group	Interleave Order	Phase Offset (Ideal)		Phase Offset (Actual)
BMR462	3	0	0	0	0º
BMR463	3	1	120°	1/3 x T_{sw}	112.5°
BMR464	3	2	240°	2/3 x T_{sw}	247.5°

Table 2. Example 1 phase spreading calculations.

Note: The Number in Group value does not have to equal the actual number of phases. It is simply a parameter used to calculate the offset. In this example the phase offset 112.5° for the BMR463 could have been achieved just as well with Number in Group = 16 and Interleave Order = 5.

Synchronization With Flex Power Designer

Configuring synchronization is easy with Flex Power Designer (FPD), as it visualizes phase spreading across your power system. If you are not familiar with FPD, consult the FPD User Guide, which is in the FPD installation in the Start Menu > Flex Power Designer > Documents > User Guide.

Example Continued

Let us continue Example 1 with Flex Power Designer. This example can also be configured to hardware using a POL Design Board (ROA 128 3836) with a BMR462, 463, and 464 in the positions shown in Figure 5.

Since we want to have a shared SYNC clock, the jumpers in position 7 for each part must be inserted, and no jumper should be in positions 6 or 8. More jumper info can be found in the POL Design Board Technical Specification.
In FPD, create a power project with three rails. As shown in Figure 6, we use a BMR462, BMR463, and BMR464 with voltages of 1.0, 1.8, and 5.0V. Next, create a SYNC/Phase Spreading function in FPD and add all three rails that you just created. Now select the created function to show the phase spread configuration view.

The first thing we want to do is ensure that there is a common synchronization signal across the devices. As shown in Figure 7, we use the Syncronization settings to set the 1.0V rail to be the clock source, i.e. the SYNC pin of that device will be configured as output. Push/pull output is the recommended choice for most applications.
The other devices then will get their SYNC pins automatically configured as inputs. It is also possible to redefine the switching frequency or choose an external sync signal source.

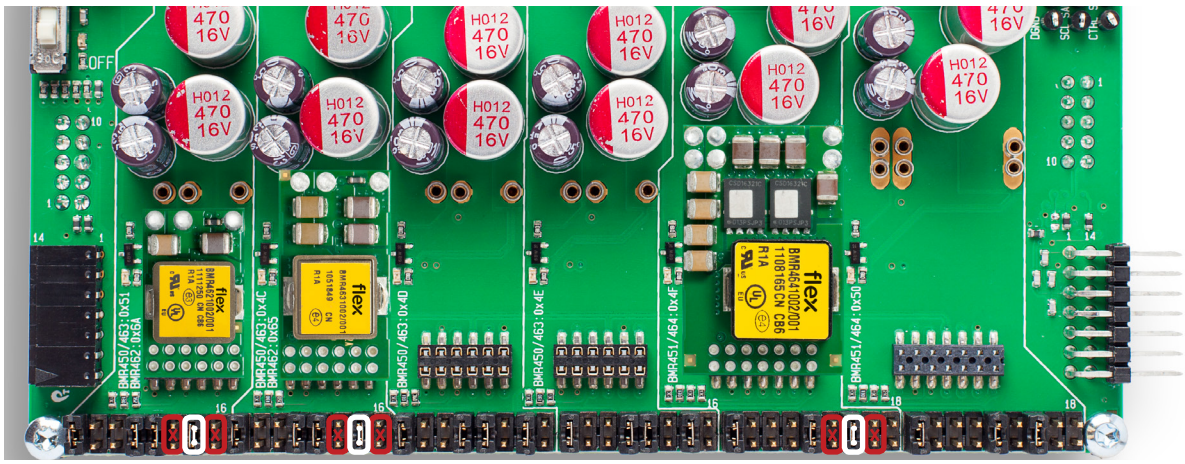


Figure 5. POL Design Board 128 3836.

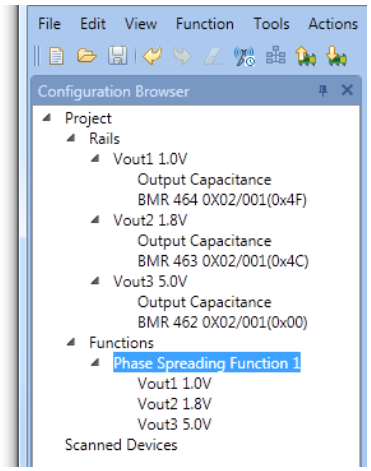


Figure 6 Rails and function setup in Flex Power Designer.

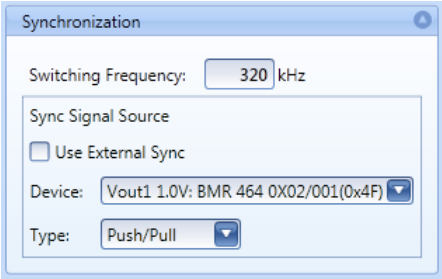
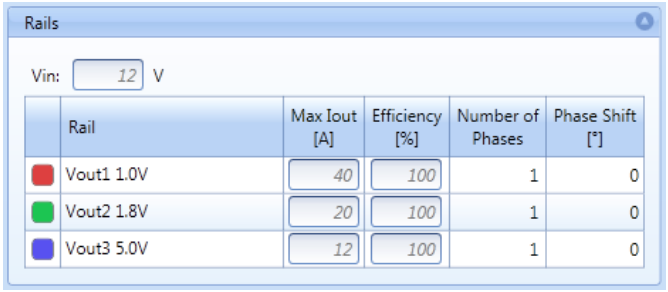


Figure 7. Configuring SYNC signal source. Vout1 is selected as sync out.

At this point, you have synchronized rails, but they draw current all at the same time - causing noise and uneven input current. To change this, we add phase spreading by configuring specific phase offsets for each rail. The phase offset for each rail is indicated in the right-most column of the Rails table as shown in Figure 8. The offset is zero for all rails by default.

Following the principle presented in Figure 3, as represented in Figure 9, the phase offset for each rail is graphically illustrated and their position visualized by colored blocks.



Rail	Max Iout [A]	Efficiency [%]	Number of Phases	Phase Shift [°]
Vout1 1.0V	40	100	1	0
Vout2 1.8V	20	100	1	0
Vout3 5.0V	12	100	1	0

Figure 8. Zero phase offsets by default.

To change the phase offset of a rail, simply left-click and drag the corresponding colored block to the desired phase offset position. In this case we distribute the phase offsets equally across the period, at 0°, 112.5° and 247.5° as in Table 2, see figure 9.

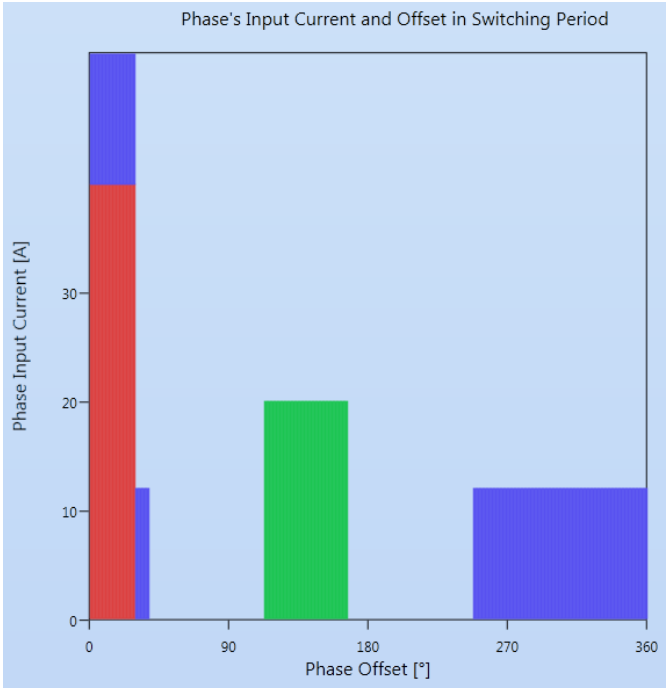


Figure 9. Configured phase offsets 0°, 112.5° and 247.5°.

Optimized Phase Spreading

The main purpose of phase spreading is to minimize the input current ripple, which in turn reduces stress on input capacitors and lowers radiated emissions. For many systems, due to different output voltage and load of the rails, the lowest input current ripple is not achieved by simply distributing the phases equally across the switching period as in the example above. There is a need to find an optimized phase spread.

Higher output current rails are typically of lower output voltage and will draw high input current during a relatively short period. Higher output voltage rails are typically of lower output current and will draw low input current during a relatively long period. See Figure 3.

Optimizing the phase spread is the task of distributing the different sized phases across the switching period in order to smooth out the current drawn from the input supply. Essentially this is a task of positioning the phases so to avoid or minimize the overlap of phases in

time.

Rails

Vin: 12 V

	Rail	Max Iout [A]	Efficiency [%]	Number of Phases	Phase Shift [°]
	Vout1 1.0V	35	87	1	0
	Vout2 1.8V	19	90	1	112.5
	Vout3 5.0V	7	85	1	247.5

Figure 10. Setup before optimizing phase spreading.

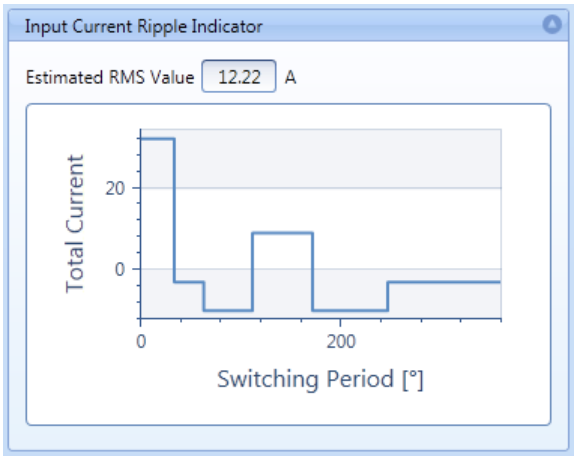


Figure 11. Input current ripple indicator.

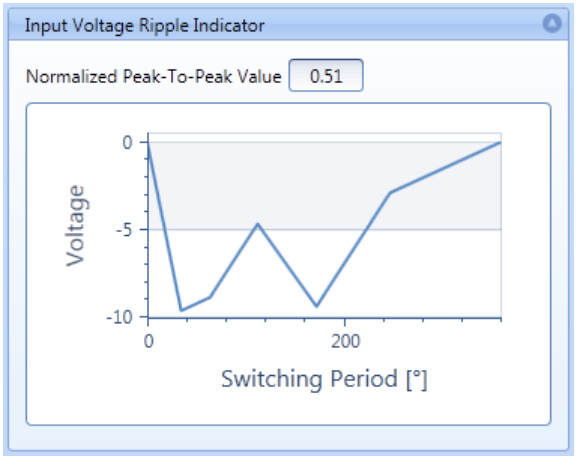


Figure 12. Input voltage ripple indicator.

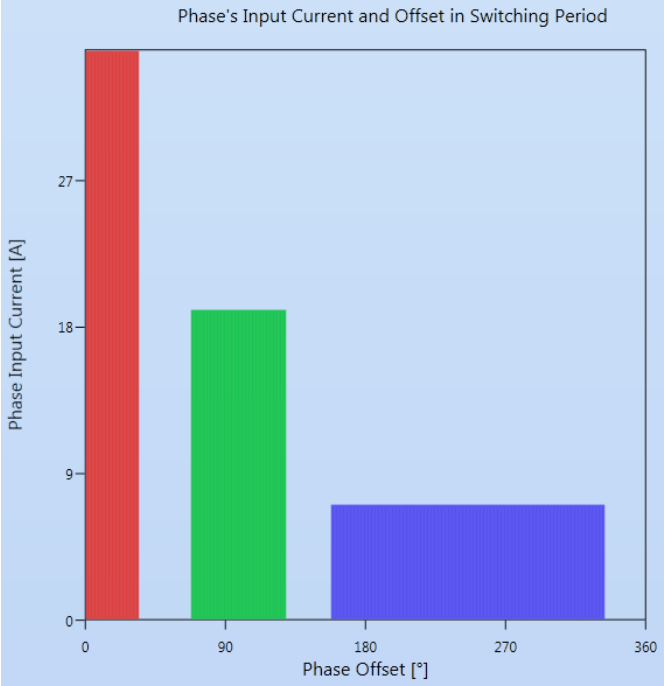


Figure 13. Spread with phase offsets 0°, 67.5° and 157.5°. Input current RMS value = 10.1A.

Optimized Phase Spreading with Flex Power Designer

Flex Power Designer (FPD) provides user friendly tools for both manual and automated optimized phase spreading.

Returning to Example 1 above, first we have to assign the input voltage of the system, Vin, and operating conditions of the rails, as shown in Figure 10.
In column Max Iout, enter the maximum anticipated load current of the rail. In column Efficiency, enter the worst case efficiency for the typical load range of the rail (such value can be collected from the Technical Specification of the applicable product).

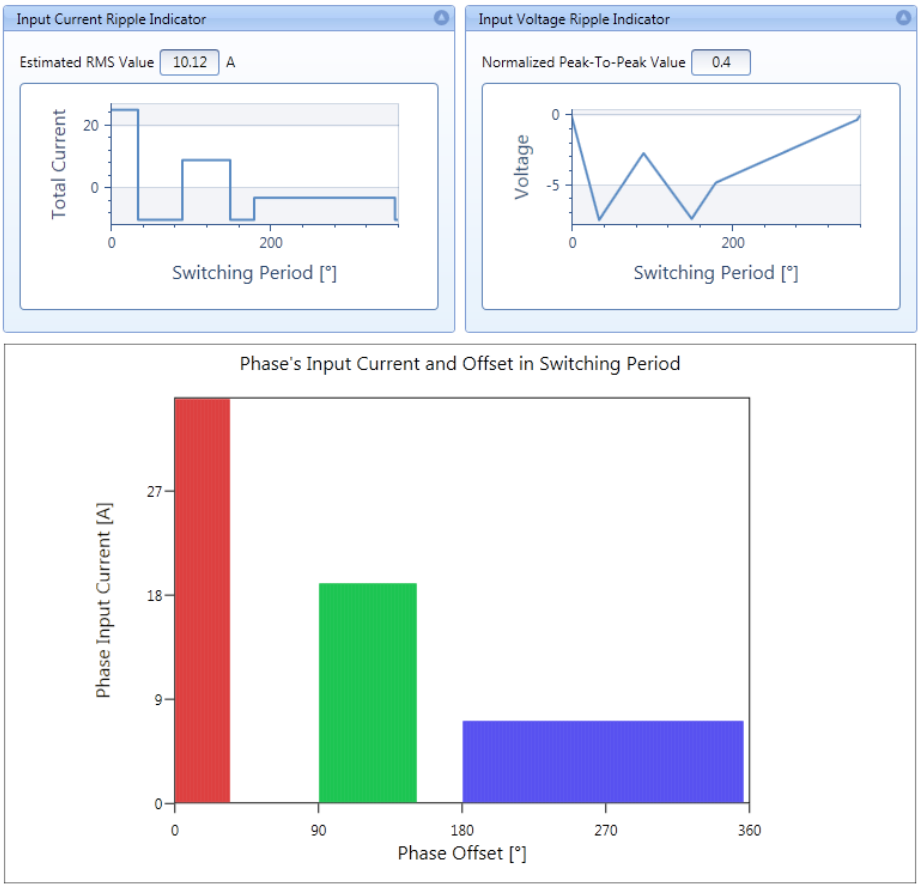


Figure 14. Automated spread with phase offsets 0°, 90° and 180°.

Before making the actual optimization, two helpful indicators in the phase spreading view of FPD are described in the next section.

Input Ripple Indicators

Pressing the “Result” expander in the upper right corner of the phase spreading view will display two indicators of the current phase spreading configuration, which give guidance when optimizing the phase spreading.

The Input Current Ripple Indicator, shown in Figure 11, provides an estimated RMS value of the total input current ripple of the rails, as well as a graphs showing the variation of the total input current along the switching period. The target is a minimized RMS value which means a smoothed-out input current.

The Input Voltage Ripple Indicator, shown in Figure 12, provides a normalized peak-to-peak value of the total input voltage ripple of the rails, as well as a graph showing the variation of the input voltage along the switching period. The normalized peak-to-peak value will be 1 in the case where all phases have zero phase offset. As offsets are introduced the peak-to-peak value will be reduced. The target is a minimized peak-to-peak value.

Note: Several simplifications are made in the calculations of the input voltage ripple values. Thus these values can not be used as estimates of the actual input voltage ripple, which for example depends on the amount and type of input capacitance used.
Rather, the input voltage ripple values are provided to aid the user in optimizing the spread of phases, by indicating if a change in the phase spreading configuration increases or decreases the input voltage ripple.

The Input Voltage Ripple Indicator graph is changed

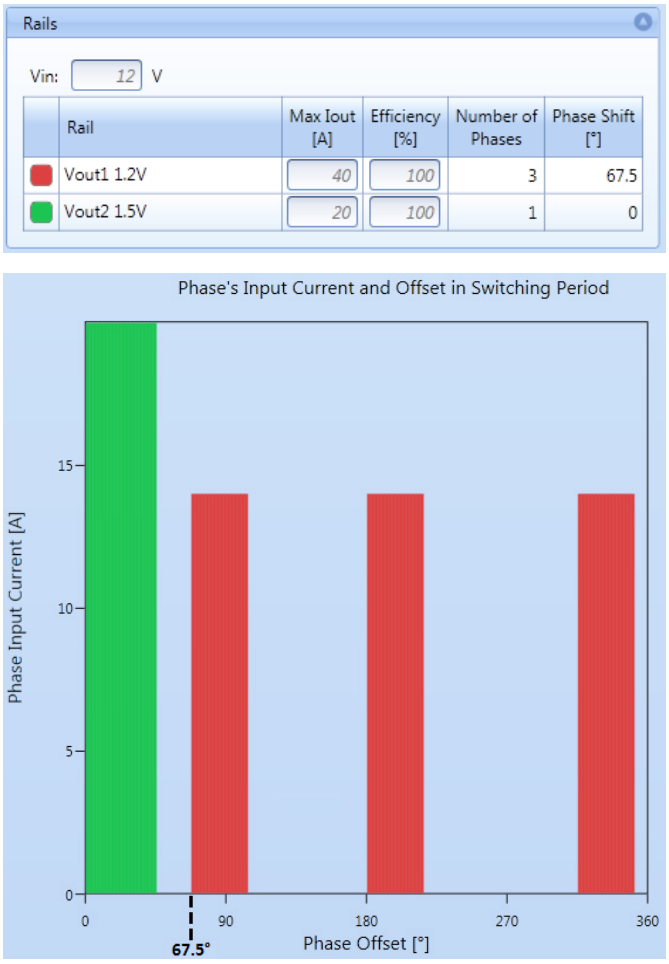


Figure 15 Current sharing rail with three phases and phase offset = 67.5° in the phase spreading view of Flex Power Designer.

somewhat but the normalized peak-to-peak value remains at 0.5.

It is recommended to use a minimized RMS input current ripple as the primary target for the optimization, and the peak-to-peak input voltage ripple as a secondary target.

Manual Optimization

The equally distributed offsets 0°, 112.5° and 247.5° configured in our example above gives input ripple indicator values according to Figures 11 and 12. With the chosen phase offsets in Figure 9 there is an overlap of the 1.0V and 5.0V phases.

By left-click and drag these phases to new phase offsets 67.5° and 157.5°, as in Figure 13, the overlap of the phases is avoided. The input current RMS value is then reduced from 12.2A to 10.1A, as can be seen in the Input Current Ripple Indicator.

Automated Optimization

For more complex systems with current sharing rails or a larger amount of rails, finding the optimized phase offsets manually may not be an easy task. With a single click on the Optimize button, Flex Power Designer will automatically find an optimized configuration of phase offsets.

Trying this on our example, we achieve a spread with the same input current RMS value as in our manual optimization, but with a lower peak-to-peak input voltage ripple, see Figure 14. The increased offset difference between the higher current 1.0V and 1.8V

rails affects the input voltage waveform so that the normalized peak-to-peak value is reduced from 0.5 to 0.4.

Phase Spreading made Simple

This phase spreading example only took a few steps, because FPD takes care of automatically calculating and setting the low-level command values. You can see which commands have been automatically set by either going to the registers tab, or by going to the Export menu and previewing the commands sent to the phase spreading group. More information on what these commands mean can be found in *Appendix 1 - Sync Command Reference* as well as AN302.

Phase Spreading with Current Sharing Rails

The instructions for FPD provided above can be applied also when parallel rails are used. The difference is that a parallel rail will have several phases with a fixed offset between those phases. For example a parallel rail with two phases will always have 180° offset between the phases.

Each phase within a current sharing rail ideally has the same duration. The magnitude of each phase will be approximately the load current divided by the number of phases. See AN307 for more details on current sharing rails.

In the phase spreading view of FPD the phases of current sharing rails are displayed with the same color, as shown in Figure 15. When any of those phases are selected and dragged, all those phases will move along, without changing the fixed offset between the individual phases. The phase offset indicated in the Rails table is the offset to the first phase of the current sharing rail.

Appendix 1 - Sync Command Reference

Behind the scenes, Flex Power Designer uses PMBus commands to setup Clock Synchronization and Phase spreading.

Sync Pin Mode Commands

For the BMR450, BMR451, BMR462, BMR463 and BMR464 products the SYNC mode is configured through the PMBus commands MFR_CONFIG and USER_CONFIG according to Table 3. See AN302 for details on these commands.

The SYNC pin of the BMR461 products is always in Input Auto-Detect mode and cannot be reconfigured (see Table 1).

To use synchronization with the BMR450/451 products the POL_ADJ_CONFIG command must be set to 0x00 in order to define the FLEX pin as a SYNC pin. Otherwise the internal oscillator will always be used and the bits in USER_CONFIG and MFR_CONFIG have no effect. When defined as a SYNC pin the FLEX pin can no longer be used for voltage adjust.

Sync Output at Disable

If SYNC pin is configured as Output (Push/Pull or Open Drain) it is possible to control the behaviour of the SYNC output during disable, through bit 11 (Sync Timeout Enable) in USER_CONFIG, see Table 4.

Note: The setting of bit 11 in USER_CONFIG has no effect when Precise Ramp-Up Delay is activated (MISC_CONFIG[7] = 0, which is the deafult setting) for applicable BMR462, BMR463 or BMR464 products. In that case SYNC output always remains on after output is disabled.

SYNC pin configuration	USER_CONFIG		MFR_CONFIG
	Bit 6	Bit 5	Bit 0
SYNC Disabled (default)	0	0	N/A
SYNC Input	1	0	N/A
SYNC Output Push/Pull	0	1	1
SYNC Output Open Drain	0	1	0

Table 3. SYNC mode configuration for BMR450, BMR451, BMR462, BMR463 and BMR464.

USER_CONFIG Bit 11	Function
0 (default)	SYNC pin output remains on after output is disabled
1	SYNC pin output remains on for 500ms after output is disabled

Table 4. SYNC output at disable for BMR450, BMR451, BMR462, BMR463 and BMR464.

Phase Spreading Commands

Phase spreading is done via the INTERLEAVE command, whose bitfields are shown in Table 5 below.

The Group ID Number can be used to assign different ID numbers if there are several phase spreading groups. However the Group ID Number has no impact on the phase offset.

The Number in Group and Position in Group values defines the set degree phase offset according to the equation below, where Interleave_Order = Position in Group

$$Offset(^\circ) = 360 \times \frac{Interleave\_Order}{Number\_in\_group}$$

Note: When using the INTERLEAVE command for modules that are operated in parallel (current sharing) all modules within the same parallel group must be assigned the same INTERLEAVE settings. The phase offset defined by the INTERLEAVE settings is added to the offset set automatically due to the parallel setup. (see AN307).

Bits	Purpose	Value	Description
15:12	Reserved	0	Reserved
11:8	Group Number	0 to 15	Sets a number to a group of interleaved rails
7:4	Number in Group	16, 1 to 15 (0 = 16)	Sets the number of rails in the group A value of 0 is interpreted as 16
3:0	Position in Group = Interleave Order	0 to 15	Sets position of the device's rail within the group

Table 5. INTERLEAVE command bitfields.

Formed in the late seventies, Flex Power Modules is a division of Flex that primarily designs and manufactures isolated DC/DC converters and non-isolated voltage products such as point-of-load units ranging in output power from 1 W to 700 W. The products are aimed at (but not limited to) the new generation of ICT (information and communication technology) equipment where systems' architects are designing boards for optimized control and reduced power consumption.

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APPLICATION NOTE
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