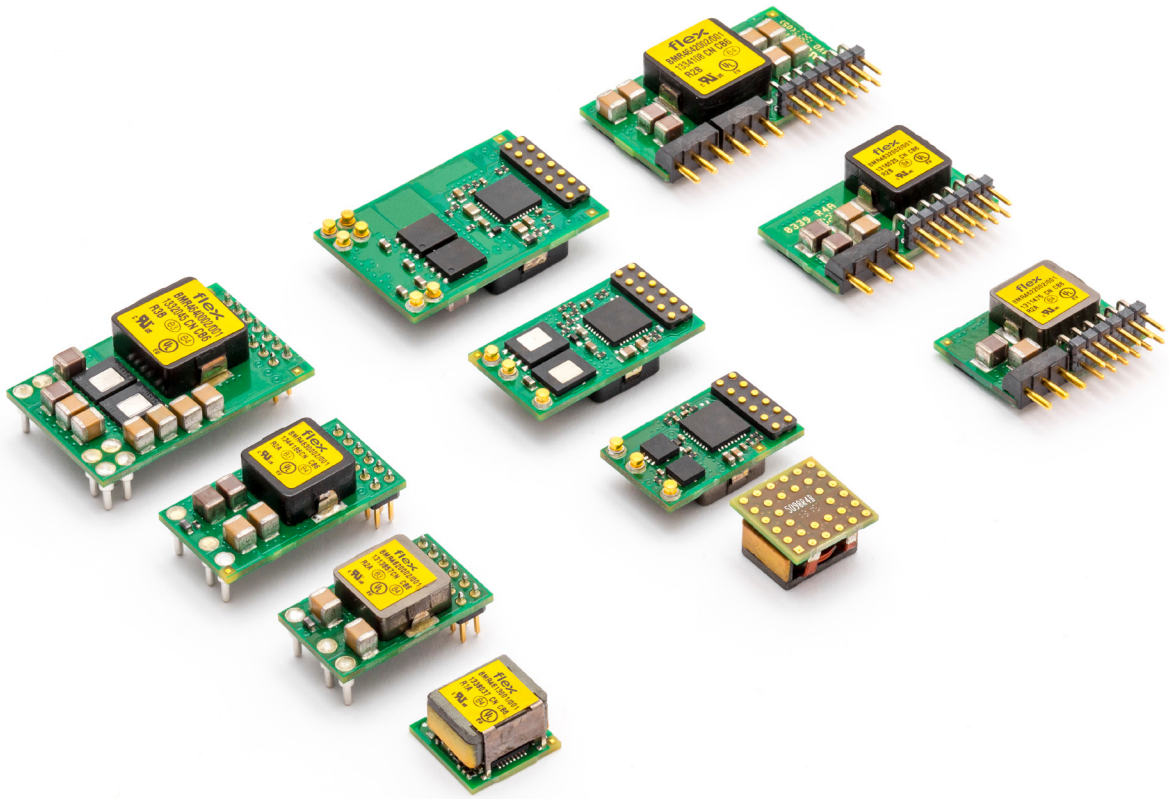
Application Note 310

Flex Power Modules



Sequencing Configuration – 3E POL Regulators

Abstract

The 3E Digital products can be configured, controlled and monitored through a digital serial interface using the PMBus™ power management protocol.

This application note provides information on different methods for sequencing of the 3E POL regulators.

This application note applies to the following products:
BMR 450/451 (no GCB based sequencing)
BMR 462/463/464/465/466 (GCB based sequencing)
BMR 461 (no GCB based sequencing)

Introduction

3E Series Point of Load Regulators utilize Digital Control and provide a lot of flexibility for implementing different sequencing schemes which can be set using Flex Power Designer Software or directly through PMBus/I2C.

The 3E POL Regulators, can be configured for sequencing in four different ways.

Time based sequencing

Time based sequencing uses the delay between appearance of enable signal and the moment the POL is turned on. All POLs get their enable signal at the same time. Once the delay time has elapsed, the output will start a ramp up. The delay and ramp times, set via PMBus for each POL, determines the sequencing order.

Event based sequencing

Event based sequencing is where the power-good signal of one POL is routed to the CTRL pin of the next POL in sequence. Thus, the sequence order is established in hardware, but rise/fall times and delays can still be changed over PMBus.

GCB based digital sequencing

GCB (Global Communication Bus) provides flexibility in the sequencing order and timing without hardware changes. GCB sequencing uses a single-wire digital bus that is commonly connected to all POLs. Sequence order, rise/fall times, and delays are all changed over PMBus. GCB sequencing is available on the BMR462, 463, 464, 465, and BMR 466.

Voltage Tracking

The last option, voltage tracking, allows to use one POL's voltage as a reference with other POL(s) following its turn-on and turn-off behavior in the tracking sequencing group. This requires connecting the output voltage of the reference POL (or from other source) to the VTRK pins of the tracking POL(s).

A system of POLs can include groups of all four sequencing methods. In this application note each sequencing configuration method is described, along with examples showing how to set up each method using the Flex Power Designer software. The software is available for download at www.digitalpowerdesigner.com.

The accuracy of timing settings are determined by the individual products. One may need to adjust timing based on the product's Technical Specification.

Contents

Method One - Time Based Sequencing

Overview

Time based sequencing allows supply output ramp-up and ramp-down sequencing based on the programmed soft start delay times. The CTRL pins for all products in the sequencing group are tied together. This requires that the ON_OFF_CONFIG register is set to 0x16 (for CTRL set to active high, and enable down-sequencing (i.e. turn-off) timings) or the default of 0x17 if down-sequencing is not needed. The start-up and shut-down sequence is determined by the soft start/stop delay settings.

Figure 1 shows three products prepared for time based sequencing.

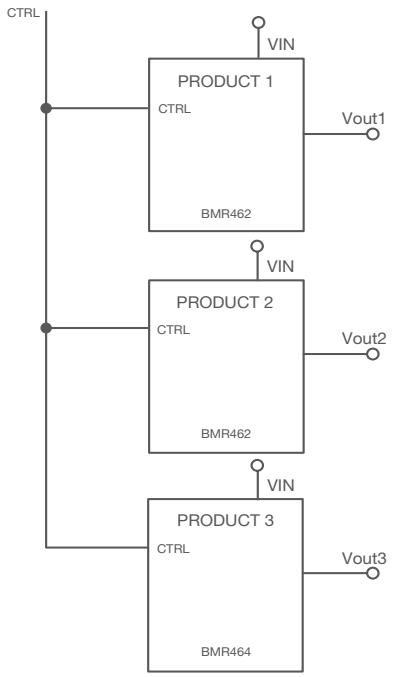


Figure 1. Time based sequencing example.

The configuration procedure for time based sequencing is straightforward. It only includes configurations of four registers, TON_DELAY, TON_RISE, TOFF_DELAY, and TOFF_FALL for all products/rails in the sequencing group.

The accuracy of the timing is defined by the accuracy of the delay and ramping timing and is specified in the product's Technical Specification. If using certain BMR 462, 463, or 464 as a standalone rail (i.e., non-current sharing), precise timing can enabled. More information on the products supporting precise timing and can be found in Appendix 1: Note on Precise Timing.

Example 1

Table 1 and 2 describe a time based up-sequencing (i.e. turn-on) configuration and down-sequencing of three rails.

	Delay [ms] TON_DELAY	Rise [ms] TON_RISE
Vout1_2.5V	10	20
Vout2_1.2V	10	10
Vout3_1.0V	15	30

Table 1. Time based up-sequencing (turn-on) example with three output rails.

	Delay [ms] TOFF_DELAY	Fall [ms] TOFF_FALL
Vout1_2.5V	10	30
Vout2_1.2V	10	10
Vout3_1.0V	10	30

Table 2. Time based down-sequencing (turn-off) example with three output rails.

While this example uses a tied CTRL pin, the PMBus OPERATION may be used by sending OPERATION to every device in the time sequence group using the Group Command Protocol. Using the Group Command Protocol lets you emulate a tied together CTRL pin by synchronizing command writes. Please note that doing sequencing this way requires that the ON_OFF_CONFIG register is set to 0x1A (PMBus control). More information on the Group Command Protocol is described in the PMBus Specification Part I, rev 1.2, Sec 5.2.3.

Configuring Time Based Sequencing With Flex Power Designer

Adding time-based sequencing with the Flex Power Designer (FPD) software is simple and aids in visualizing ramp-up and ramp-down timing. If you're not familiar with FPD, consult the FPD User Guide, which is in the FPD installation in the Start Menu > Flex Power Designer > Documents > User Guide.

This example can be configured to actual hardware, using a 3E POL Design Board (ROA 128 3836) with a BMR462, 463, and 464 in the positions shown in Figure 2.

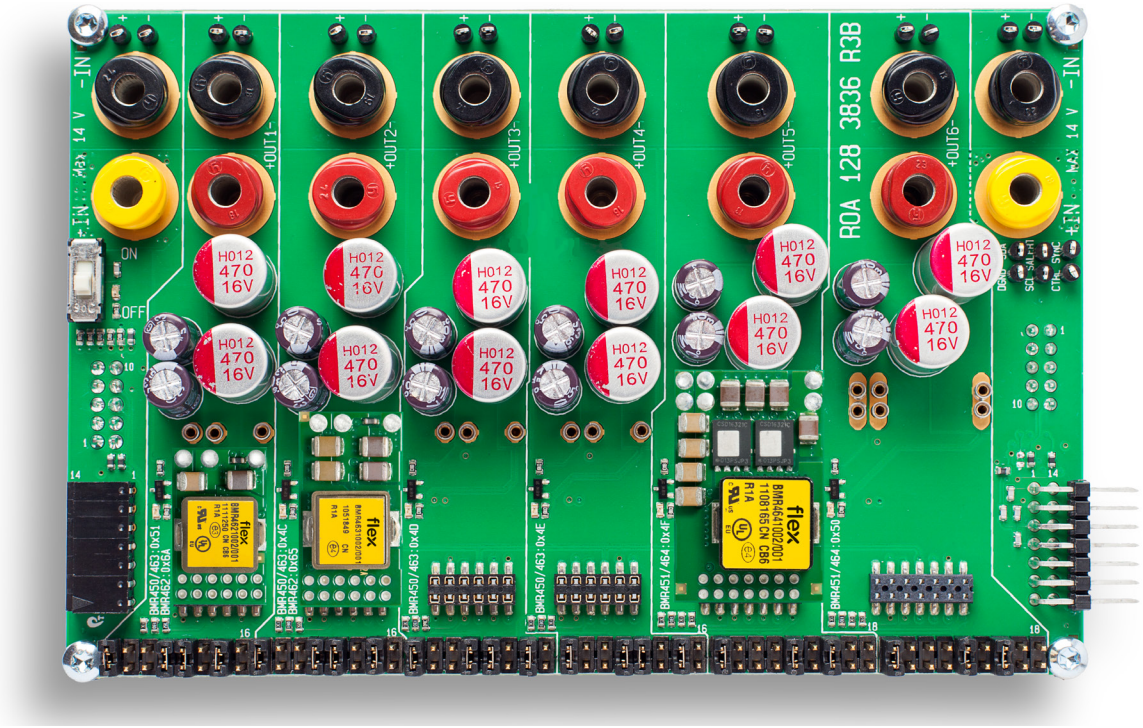


Figure 2. Example 1 implemented on 3E POL Test Board.

To start, let's create three rails in FPD. As shown in Figure 3, we use a BMR462, BMR463, and BMR464 with voltages of 1.0, 1.2, and 2.5V - similar to the timings in Example 1.

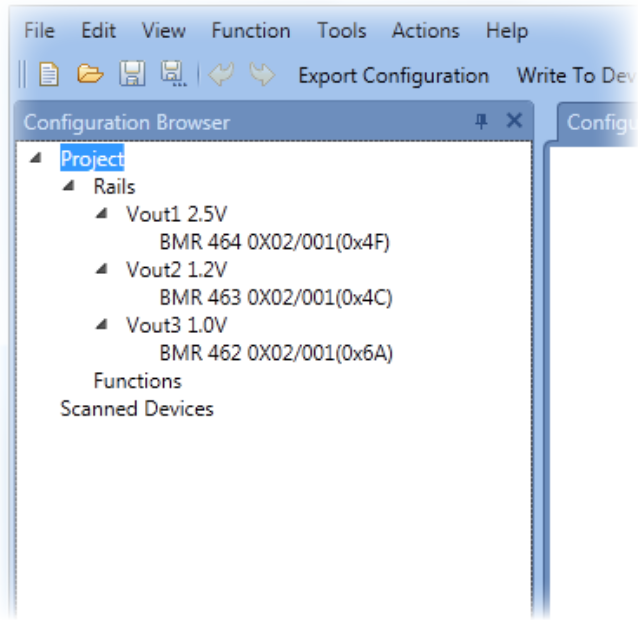


Figure 3. Rails from Example 1 in Flex Power Designer.

Next, add a time-based sequencing function by right-clicking the "Functions" item in the Configuration Browser. Then click "Add Time Based Sequencing", as shown in Figure 4.

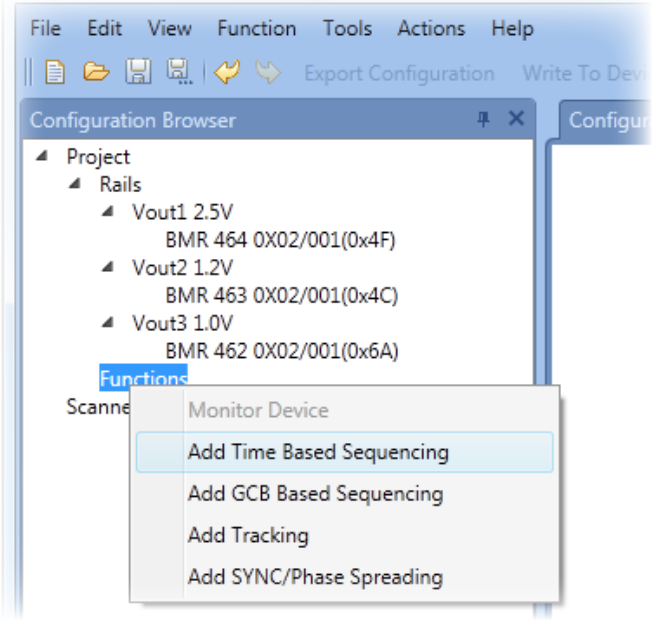


Figure 4. Adding Time Based Sequencing.

After adding the function, add rails to be sequenced by right-clicking on the “Time Based Sequencing Function” and selecting “Add/Remove Rails”, shown in Figure 5. This will create a pop-up menu to select which rails you want to be included in the sequencing group.

After doing this, you should now be able to see the sequencing timing diagrams, and set the desired timings. See Figure 6 & 7 for timing settings used in Example 1.

To get the best timing accuracy out of the rails, precise timing can be enabled in certain BMR 462/463/464/466 products. By default, precise timing is enabled whenever this feature is supported (see Appendix A for further details on precise timing)

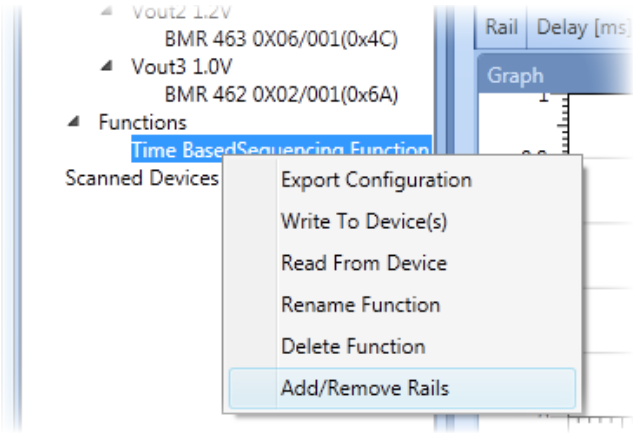


Figure 5. Adding Rails to the Sequencing Function.

	Rail	Delay [ms]	Rise [ms]
	Vout1 2.5V	10	20
	Vout2 1.2V	10	10
	Vout3 1.0V	15	30

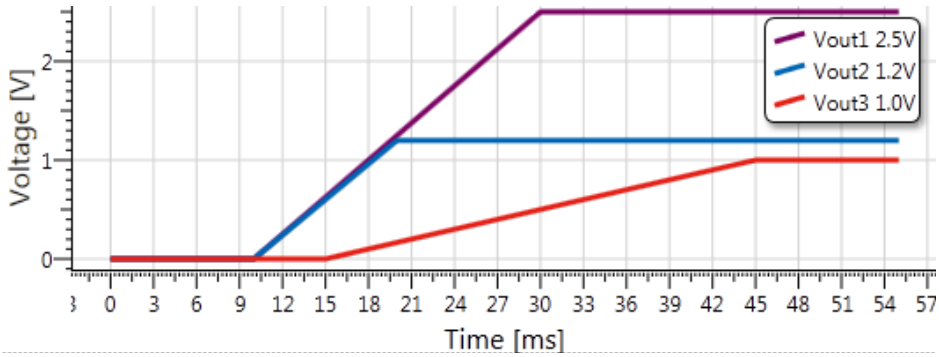


Figure 6. Example 1 Power-Up Sequence Timing.

	Rail	Delay [ms]	Fall [ms]
	Vout1 2.5V	10	30
	Vout2 1.2V	10	10
	Vout3 1.0V	10	30

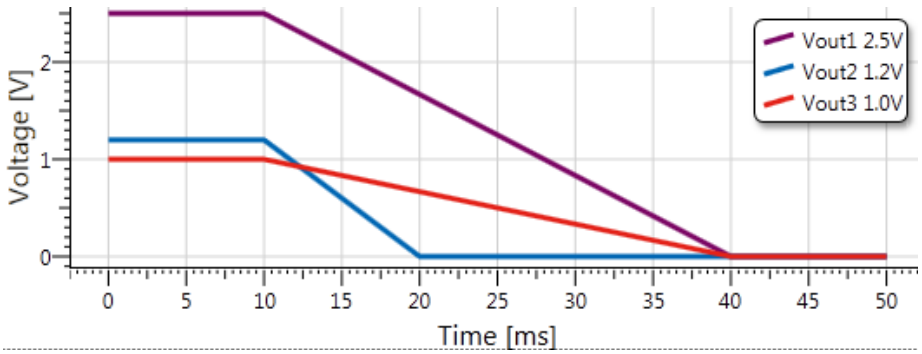


Figure 7. Example 1 Power-Down Sequence Timing.

Method Two – Event Based Sequencing

Overview

Event based sequencing of power rails is a method of sequencing where the output of one rail provides the signal to start another rail. In event based sequencing the power good (PG) signal from one product is tied to the enable pin (CTRL) of the next product and is repeated throughout the sequence.

Using the Event based method, i.e. connecting PG to CTRL, as shown in Figure 8, the same order for start-up and shut-down are provided. Unlike the GCB-based sequencing method, this method requires a hardware modification if the sequence order is changed.

Example 2

Tables 3 and 4 describe an event based up-sequencing configuration and down-sequencing of three rails. The settings are similar to Example 1, but the resulting start-up and shut-down waveforms will be different due to event-based sequencing

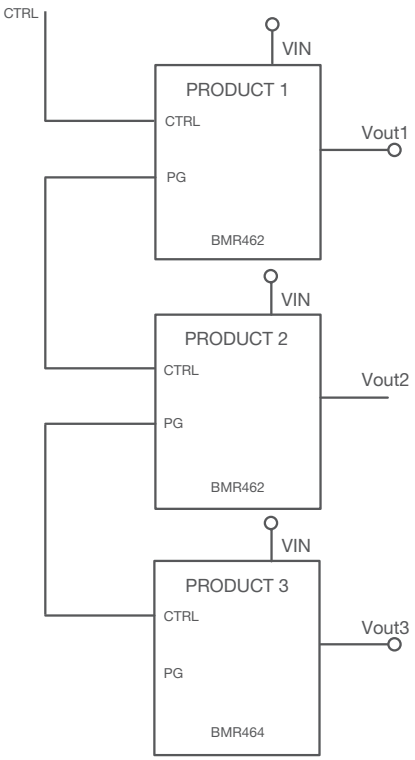


Figure 8 Event based sequencing example. A change of sequencing order will require a hardware re-configuration.

	Delay [ms] TON_DELAY	Rise [ms] TON_RISE	Power Good On [V] POWER_GOOD_ON	Power Good Delay [ms] POWER_GOOD_DELAY
Vout1_2.5V	10	20	2.40 V	20
Vout2_1.2V	10	10	1.15 V	10
Vout3_1.0V	15	30	1.15 V	10

Table 3. Event based sequencing power-up example timings. These can to be entered in Flex Power Designer via the rail configuration tab.

	Delay [ms] TOFF_DELAY	Rise [ms] TOFF_FALL	Power Good Off [V] POWER_GOOD_OFF*
Vout1_2.5V	10	30	2.30 V
Vout2_1.2V	10	10	1.05 V
Vout3_1.0V	10	30	0.85 V

Table 4. Event based sequencing shut-down example timings. These can to be entered in Flex Power Designer via the rail configuration tab.

* The threshold for down-sequencing is controlled.by POWER_GOOD_OFF if this command is supported, otherwise VOUT_UV_FAULT_LIMIT is used.

Event Based Sequencing In Action

The effect of different settings in the products generating, are illustrated in Figure 9a-b. Note that the up-sequencing parts as described in Figure 9a are valid for both Event and GCB based sequencing.

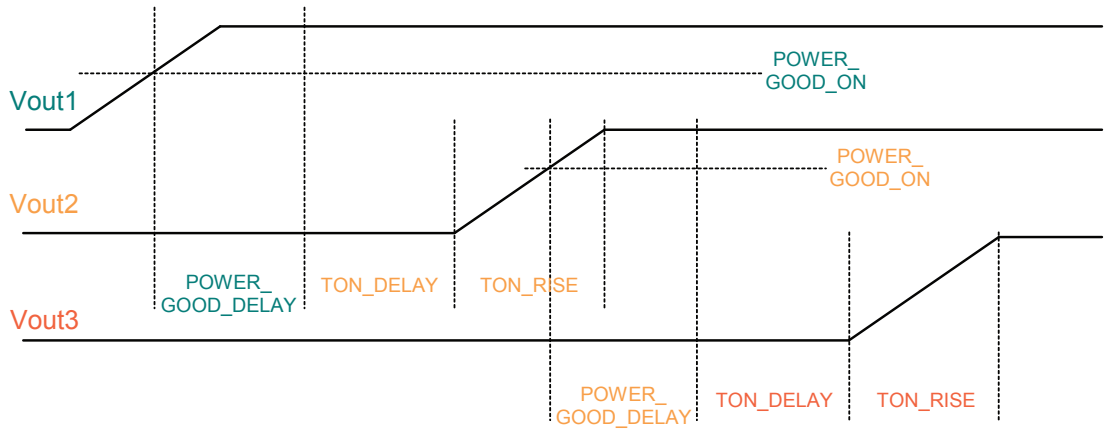


Fig 9a GCB and Event based up-sequencing – Illustration of which settings to be made in which rail. The total time between the Preceding rail, Vout1, and the following rail, Vout2, is determined as follows: Vout1 is configured using POWER_GOOD_ON and POWER_GOOD_ DELAY while Vout2 is configured using TON_DELAY and TON_RISE

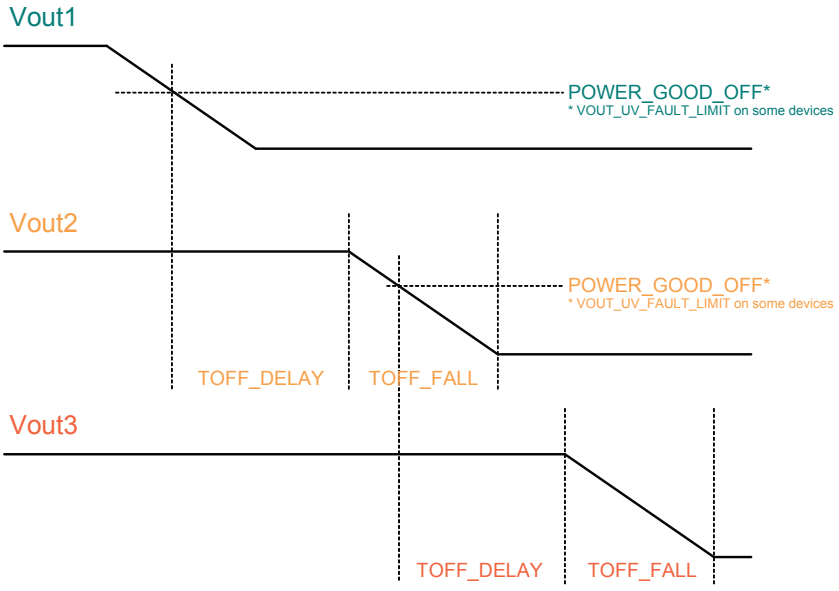


Fig 9b Event based down-sequencing – Illustration of which settings to be made in which rail. The total time between the Preceding rail, Vout1, and the following rail, Vout2, is determined as follows: Vout1 are configured using POWER_GOOD_OFF (or VOUT_UV_FAULT_LIMIT) while Vout2 is configured using TOFF_DELAY and TOFF_FALL.

Method Three – GCB Based Sequencing

Overview

As described earlier, the GCB based and Event based sequencing of power rails are both methods of sequencing where the output of one rail provides the signal to start another rail. While event based sequencing's signalling is done via chaining together PG and CTRL pins, GCB based sequencing works by using the General Communications Bus (GCB) and allows to change the sequencing order without any hardware changes..

Figure 10 illustrates the GCB Based Sequencing method. As shown, the devices use the GCB bus to communicate power good and power down events. This provides a higher level of flexibility in that the sequence order can be changed via PMBus configuration.

Enabling of up- and down-sequencing can be generated via the CTRL pin or using the PMBus OPERATION command. The products must physically be wired together on the same GCB bus.

About the General Communications Bus (GCB)

Several of the Flex Power Modules 3E products utilize a dedicated serial bus (the GCB bus) to synchronize and communicate real-time events. Addressing rails across the GCB is done with a 5 bit GCB ID, yielding a total of 32 rails that can be be shared with a single GCB bus. Ensure that the GCB signal integrity is maintained when using a large product count.

During GCB events, all products will receive messages; however, only those products configured to respond will do so. GCB products can also transmit events if their programmed algorithm requires inter module communication. Some examples include fault spreading, sequencing, phase add/drop, broadcast margin and broadcast enable.

Multiple sequencing groups can communicate and connect to the same GCB bus.

Example 3 - Configuring GCB Based Sequencing with Flex Power Designer

This example is similar to the earlier Time-based sequencing Example 1, which used a BMR462, 463, and 464. This time we'll have the same devices but use GCB based sequencing. First, we start again with creating our three rails, as shown in Figure 11.

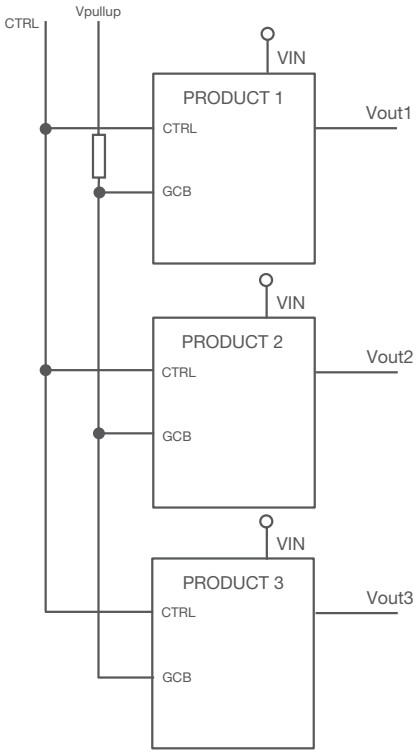


Figure 10 GCB Based Sequencing example – Enabling is shown generated via CTRL pin, but can also be done without a common CTRL by using PMBus OPERATION command.

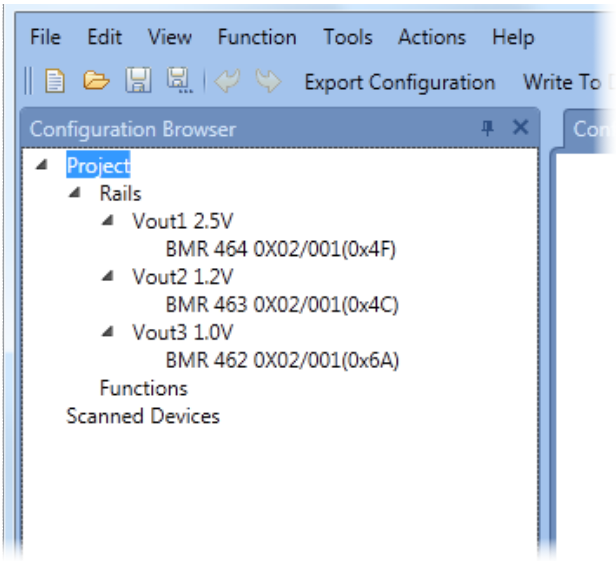


Figure 11. Rails for Example 3 in Flex Power Designer. Without any sequencing added yet, this is the same Rail setup as in Example 1

Then in the functions item right-click and add GCB Based Sequencing.

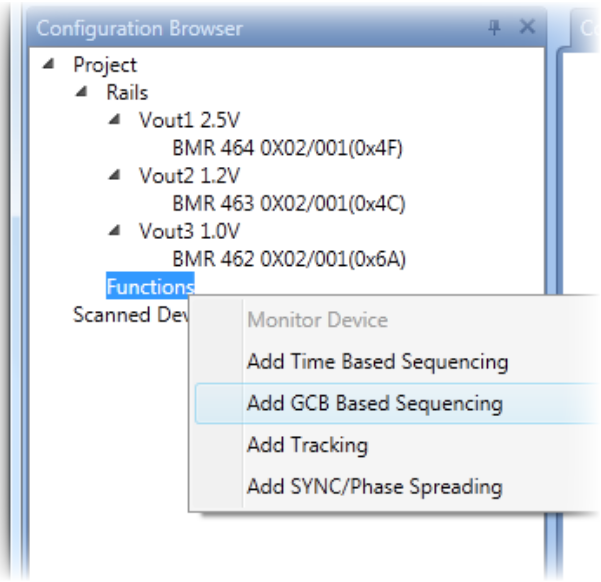


Figure 12. Adding GCB Based Sequencing

Finally add your rails again by right clicking the GCB Based Sequencing Function and selecting Add/Remove Rails.

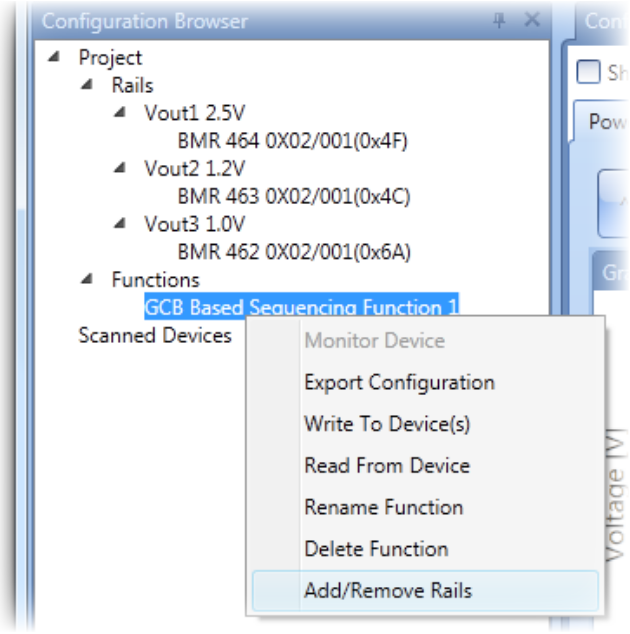


Figure 13. Adding GCB Based Sequencing

Now you can set timings and more importantly, re-arrange sequencing order without any hardware changes.

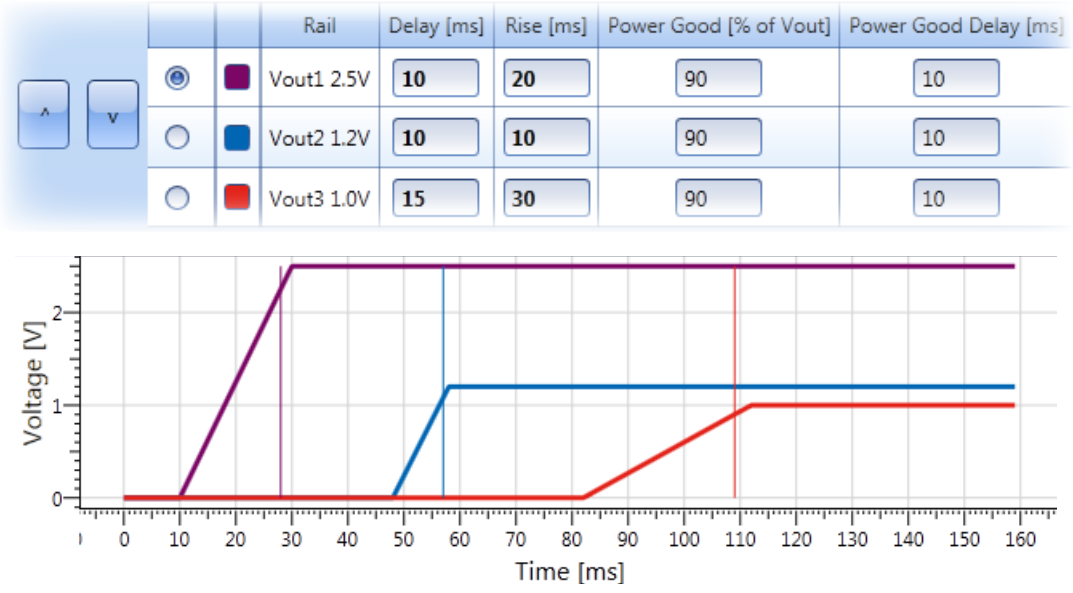


Figure 14a. GCB Based Power-Up Sequencing. There arrow buttons allow one to change the sequencing order.

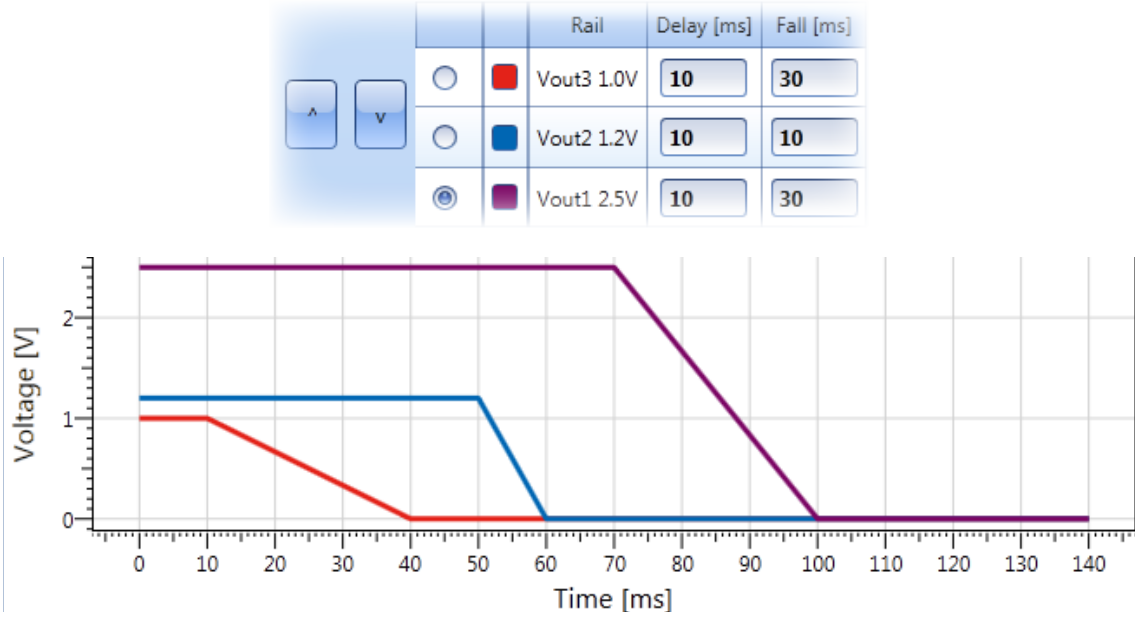


Figure 14b. GCB Based Power-Up Sequencing. There arrow buttons allow one to change the sequencing order.

Power-up is shown in Figure 14a. The time at 0 is the time the CTRL signal or PMBus OPERATION asserts to enable. The first rail to power-up is Vout1 since it has been configured to be the first product in the sequence. It starts it's ramp after 10 ms (TON_DELAY). The time of the Vout1 ramp, TON_RISE, is 20 ms. Power good for Vout1 then goes high 10 ms (POWER_GOOD_ DELAY) after Vout1 is above power good threshold, which is marked by the vertical cursors in Figure 9a. At the time of power good for Vout1 going high, the first product communicates over the GCB bus that the next product in the group can begin its enable procedure (not shown). The delay for Vout2 to begin its turn on is set to 10 ms (TON_DELAY). The ramp time, TON_ RISE, for Vout2 is 10 ms. Similarly, once Vout2 reaches Power Good and after it's POWER_GOOD_DELAY, it communicates over GCB for Vout3 to power-up.

For power-down, the devices are configured to go down in the reverse order of power-up in this example. In Figure 14b, we again assume that the time at 0 is the time of a power-down event. Vout3 turns off first as it's configured as the first in the power-down sequence. Vout3 powers down after its TOFF_DELAY of 10ms. The time of the Vout3 ramp, TOFF_FALL, is 30ms. The next signal to change is the Power Good of Vout3 which goes low after Vout3's ramp-down is completed. At the time Vout3 ramps to zero volts, it communicates over the GCB bus that the next product in the group (Vout2) can begin its disable procedure. The delay for Vout2 to begin its turn off, TOFF_DELAY, is set to 10 ms. The ramp time, TOFF_FALL, for Vout2 is 20 ms. Finally, after Vout2 powers down, it communicates to Vout1 to begin power-down.

To test GCB sequencing with a 3E POL board (ROA 128 3836), use the same arrangement of BMR 462, 463, and 464 modules as shown in Example 1. One difference though is that each module must be connected to the common GCB bus, which is done by connecting the fourth jumper for each module. The jumper pins for the Example are shown in Figure 15 below.

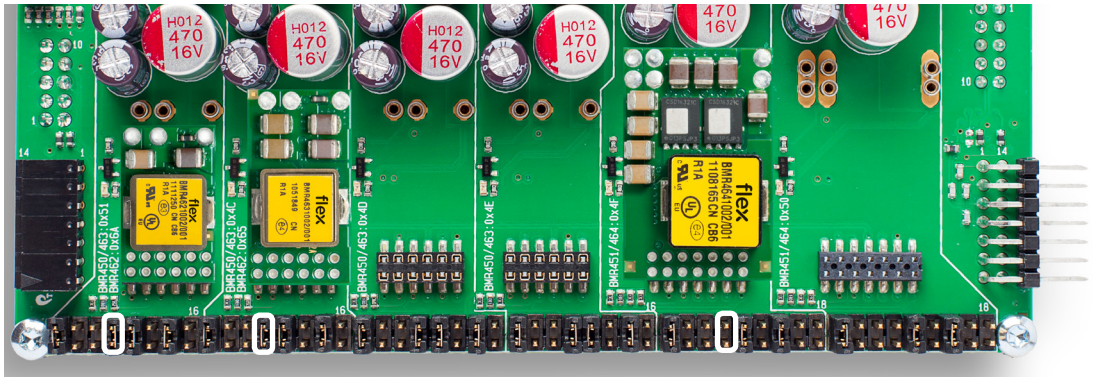


Figure 15. Setting up 3E POL Board (ROA 128 3836) jumpers for GCB Based Sequencing.

Commands used by Flex Power Designer for GCB Sequencing

When creating a GCB-based sequencing rail with Flex Power Designer, the following commands are automatically set:

- SEQUENCE - Used to arrange the sequence order
- GCB_CONFIG - The GCB_ID on each device is assigned and used in the SEQUENCE command, and GCB_TX communication enabled (GCB_TX is not configurable in any register in BMR 465. It is always enabled)
- MISC_CONFIG - Disable precise timing mode (Precise timing is not available for all products. See appendix I for details on precise timing.)
- ON_OFF_CONFIG - Power-Down with Soft-Off timing settings
- Ramp-Up timing settings - TON_DELAY, TON_RISE, POWER_GOOD_ON, POWER_GOOD_DELAY
- Ramp-Down timing settings - TOFF_DELAY, TOFF_FALL

Tables 5 and 6 describe these settings using the configuration of Example 3. Specific command descriptions can be found in AN302.

NOTE: As shown in these tables, the SEQUENCE command has separate enable bits for up and down sequencing. Due to a device issue, disabling sequencing can only be done by setting the SEQUENCE command to all 0's, disabling both up and down sequencing.

	GCB_CONFIG			SEQUENCE		SEQUENCE	
	GCB Broadcast Group Bits 12:8	GCB TX Inhibit Enable Bit 5	GCB Id Bits 4:0	Enable Prequel Rail Bit 15	Prequel Rail Bits 12:8	Enable Sequel Rail Bit 7	Sequel Rail Bits 4:0
Vout1 (2.5 V)	00000	0	00001	0	0 0000	1	0 0010
Vout2 (1.2 V)	00000	0	00010	1	0 0001	1	0 0011
Vout3 (1.0 V)	00000	0	00011	1	0 0010	0	0 0000

Table 5. Example 3 settings of GCB_CONFIG and SEQUENCE commands. Note that this table is only valid for BMR 462- 64 and BMR 466. For GCB_CONFIG bit definitions of BMR 465, please refer to the BMR 465's Technical Specification.

	TON_DELAY	TON_RISE	POWER_GOOD_ON	POWER_GOOD_DELAY	MISC_CONFIG[7]	TOFF_DELAY	TOFF_FALL	ON_OFF_CONFIG
	Delay [ms]	Rise [ms]	Power Good [V]	Power Good Delay [ms]	Disable Precise Timing mode	Delay [ms]	Fall [ms]	Power-down using soft-off settings Bit 0
Vout1 (2.5 V)	10	20	2.40	10	1	10	30	0
Vout2 (1.2 V)	10	10	1.15	10	1	10	10	0
Vout3 (1.0 V)	10	30	1.15	10	1	10	30	0

Table 6. Example 3 power-up and power-down settings. Note that MISC_CONFIG command and Precise Timing bit are not implemented in all products, see Appendix 1.

Method Four - Voltage Tracking

Overview

Voltage tracking allows one or more power rails to track another power rail's voltage. 3E Point of Load modules include an analog input pin, VTRK, which can be used to track another voltage supply.

When a product is configured to the voltage tracking mode as shown in Figure 16, the voltage applied to the VTRK pin acts as the reference for the product's output regulation. Rise and fall time settings are ignored. The startup delay settings control when tracking starts. The output will take on the power-up/shut-down characteristics of the reference voltage present at the VTRK pin. The shut-down delay setting is only used on the turn-off end of the tracking condition. This means that the shut-down delay setting sets the timeout for the tracking voltage to turn off in the event that the tracked voltage does not achieve zero volts. Certain tracking modes are also configurable to set the percentage of tracking and response to the power good signal.

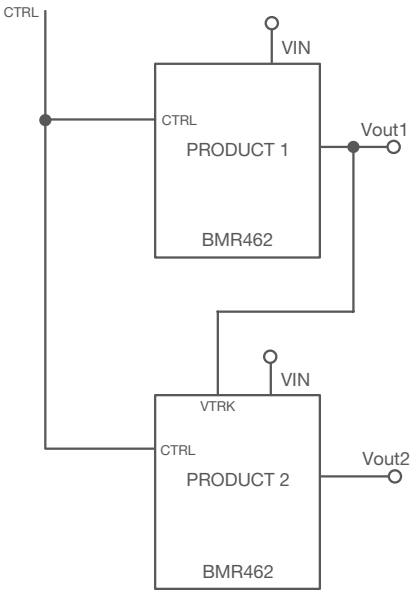


Figure 16 Voltage Tracking Configuration.

In a tracking group, the product that has its output voltage to any VTRK pin of another product is defined as the tracking master. This tracking master will control the ramp delay and ramp rate of all tracking products and is not itself placed in the tracking mode. The tracking master is typically configured to the highest output voltage for the group since all other product output voltages are meant to track and never exceed the tracking master output voltage. It is assumed for a tracking group, that all of the CTRL pins are connected and driven by a single logic source.

Example 4 - Configuring Voltage Tracking With Flex Power Designer

Setting up the tracking relationship can be done with Flex Power Designer. In this example, a BMR 464 with an output voltage of 2.5 V is used as the tracking master, whereas a BMR 463 is used for the 1.25V tracking slave rail,and a BMR 461 used for the 1.45V tracking slave rail. In the following steps we'll setup the second rail to 'track' the first rail with a scale of 50%.

First, add the tracking function by right-clicking the "Functions" menu.

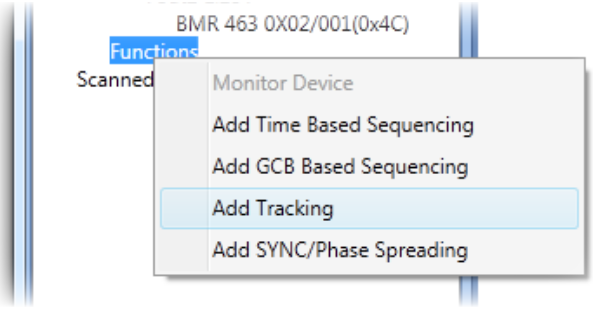


Figure 17 Adding Voltage Tracking Function.

Then, add the three rails to the tracking function

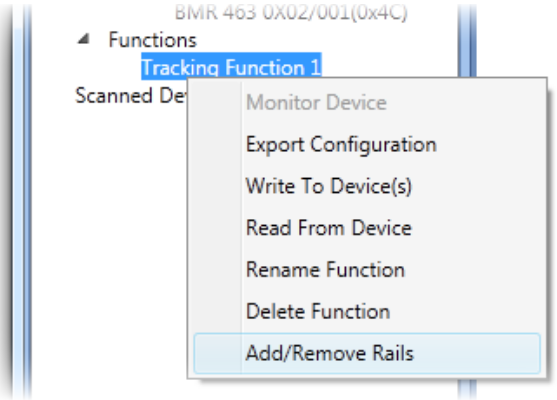


Figure 18. Adding rails to tracking function.

Once you have created your tracking function, in this case the name is "Tracking Function 1", you can start to configure it.

In the following, you will make necessary tracking-related settings, that in the end will result in the configuration shown in Figure 19.

Master Rail	Output Voltage [V]	On Delay [ms]	On Rise [ms]	Off Delay [ms]	Off Fall [ms]	Status
Vout1_2.5V	2.50 V	2.25	10	7	10	

Slave Rails	Uplimit Voltage	Target Voltage [V]	Ramp Scale [%]	Track Sag Always	External resistor R1 [kΩ]	External resistor R2 [kΩ]
Vout2_1.25V	Master	1.25	50	<Default>	Not needed	0
Vout3_1.45V	Master	1.45	58	<Default>	10	73.2

Figure 19. Tracking settings in Flex Power Designer. Vout1 is configured as tracking master, whereas Vout2 and Vout3 are the slaves that tracks Vout1.

There are a few basic rules that must be followed in setting the turn-on and turn-off settings in a tracking relationship of standalone as well as parallel rails. The Power Designer checks these rules and reports a green light on the Status indicator of everything is correct. For information about these rules, see Appendix 2.

Tracking Master Rail's configuration:

The desired turn-on and turn-off settings are added in the Master Rail's row in the Power Designer as shown in Figure 19. In order to fulfill the rules, indicated by a Status green light, you may need to increase the On Delay times.

Slave Rails' configuration

The first thing to set, for each slave, is the Uplimit Voltage, which is the upper limit of the slave's voltage. It can be set to either Master or Target. If Target is selected, then the desired voltage level is manually written in the Target Voltage field. After turn-on is completed, this voltage will be the slave's ouput voltage during normal operation. If Master is selected, then the slave's output voltage will be determined by the Master's output voltage multiplied with the Ramp Scale value. Choosing 100% Ramp Scale will result in a coincident tracking, whereas all values below 100% will result in a ratio-metric tracking.

If the chosen Ramp Scale requires an external voltage divider to be connect between the master's output voltage and the slave's tracking input, the Power Designer will return information on that in terms of resitors values for R1 and R2, see Figure 20.

Finally, the BMR 462 - 464 products offer a special feature called Track Sag Always, which is disabled by default. See AN302, TRACK_CONFIG, bit 0 for details about this feature.

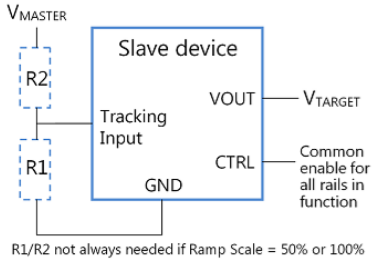


Figure 20 Tracking – Turn-on sequence example.(x-scale is 10 ms/div)

Tracking In Action

Figure 21 shows the scope set to trigger on the CTRL event. The CTRL signal is the first to go high. The next signal to change is the beginning of the Vout1 turn-on ramp since it has been configured to be the tracking master of the tracking group. It occurs about 15 ms after CTRL. The time of the Vout1 ramp is 10 ms. Vout2 then begins tracking at 50% of Vout1, whereas Vout3 is tracking at 58% of Vout1.

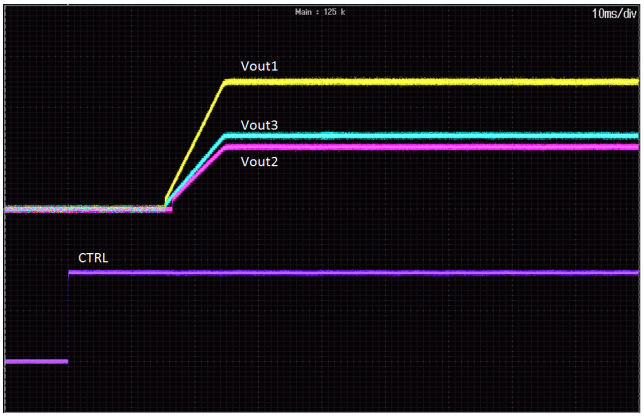


Figure 21 Tracking – Turn-on sequence example.(x-scale is 10 ms/div)

BMR 461 Tracking Design Considerations

The BMR 461 series offers tracking as well, but the configuration differs somewhat from the BMR 462-464, and 466 configuration.

First, the tracking mode is set via a resistor pinstrap between the VSET and PREF pins. This is detailed further in the BMR 461 Technical Specification

Secondly, a BMR 461 product always requires a voltage divider in terms of R1 and R2 as illustrated in Figure 20.

BMR 463,464 and 466 Tracking Design Considerations

If Dynamic Loop Compensation (DLC) is enabled the tracking slaves' Rise/Fall times may be adjusted slightly until the desired tracking accuracy is achieved.

When using a current sharing group and voltage tracking, the VTRK pin of each current sharing group member must be tied together, and connected to the tracking master's output voltage. The tracking slaves' Rise/Fall times may also be adjusted slightly until the desired tracking accuracy is achieved.

If both current sharing and DLC is used together with voltage tracking, constrain the rise/fall time between 5 and 10 ms to ensure current sharing while ramping. The time requirement is needed for the DLC to calculate loop gain during the start-up/shut-down ramps.

For the best possible tracking accuracy, disable DLC and instead assign PID coefficients using the Loop

For details about Voltage Tracking, see Appendix 2.

BMR 465 Tracking Design Considerations

Having the BMR465 as a tracking slave requires that the tracking master use a TON_DELAY of 0-10ms. It is preferred that the delay be 0ms unless a delay is required. In Figure 22, an power-up and off sequence of 100 accumulated traces are shown.

Higher TON_DELAY values of the tracking master may work, but may require adjustments of USER_ CONFIG[15:11] (Minimum duty cycle) settings of the BMR 465 tracking slave. You may also need to adjust the IOUT_UC_FAULT_LIMIT and/or IOUT_OC_ FAULT_LIMIT settings to avoid such faults during down-tracking.

Figure 22 Coincident Tracking – Power-o/noff sequence of a BMR 464 as tracking master (TON_DELAY = 10ms, TOFF_DELAY = 0ms, Vout = 3.,3V in yellow color) and a BMR 465 as tracking slave (TON_DELAY = 0 ms, TOFF_DELAY = 35ms, Vout = 1V in light blue color) CTRL signal is shown in lilac color. The oscillscope plot shows 100 accumulated tests. (x-scale is 20 ms/div).

As a consequence of this BMR 465 TON_DELAY requirement, you can not have a current sharing rail of BMR 463, 464 or 466 as a tracking master for a BMR 465: The TON_DELAY time needed for a proper current sharing functionality is too long.

Appendix 1 – Note On Precise Timing

As mentioned earlier, some BMR 462, 463, 464 and 466 3E Point of Load products offer a “precise timing” mode during ramp-up. This mode, when enabled, reduces turn-on-delay variations by continuously monitoring the output voltage even when the product is disabled.
Precise ramp-up timing mode may be applied when using either time-based, event-based or voltage tracking sequence methods with standalone rails (i.e., not current sharing rails).

For the products supporting precise ramp-up timing it is enabled by default. Precise ramp-up timing is activated when MISC_CONFIG[7] is set to 0. It shall be noted that Precise ramp-up timing does increase the amount of standby current used by the product.

Without precise ramp-up timing on BMR 462, 463, and 464 product, there is an additional delay during turn-on. Please refer to the products’ Technical Specification for details about delay accuracy.

NOTE: BMR 465 does not offer a precise timing mode.

NOTE: BMR 465 does not support the MISC_CONFIG command.

Appendix 2 – Voltage Tracking Details

There are a few basic rules that must be followed when configuring the turn-on and turn-off settings in a tracking relationship of standalone rails. This appendix describes these rules for standalone rails. If the design includes tracking with parallel rails, consult the section on Voltage Tracking in AN307.

When using the Tracking function in Flex Power Designer all these rules will be handled automatically.

Turn-on Delay (TON_DELAY):

The module that is tracking the master device, called the slave, should have its turn-on delay, T_{ONdel}, set to a value that is some milliseconds less than the master device's turn-on delay. This is to take the accuracy of the delay values into account and to make sure that the slave is already enabled when the master starts to ramp-up. The T_{ONdel} value will vary for different products and modes.

First, The master's turn-on delay, $T_{ONdel,M}$, is entered by the user, but it must fulfill the unequality in Eq A1, where *n* is the number of slaves.

$$T_{ONdel,M} \geq \max_{1 \leq i \leq n} \left(T_{ONdel,Min,M}, \left(T_{ONdel,Min,Si} + T_{Acc_{Pos},Si} - T_{Acc\_Neg,M}\right)\right) \quad (A1)$$

The minimum turn-on delay values, $T_{ONdel,Min}$, are found in each product's Technical Specification. The T_{Acc_Pos} (> 0), and T_{Acc_Neg} (< 0) values are the products' output voltage delay time (TON_DELAY) accuracy also found in each product's Technical Specification.

From Eq A1, the smallest possible turn-on delay value of the master can be defined as defined in Eq A2. In Fig A1, the usage of Eq A2 is illustrated.

$$T_{ONdel,M} = \max_{1 \leq i \leq n} \left(T_{ONdel,Min,M}, \left(T_{ONdel,Min,Si} + T_{Acc\_Pos,Si} - T_{Acc\_Neg,M}\right)\right) \quad (A2)$$

Having the turn-on delay time for the master, $T_{ONdel,M}$, the turn-on delay for each slave *i*, $T_{ONdel,Si}$, is then calculated by using Eq. A3.

$$T_{ONdel,Si} = T_{ONdel,M} + T_{Acc\_Neg,M} - T_{Acc\_Pos,Si} \quad (A3)$$

Note: When BMR 465 being a tracking slave, the TON_DELAY value can not be set in accordance to Eq. A3. Instead, the TON_DELAY value of the BMR 465 tracking slave should be set to smallest possible value. (This reflect the fact that the BMR 465 actually ignores the TON_DELAY setting and instead uses shortest possible delay time).

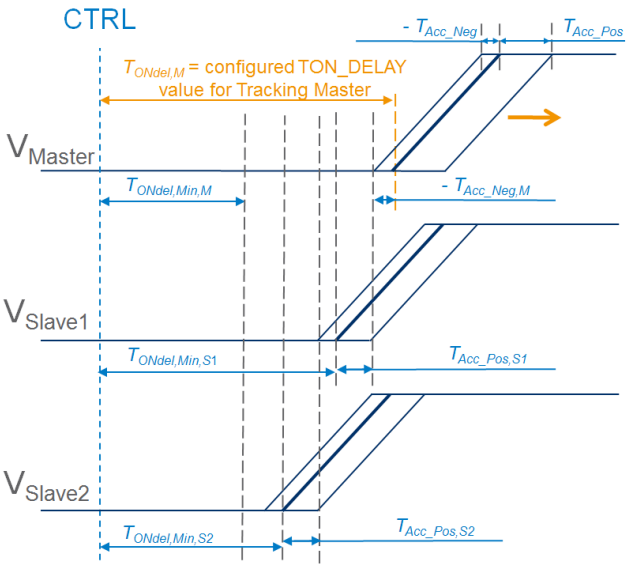


Figure A1. Calculation of smallest possible turn-on delay value of the master using Eq. A2.

Turn-Off Delay (TOFF_DELAY):

The master's turn-off delay, $T_{OFFdel,M}$, has no restrictions but the slaves have: Every slave must have a turn-off delay following Eq A4. This is to take the accuracy of

$$T_{OFFdel,Si} \geq \max\left(T_{OFFdel,Min,Si}, \left(T_{OFFdel,M} + T_{OFFfall,M} + T_{Acc_{Pos},M} - T_{Acc_{Neg},Si}\right)\right) \quad (A4)$$

the delay values into account and to make sure that the master has finished ramp down before the slaves are disabled. In Fig A2, the implications of Eq A4 are illustrated.

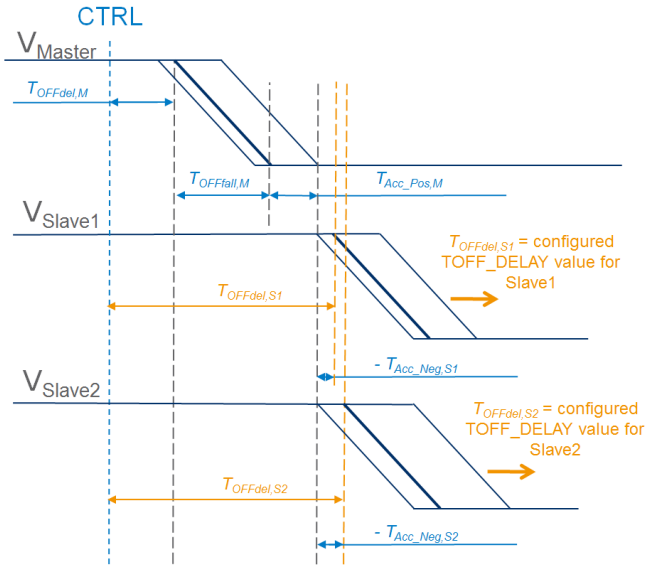


Figure A2. Calculation of smallest possible turn-off delay values of the slaves using Eq. A4.

Output Voltage Delay Time See Note 6	Delay duration	See Note 16	10	ms
	Delay duration range	PMBus configurable	2-500000	
	Delay accuracy turn-on	Default configuration: CTRL controlled Precise timing enabled	±0.25	ms
		PMBus controlled Precise timing disabled Current sharing operation	-0.25/+4	ms
	Delay accuracy turn-off		-0.25/+4	ms

Figure A3. Delay accuarcy and minimum delay values as found in the BMR 463 (and BMR 464) Technical Specification.

Soft-start On Delay Time Note 5	Delay duration		10	ms
	Delay duration range	PMBus configurable TON_DELAY	1-145	ms
	Delay set resolution		0.6	ms
	Delay set accuracy	TON_DELAY value sent versus read-back	±0.5 x Delay set resolution	ms
	Delay accuracy	Actual delay duration versus TON_DELAY read-back	±0.8	ms

Figure A4. Delay accuarcy and minimum delay values as found in the BMR 461 Technical Specification.

Turn-On Rise Time (TON_RISE):

If a standalone rail is tracking, this is essentially a don't care value as it will be following the tracking master's turn-on slope. If using a current-sharing rail, follow the directions in the Current Sharing section in page 19.

Turn-Off Fall Time (TOFF_FALL):

Similar to the rise time, this is also a don't care value for the standalone tracking slave. If using a tracking with current-sharing rail, follow the directions in page 19.

Example

In the example in Fig 19, the 2.5 V tracking master is a standalone BMR 463 2002, the 1.25 V tracking slave is a standalone BMR 464 2002, whereas the 1.45 V tracking slave is a standalone BMR 461 3001.

First, we need information about the Master's minimum delay accuracy value, $T_{Acc\_Neg,M}$. The 2.5 V master is configured for precise ramp-up timing. From the BMR 463 Technical Specification, see Fig A3, we find that $T_{Acc\_Neg,M}$ equals -0.25 ms in the 'Precise timing enabled' row. For shut-down (e g turn-off) we see that the delay accuracy follows the normal timing specifications, regardless of precise ramp-up timing settings. Reading the BMR 463 Technical Specification again, we find that $T_{Acc\_Pos,M}$ equals +4 ms. We also see that the minimum delay duration, $T_{ONdel,Min,M}$ equals 2 ms.

The 1.25 V slave is configured for normal timing. In a similar way as for the BMR 463 product, we find that $T_{Acc\_Pos,1.25V\ Slave}$ is 4 ms, and that the minimum delay, $T_{ONdel,min,1.25V\ Slave}$, is found to be 2 ms by reading the BMR 464 Technical Specification.

The BMR 461 only offers normal timing. So, we then find that the $T_{Acc\_Pos,1.45V\ Slave}$ equals 0.8 + (0.5 x 0.6) ms = 1.1 ms and that the minimum delay, $T_{ONdel,min,1.45V\ Slave}$, equals 1 ms from the BMR 461 Technical Specification, see Fig A4.

We now have collected the data we need from the products' Technical Specifications. Next, we can calulate the delay times.

By using Eq A2, we find that the minimum turn-on delay time of the master is limited by the 1.25 V slave, which in this example has a minimum turn-on delay equal to 2 ms and a delay accuracy equal to 4 ms. Since the negative delay accuracy of the master is -0.25 ms the minimum possible TON_DELAY value for the master is 6.25 ms. Hence, we can set $T_{ONdel,M}$ to 6.25 ms. The calculations are also illustrated in Fig A5.

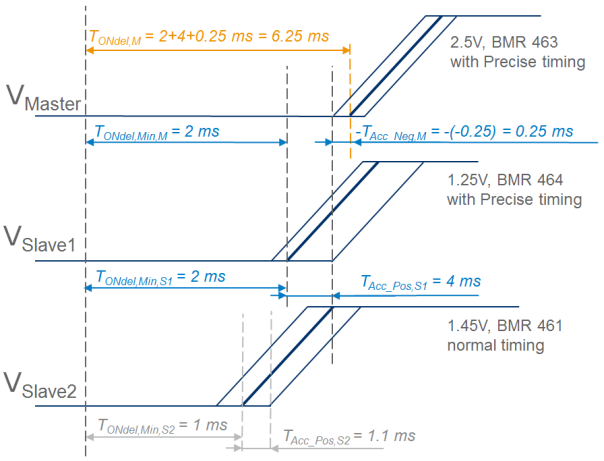


Figure A5. TON_DELAY calculations for tracking master using Eq. A2.

Now, by using Eq A3, $T_{ONdel,1.25V\ Slave}$ is easily found to be 6.25 - 0.25 - 4 ms = 2 ms, whereas $T_{ONdel,1.45V\ Slave}$ is found to be 6.25 - 0.25 - 1.1 ms = 4.9 ms (not shown in figure).

Finally, in track-down we have chosen $T_{OFFdel,M}$ to 7 ms and $T_{OFFfall,M}$ to 10 ms. By applying these values to Eq A4, $T_{OFFdel,1.25V\ Slave}$ will be 7 + 10 + 0.25 + 0.25 ms = 17.5 ms, whereas $T_{OFFdel,1.45V\ Slave}$ will be 7 + 10 + 0.25 + 1.1 ms = 18.35 ms. The calculations are illustrated in Fig A6.

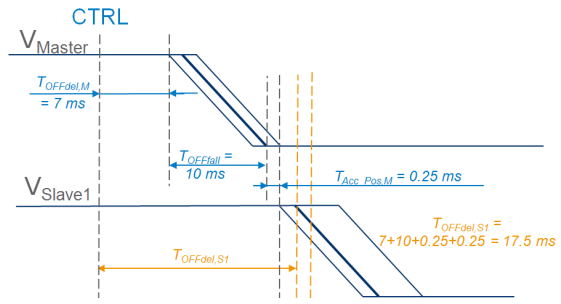


Figure A6. TOFF_DELAY calculations for the two tracking slaves using Eq. A4.

Current Sharing (BMR 463, 464, and 466)

For current sharing rails, voltage tracking is emulated by configuring the output ramp to match the ramp of the tracking master's ouput voltage via each tracking slave's VTRK pin. Doing this affects how the tracking slaves Rise/Fall times should be set along with the tracking master's power-up delay times.

Setting Rise/Fall Times

The relation between the tracking master and a tracking slave's rise/fall times when the tracking slave is also a current sharing rail is calculated from Eq A5,

$$T_{Rise;Fall,Si} \geq 1.1 \cdot T_{Rise;Fall,M} \cdot \frac{V_{Out,Si}}{V_{Out,M}} \cdot \frac{1}{Tracking\_ratio} \quad (A5)$$

where $T_{Rise;Fall,M}$ is the rise or fall time of the tracking master, $V_{Out,M}$ is the output voltage of the tracking master, $V_{Out,Si}$ is the output voltage of the tracking slave *i*, *Tracking_ratio* is the desired (and emulated) ratio between the tracking slave and tracking master (normally this value is between 0.5 and 1), and finally, $T_{Rise;Fall,Si}$ is the rise or fall time of the tracking slave *i*.

Note, that Eq A5 allows configuring of any tracking ratio, simply by adjusting the rise/fall time (tracking ratio should always be set to 100% in TRACK_CONFIG).

Example

To configure a 1.2 V current sharing rail to track a 3.3 V voltage with ramp time 5 ms, by the desired tracking ratio 50%, the ramp time of the products in the current sharing group should be set to

1.1 x 5ms x (1.2V / 3.3V) x (1 / 0.50) = 4 ms.

The ramp time can be adjusted upwards to improve the current sharing balance during the ramp, or downwards to improve the accuracy of the tracking ratio.

Setting Turn-on Delay Times

For current sharing rails also the turn-on delay time (TON_DELAY) values shall be configured somewhat different from a stand-alone rail. The value to use is found in the Product' Technical Specification. Typically this value is 15 ms. Hence, you should use $T_{ONdel,Min,Si}$ = 15 ms for each slave in Eq A2 to calculate the TON_DELAY value to use for the tracking master, $T_{ONdel,M}$.

In addition, the $T_{Acc\_Pos,\ Si}$ to use for a the tracking slave devices in a current sharig rail is 7 ms.

Setting Turn-Off Delay Times

For current sharing rails the turn-off delay time (TOFF_DELAY) values shall also be configured somewhat different from a stand-alone rail. The value to use is found in the Product's Technical Specification. Typically this value is the same as the TON_DELAY value (see above), i.e., 15 ms. Hence, you should use $T_{OFFdel,Min,Si}$ = 15 ms for each slave in Eq A4 to calculate the TOFF_DELAY value to use for each tracking slave $T_{OFFdel,Si}$.

NOTE: Voltage tracking with a pre-bias voltage at the output is not recommended since there is risk of phase currents to drift apart.

NOTE: For BMR 465 current sharing rails, voltage tracking is not supported. Only single BMR 465 supports tracking.

Appendix 3 – Experimental Results

In this appendix, experimental results of different sequencing & tracking setups are shown.

Time-based Sequencing - Example

Five rails were configured as a Time-based sequencing group enabled by a CTRL signal connected to all products' CTRL input. The products used, the power-up sequencing configuration, and the results from 100 power-ups (at room temperature), without and with precise ramp-up timing, are shown below.

Products used in experiment

BMR 462 2002/001	3.3V, 2.5V
BMR 463 2002/001	1.8V, 1.5V
BMR 464 2002/001	1.2V

Analysis

As can be seen from Fig A8, BMR 462-464 and 466 products without precise ramp-up timing one have to design for a larger safe margin in TON_DELAY than for products with precise timing in order to avoid overlaps of rails during power-up.

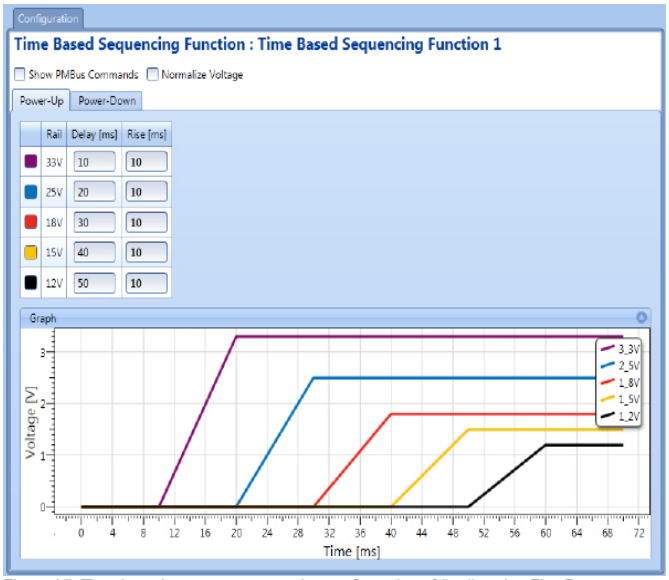


Figure A7. Time-based power-up sequencing configuration of 5 rails using Flex Power Designer design tool. The configured time space between the rails is 10ms.

Figure A8. Time-based up-sequencing accumulated variations from 100 power-up occasions, without precise timing of BMR 462-464 room temperature. The CTRL signal, the bottom trace, triggers the start of all five rails. As seen, the accuracy of the start-up time for each rail is in the range of {-0.25, 4ms] related to the CTRL signal positive ramp. Note: The 1.5V rail (in light blue color), is configured for precise-timing ramp-up. (20 ms/div).

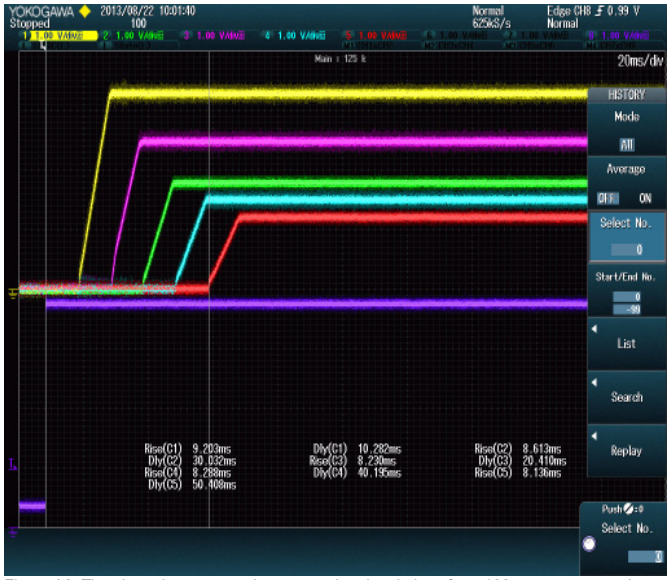


Figure A9. Time-based up-sequencing accumulated variations from 100 power-up occasions, with precise timing of BMR 462-464 at room temperature. The CTRL signal, the bottom trace, triggers the start of all five rails. Compared to the same devices configured without precise-ramp-up timing, the accuarcy are now in the +/- 0.25 ms range. From the one of the 100 sweeps, the following was measured by the oscillscope: First rails starts to ramp-up after 10.3ms, second rail after 20.4 ms, third rail after 30.0ms, fourth rail after 40.2ms, and finally rail 6 starts to ramp after 50.4 ms. As seen, there variations are very small. (20 ms/div).

Event-based Sequencing - Example

Five rails were configured for event-based sequencing enabled by a common CTRL signal connected to all products' CTRL input. The products used, the power-up and power-down sequencing configuration, and the results from 100 power-ups (at room temperature) are shown below.

Products used in experiment

...BMR 464 2002/001 3.3V, 2.5V, 2.2V*
...BMR 461 3001/001 1.5V, 1.0V

*The 2.2V rail is configured for precise ramp-up timing.

Analysis

As seen from Fig A10 and A12, BMR 461 products and BMR 462-464 products with precise ramp-up timing can be ramped-up with quite a good accuracy: 91 ms configured/expected for last rail's PG signal to be asserted and 91.1 - 92.8 ms acheived from 100 power-ups.

In power-down, the variation is much larger: 66 ms configured/expected whereas 65.5 - 78.2 ms achieved from 100 power-downs.

Note, non-overlap power-up and power-down is always acheived when using event-based sequencing.

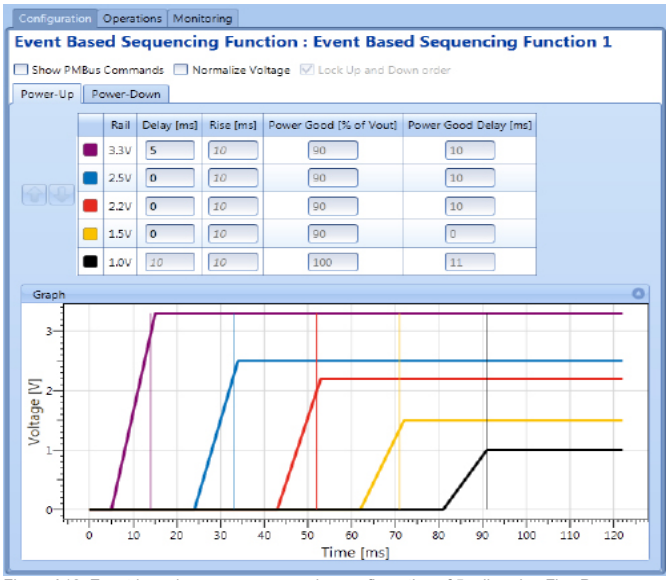


Figure A10. Event-based power-up sequencing configuration of 5 rails using Flex Power Designer design tool. The configured start-up time for all rails is 91 ms.

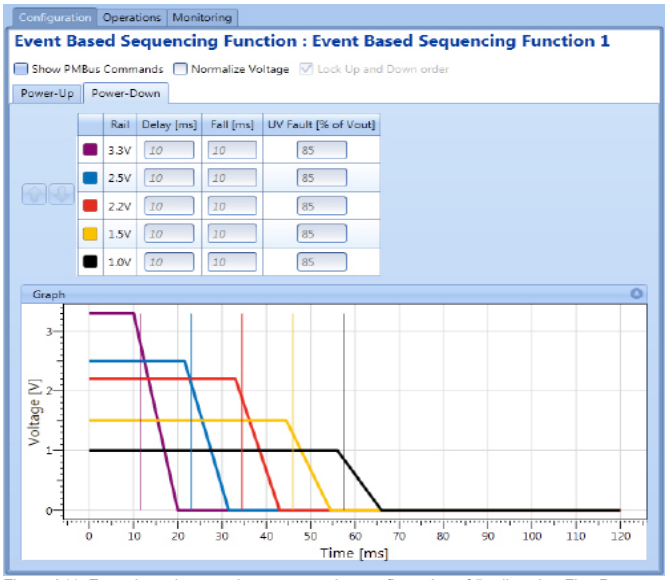


Figure A11. Event-based power-down sequencing configuration of 5 rails using Flex Power Designer design tool. The configured shut-down time for all rails is 66 ms.

Figure A12. Event-based up-sequencing accumulated variations from 100 power-up occasions at room temperature. The CTRL signal, the bottom trace, triggers the start of all five rails. First three rails uses BMR 464 2002/001 (with precise ramp-up timing) and the last two rails uses BMR 461 3001/001. The configured total up-sequencing time is 91 ms, see Figure A10. The achieved timing variation is 91.1 – 92.8 ms in this example. Also shown in this plot are the relativley small timing variations of the two PG signals from the 1.5V and 1.0V rails, respectively (the two small middle traces in dark lilac color). (20 ms/div).

Figure A13. Event-based down-sequencing accumulated variations from 100 power-down occasions at room temperature. The CTRL signal, the bottom trace, triggers the start of all five rails. First three rails use BMR 464 2002/001, whereas the last two rails uses BMR 461 3001/001. The configured total down-sequencing time is 66 ms, see Fig A11. The achieved timing variation for the whole sequencing group is 65.5 – 78.2 ms in this case, due to accumulation of errors in previous rails. Note that the BMR 464 rails significantly contributes to the this varation, whereas the BMR461 rails only do that marginally. (20 ms/div).

GCB-based Sequencing - Example

Five rails were configured for GCB-based sequencing group enabled by a common CTRL signal connected to all products' CTRL input. The products used in the experiment, the power-up and power-down sequencing configurations, and the results from 100 power-ups (room temperature) are shown below.

Products used in experiment

...BMR 462 2002/001 3.3V, 2.5V
...BMR 463 2002/001 1.8V, 1.5V
...BMR 464 2002/001 1.2V

Note: Precise ramp-up timing can not be used in GCB sequencing.

Analysis

As seen from Fig A16 and A17, BMR 462 - 464 (and BMR 465 and 466) can be powered-up and -down using GCB-based sequencing in the desired order (in contrast to event-based sequencing). But,the accuracy of the total sequencing time is in the same range for both power-up and power-down, since precise ramp-up timing cannot be used within a GCB-based sequencing group. This comes from the accumulation of the TON_DELAY accuracy of all rails.

Note, non-overlap power-up and power-down is always acheived when using GCB-based sequencing.

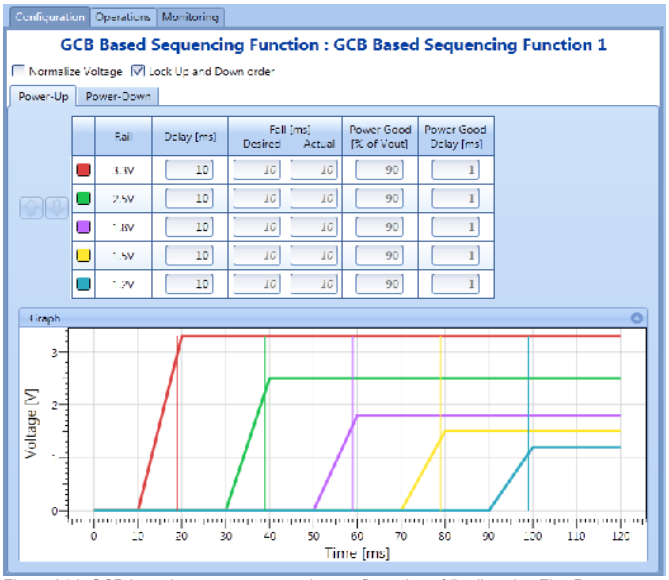


Figure A14. GCB-based power-up sequencing configuration of 5 rails using Flex Power Designer design tool. The total configured power-up time until last rail's PG is asserted is 98 ms.

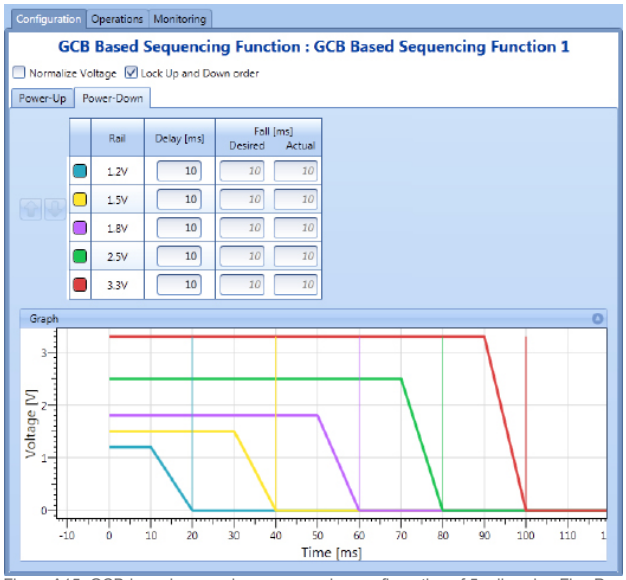


Figure A15. GCB-based power-down sequencing configuration of 5 rails using Flex Power Designer design tool. Total configured power-down time until last rail starts to fall is 90 ms.

Figure A16. GCB-based up-sequencing accumulated variations from 100 power-up occasions, of BMR 462-464. The CTRL signal, the bottom trace, triggers the start of all five rails. The configured total up-sequencing time is 98 ms. The achieved timing variation of the last rail is quite large in this example, 94.5 – 106.5 ms. This is due to to the fact that the timing error in previous rails are accumulated. However, non-overlap is always granted in GCB-based sequencing. (20 ms/div).

Figure A17. GCB-based down-sequencing accumulated variations from 100 power-down occasions of BMR 462-464. The CTRL signal, the bottom trace, triggers the start of all five rails. The configured total down-sequencing time is 90 ms. The achieved down-sequencing time, incl timing variation, is 105.0 – 118.0 ms. This is due to to the fact that the timing error in previous rails are accumulated. However, non-overlap is always granted in GCB-based sequencing. (20 ms/div).

Voltage Tracking - Example

Six rails were configured for voltage tracking enabled by a common CTRL signal connected to all products' CTRL input. The products used, the power-up and power-down sequencing configuration, and the results from 100 power-ups (room temperature) are shown below.

Products used in experiment

...BMR 463 0002/001 3.3V Tracking Master*
...BMR 463 0002/001 2.5V Slave, Coincident
...BMR 463 0002/001 1.65V Slave, Ratiometric, 50%
...BMR 461 3001/001 1.98V Slave, Ratiometric, 50%
...BMR 461 3001/001 2.3V Slave, Coincident
...2xBMR 464 0002/001 1.0V Slave, Coincident

*configured for precise ramp-up timing.

Analysis

When applying statistics methods to the data generated from this test, the findings in Table A1 about the rise and fall time variations during power-up and power-down voltage tracking can be made.

Rail	Type of Product	Rise time deviations		Fall time deviations	
		3σ [ms]	3σ [ms]	3σ [ms]	6σ [ms]
(Master)	BMR 463 0002/001	0.11	0.22	0.33	0.66
2.5V(coincident)		0.13	0.25	3.71	7.43
1.65V (50% slave)		0.26	0.53	0.35	0.70
1.98V (50% slave)	BMR 461 3001/001	0.15	0.30	0.26	0.52
2.3V (coincident)		0.10	0.21	4.67	9.33
1.0V (coincident)	BMR 464 0002/001 (2 pcs in parallel)	1.12	2.23	3.24	6.48

Table A1. Statistics from voltage up- and down-tracking of 100 occasions. σ is the standard deviation. 3σ means three times the standard deviation, etc.

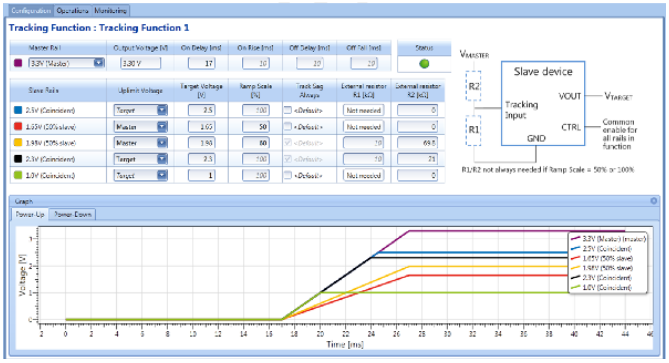


Figure A18. Voltage tracking power-up configuration of 6 rails using Flex Power Designer design tool.

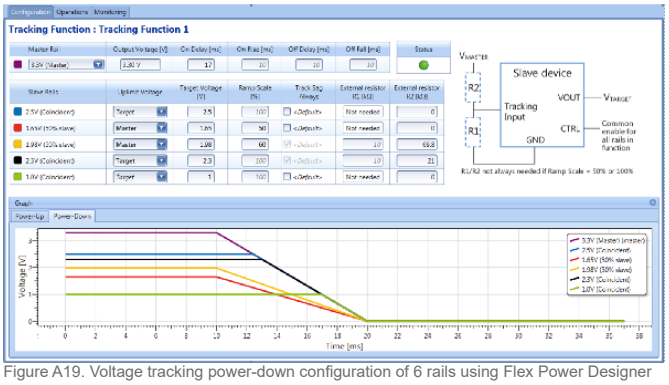


Figure A19. Voltage tracking power-down configuration of 6 rails using Flex Power Designer design tool.

Figure A20. Voltage up-tracking accumulated variations from 100 power-up occasions. The CTRL signal, the bottom trace, triggers the start of the tracking master rail. The tracking master, a BMR 463 0002/001 (3.3V) is configured with precise-ramp-up timing. As seen, the tracking slaves are following the master closely and the timing variation is small. The statistics are collected in Table A1. (20 ms/div).

Figure A21. Voltage down-tracking accumulated variations from 100 power-down occasions. The CTRL signal, the bottom trace, triggers the start of the tracking master rail. Compared to power-up, the timing variation between different start-up occasions is quite large.
Still the tracking slaves follows the tracking master closely in each start-up occasssion. This is however not possibe to see in this plot. The statistics are collected in Table A1. (20 ms/div).

Formed in the late seventies, Flex Power Modules is a division of Flex that primarily designs and manufactures isolated DC/DC converters and non-isolated voltage products such as point-of-load units ranging in output power from 1 W to 700 W. The products are aimed at (but not limited to) the new generation of ICT (information and communication technology) equipment where systems' architects are designing boards for optimized control and reduced power consumption.

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