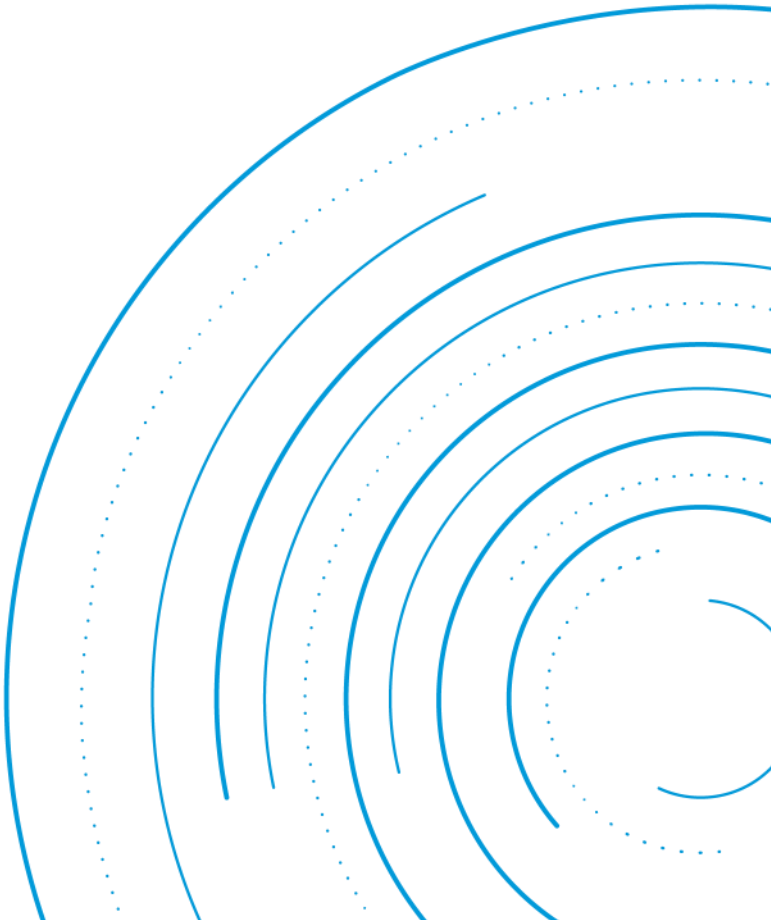
flex Power Modules

APPLICATION NOTE 323

# Input filter design - digital Point of Load



# Abstract

Our digital Point of Load products can be configured, controlled and monitored through a digital serial interface using the PMBus® power management protocol. This application note provides information on how to design input filters for these digital PoL regulators. This application note applies to the following products:

- BMR461
- BMR462
- BMR463
- BMR464
- BMR465
- BMR466
- BMR467
- BMR469
- BMR473
- BMR474

# Content

# Input filter design

## Introduction

Flex Power Modules' digital PoL regulators are implemented by using a non-isolated synchronous buck topology as shown in Fig. 1.

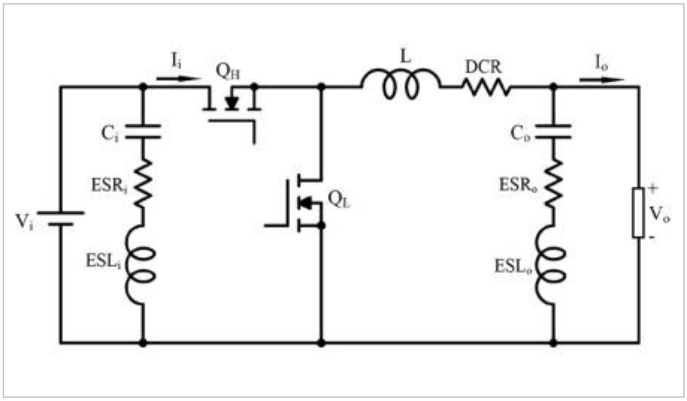



*Figure 1a: Simplified schematics*

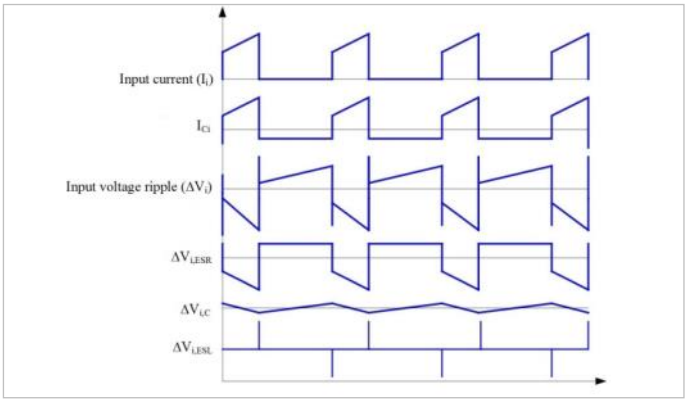



*Figure 1b: Input waveforms of a buck converter*

During normal operation of a buck power stage, $Q_H$ and $Q_L$ are alternatively switched on and off with the on and off times governed by a control circuit with a fixed frequency PWM scheme. Output current for a buck power stage is smooth as a result of the inductor/capacitor combination on the output side. But input current for a buck power stage is pulsating or chopped due to the power switch $Q_H$ current that pulses from zero to full load every switching cycle. Obviously, the input capacitor is critical for proper operation of the regulator and to minimize noise emissions from a switching regulator.

In many applications, a fairly conventional intermediate bus architecture (IBA) is used as shown in Fig. 2.

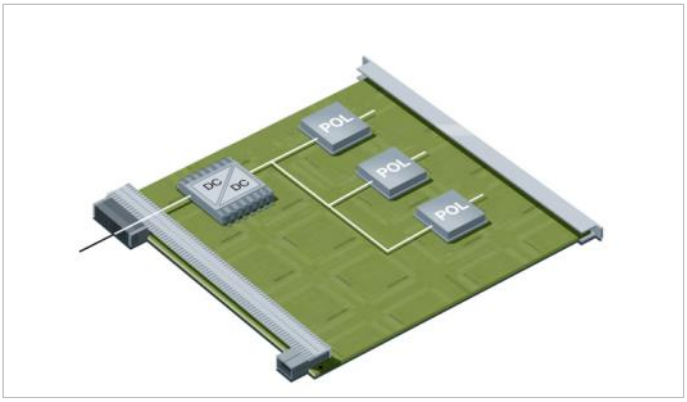



*Figure 2: In a IBA board IBC feeds multiple PoLs*

In an IBA, a board-level intermediate bus converter (IBC) feeds multiple PoL regulators which are located in proximity to the load circuitry and supply the final operating voltages.

All these switching converters generate ripple and noise on the common DC input bus which should be suppressed. If it isn't filtered, input ripple and noise of a regulator can reach levels high enough to interfere with other devices powered from the same source.

In addition to the input ripple and noise generated by the PoL converters, the IBC has its own output voltage ripple and noise.

So the input filter on a PoL regulator may play two important roles. One is to prevent electromagnetic interference, generated by the switching source from reaching the power line and affecting other equipment. The second purpose of the input filter is to protect the converter and its load from transients that appear in the input voltage thereby improving the system reliability. This application note describes sources of input ripple and noise in PoL regulators and design of input filters to attenuate its occurrence.

## Stability

A filter having attenuation sufficient to meet noise and ripple specifications is constructed and added to the input. If the input filter consisting of only capacitors (C), stability is not a problem. If the input filter also includes inductors (LC), the stability must be checked: the input filter changes the dynamics of the regulator. The output impedance may become large over some frequency range, possibly exhibiting resonances. The audio susceptibility may be degraded. The problem is that an LC input filter can affect the dynamics of the converter, often in a manner that degrades regulator performance.

An important yet often overlooked aspect of input filter design is meeting the Middlebrook criterion. According to the criterion, the input filter does not significantly modify the converter loop gain if the output impedance curve of the input filter is far below the input impedance curve of the converter, see Equation (1). In other words to avoid oscillations it is important to keep the peak output impedance of the filter, $Z_{o,filter}$, below the input impedance of the converter, $Z_{i,}$PoL. See Fig. 3 for an example

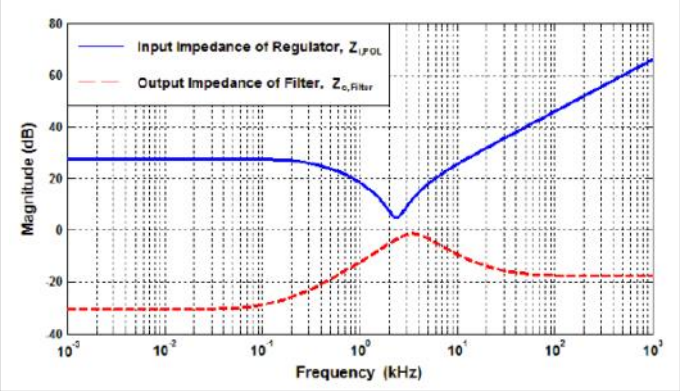



*Figure 3: Example output impedance of Input filter and input impedance of regulator— waveforms of a buck converter: the two curves are separated*

$$Z_{i,\mathrm{POL}} >> Z_{o,\mathrm{Filter}} \qquad \text{(E:1)}$$

A PoL regulator is designed to supply constant voltage to a load, (almost) independently of load currents. So the minimum input impedance of the regulator, $Z_{i,PoL,min}$ over the controller bandwidth is computed as follows.

$$Z_{i,\mathrm{POL,min}} = \frac{V_i^2}{\eta \cdot V_o \cdot I_o} \qquad \text{(E:2)}$$

where

- $V_i$ is the input voltage,
- $V_o$ is the output voltage,
- $I_o$ is the steady state output load current,
- η is efficiency of the regulator.

Appendix A permits calculation of the input impedance of a buck converter with more details.

## Input ripple and noise sources

For a PoL regulator, the input ripple and noise has three components. The first occurs at the fundamental switching frequency commonly referred to as ripple. The second component is AC voltage excursions on the input bus due to load transient changes at the output of PoL modules. This is usually a low frequency phenomenon with settling times of the order of several hundred microseconds with equivalent frequencies in the few tens of kHz.

The third noise component is associated with the very high frequency ringing that occurs during switching transitions. This type of noise is created due to the switching action of the PoL when it draws power from the input source in discontinuous current pulses. The frequency of this component is equal to the switching frequency of the PoL and it has several harmonics, expanding well into the MHz frequency region.

Another source for high frequency noise on the DC bus is the IBC. The reflected ripple and noise from the source converter is usually much smaller than the ripple and noise caused by the PoL modules.

This is due to the fact that typical IBC has an LC filter at its output which reduces the ripple and noise significantly. Therefore, most of the ripple and noise created on the input bus is mainly due to the PoL regulators.

Note that all Flex Power Modules' digital PoL regulators have ceramic filter capacitors placed on the module which reduces the ripple and noise significantly. However, this ripple and noise can be reduced further by placing extra capacitors on the input bus of the PoL modules.

### Fundamental switching frequency input ripple

For a buck converter, the output inductor connects to the input during the on portion of the switching cycle and disconnects during off periods. For a constant DC voltage on the input, the input capacitor charge at $Q_H$ on-time must be equal and opposite to the capacitor charge at $Q_H$ off-time. Fig. 1 displays the input capacitor wave-shapes and Equation (3) details the amount of ceramic capacitance required to reduce the ripple voltage amplitude to an acceptable level. The ripple magnitude varies with the input voltage and is a maximum at 50% duty cycle.

$$C_{i,\min} = I_o \cdot \frac{D \cdot (1-D)}{\Delta V_{i,pp} \cdot f_{sw}}, \quad D = \frac{V_o}{\eta \cdot V_i} \qquad \text{(E:3)}$$

where

- $C_{i,min}$ is the minimum required ceramic input capacitance,
- $\Delta V_{i,pp}$ is the maximum allowed peak-peak input ripple voltage,
- $f_{sw}$ is the switching frequency,
- D is the duty cycle as defined above.

The input voltage ripple contributed by the equivalent series resistance, ESR, can be estimated as:

$$\Delta V_{i,ESR} = \left( I_o + \frac{\Delta I_{pp}}{2} \right) \cdot ESR_i \qquad \text{(E:4)}$$

where

- $\Delta V_{i,ESR}$ is the input voltage ripple caused by ESR of the input capacitor,
- $ESR_i$ is the ESR of input capacitor,
- $\Delta I_{pp}$ is the maximum output current ripple.

According to Equations (3) and (4), to reduce the input ripple, either increase the capacitance or decrease the ESR of the input capacitor. Ceramic capacitors typically have a very low ESR, and contribute little to the input voltage ripple.

The input filter capacitors carry the AC component of the current. Most of the ripple current flows through the input ceramic capacitors already placed inside the module. However, a portion of the AC ripple current is also drawn from the input bus where most of it is supplied by the external input capacitors. It is therefore crucial not to exceed the RMS current rating of the external capacitor chosen.

The RMS total current distributed between external and internal input capacitors, $I_{Ci,RMS}$, is calculated as follows

Note that the input RMS current can be calculated by sync/phase spreading function in Flex Power Designer (FPD) tool.

$$I_{Ci,\mathrm{RMS}} = I_o \cdot \sqrt{D \cdot (1-D)} \qquad \text{(E:5)}$$

### Low frequency noise due to output transient

When designing a system consisting of a single PoL or multiple PoL modules that make use of a shared bulk input capacitor bank, the first step is to calculate the magnitude of the input transient current. This is done by calculating the reflected input transient for each PoL module's output transient. After calculating the individual input transients for each module, add them up to get the total transient current. When calculating, one must determine the worst case transient combination of all modules and proceed accordingly. The magnitude of the input current transient, $\Delta I_i$, is calculated from Equation (6):

$$\Delta I_i = \frac{V_o}{V_i \cdot \eta} \cdot \Delta I_o \qquad \text{(E:6)}$$

where

- $\Delta I_i$ is the input transient current,
- $\Delta I_o$ is the output transient current.

Next, determine the maximum allowable voltage deviation, $\Delta V_{tr}$, on the input bulk capacitors. This is the maximum allowable dip during the peak transient step that was calculated in step one. The following equation calculates the minimum required input bulk capacitance, $C_{i,tr,min}$.

$$C_{i,tr,\min} = \frac{1.21 \cdot (\Delta I_i)^2 \cdot L_{ftotal}}{(\Delta V_{tr})^2} \qquad \text{(E:7)}$$

where $L_{ftotal}$ is a series filter inductor plus stray inductance. If not using filter inductor, stray inductance, $L_{src}$, should be accounted in the calculation.

**Note** that this equation is an approximation. The value it produces should be considered to be an absolute minimum amount. The value of capacitors selected to meet required total capacitance should take an account impact of the temperature and other factors such as DC bias and ripple current derating that can reduce an actual value.

### High frequency noise

High frequency input noise in DC/DC converters is a product of high frequency ringing or oscillation associated with parasitic elements of the converter power stage. Energy stored in the parasitic elements oscillates or rings during the switching transitions. This type of noise is usually hundreds of MHz.

Aluminum electrolytic and tantalum capacitors have high ESR values and thus are generally not suitable for decoupling the switching noise and ripple of the PoL module. However, they can be used in combination with ceramic capacitors for other purposes such as suppressing the lower frequency ripple caused by load transients.

For high frequency attenuation, capacitors with low ESL and low ESR for ripple current capability must be selected. To reduce high frequency voltage spikes at the input of the module, small-package ceramic capacitors should be placed at the input of the module. Layout is also important in dealing with high frequency switching ripple and noise. The ceramic capacitors should be placed as close to the PoL regulator as possible as shown in Fig. 4, followed by low ESR polymer and aluminum electrolytic capacitors if needed. Stray inductance should be minimized by using wide traces or shapes and parallel planes.

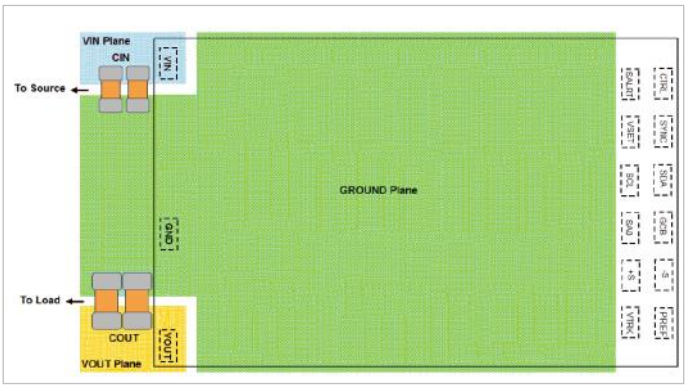



*Figure 4: Example layout of BMR463 module showing placing of input capacitors*

Since the RMS current will be shared by the input capacitors, it is recommended that ceramic capacitors be selected such that their impedance is considerably lower than the impedance of the tantalum and/or aluminum electrolytic capacitors at the switching frequency. This will ensure that most of the RMS ripple current will flow through the ceramic capacitors and not through the high ESR tantalum and/or aluminum electrolytic capacitors.

Note that X5R multi-layer ceramic capacitors (MLCCs) offer high capacitance, but capacitance decreases significantly above 50% of rated voltage. Typical capacitance change of X7R capacitor versus DC voltage and temperature are shown in Figs. 5 and 6.

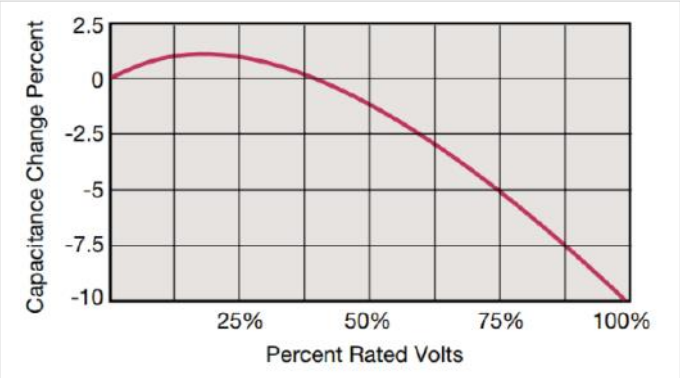



*Figure 5: Typical capacitance change of X7R capacitor vs. DC voltage*

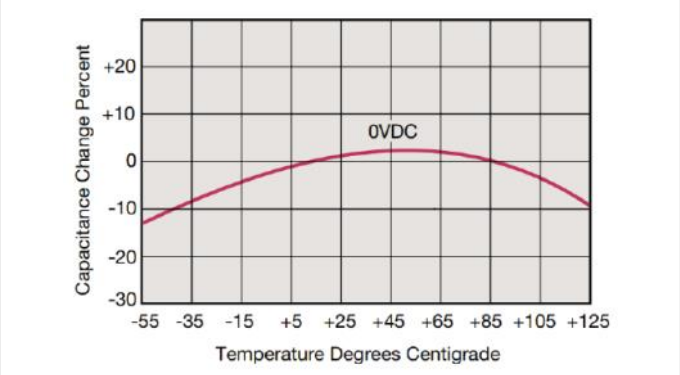



*Figure 6: Typical capacitance change of X7R capacitor vs. temperature*

As can be seen, the X7R capacitor varies only ±15% over the temperature range of -55 °C to 125 °C. Then it finds applications where stability over a wide temperature range is required. So X7R is a preferred dielectric due to its good temperature and voltage coefficients. MLCCs larger than 1210 should be avoided due to cracking issues and capacitor manufacturers' soldering and handling instructions should also be observed.

## The input DC bus with extra-low ripple and noise

Depending on the application, sometimes the designer's choice is to insert an inductor between the distributed bus and the input of a switching regulator to isolate noise from being coupled to other circuits on the board. In such cases, the best cost and space saving approach for decoupling is to use a filter with combination of a small inductor and capacitors, see Fig. 7.

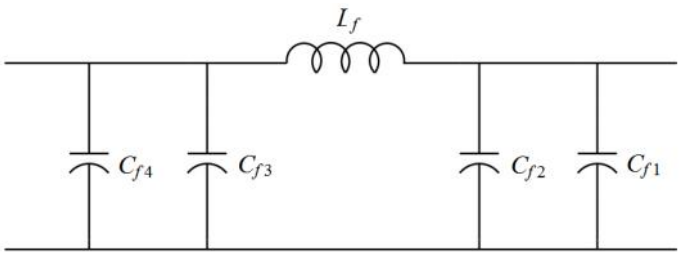



*Figure 7: Circuit diagram showing a filter with the combination of an inductor and capacitors*

The inductor in the filter circuit increases the source impedance of the input bus. The value of the inductor should be chosen in such a way that Equation (1) is satisfied. Appendix B explains how to choose and design the optimal input filter to have extra-low noise.

## Phase spreading

When multiple PoL regulators share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices have coincident rising edges. In order to enable phase spreading, all converters must be synchronized to the same switching clock. **Note** that Application Note AN309 provides information on how to synchronize the digital PoL regulators and use phase spreading for optimized performance.

In the phase spreading supply, the parallel regulators are switched at specific phase angles. The angles are evenly distributed so that a maximum ripple current cancellation can be achieved. A general equation for the input capacitor RMS current, $I_{Ci,RMS}$, can be approximated as:

$$I_{Ci,\mathrm{RMS}} = I_o \cdot \sqrt{\left(D - \frac{m}{N}\right) \cdot \left(\frac{m+1}{N} - D\right)} \quad \text{(E:8)}$$

where *m=floor(N*D)*. The *floor* function returns the greatest integer less than or equal to the input value, *N*D*, and *N* is the number of active phases.

Fig. 8 shows the normalized input ripple current RMS value over the load current versus duty cycle with different number of active phases.

As can be seen from Equation (8) and Fig. 8, the input ripple current cancellation is related to the number of phases and duty cycle. Greater ripple reduction is generally achieved with additional phases. Large ripple current will cause very high power dissipation in the input capacitors due to the capacitor ESR. The capacitor lifetime also will be reduced. In addition to the reduction of the input RMS current, the peak-to-peak current is also reduced due to interleaving.

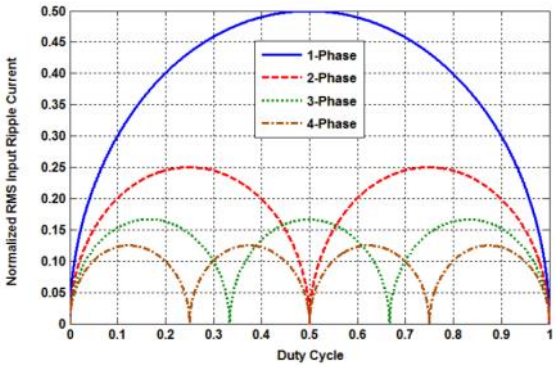



*Figure 8: Normalized RMS input ripple current vs duty cycle*

The switching current in the input capacitor is typically a large source of high frequency noise. With the reduced switching current amplitude, the current slew rate is reduced while providing the AC current to the high-side MOSFET. Hence, the noise is reduced. The input ripple frequency will also be higher than that of single-phase operation. The higher frequency makes the input filter smaller and less costly.

The required input capacitance to reduce the ripple voltage amplitude to an acceptable level with phase spreading is defined in Equation (9).

$$C_{i,\min} = \frac{I_o}{\Delta V_{i,pp} \cdot f_{sw}} \cdot \left( D - \frac{m}{N} \right) \cdot \left( \frac{m+1}{N} - D \right) \quad \text{(E:9)}$$

The $\Delta V_{i,pp}$ is the acceptable input voltage ripple contributed by the amount of input capacitance, of which is the input capacitors that filter most of pulsating currents.

The input voltage ripple induced by the ESR of the input capacitor, $ESR_i$, can be estimated with Equation (10).

$$\Delta V_{i,ESR} = \left( \frac{I_o}{N} + \frac{\Delta I_{pp}}{2} \right) \cdot ESR_i \quad \text{(E:10)}$$

As can be seen from Equation (9), phase spreading can dramatically reduce input capacitance requirements.

## Design examples

### Single-phase (standalone product)

Assume a BMR4630008/001 PoL product to analyze input voltage ripple. The BMR463 is a single-phase 25 A digital PoL product. It supports a wide range of output voltages (0.6 V to 3.3 V) operating from input voltages as low as 4.5 V up to 14 V. According to the Technical Specification of the BMR463 series, the product has 70 µF internal input capacitor and the efficiency of the product is almost η = 94% at $V_i$ = 12 V, $V_o$ = 3.3 V, $I_o$ = 25 A and $f_{sw}$ = 320 kHz.

It is assumed that the input filter should limit the peak-to-peak input voltage ripple to 1% of its DC value, i.e., $\Delta V_{i,pp}$ = 120 mV and allowable voltage deviation due to 50% output transient current is $\Delta V_{tr}$ = 100 mV.

This section shares a step-by-step guide to designing the input filter.

1. Calculate the duty cycle, D, of the PoL regulator:

$$\Delta V_{i,ESR} = \left( \frac{I_o}{N} + \frac{\Delta I_{pp}}{2} \right) \cdot ESR_i \quad \text{(E:11)}$$

2. Calculate the total input filter capacitance, $C_{i,min}$, needed based on the required peak-to-peak input voltage ripple, see Equation (3):

$$C_{i,\min} = I_o \cdot \frac{D \cdot (1-D)}{\Delta V_{i,pp} \cdot f_{sw}} = 134.74\ \mu\text{F} \quad \text{(E:12)}$$

Since the module has 70 µF internal capacitors, minimum required external ceramic input capacitance will be 64.74 µF. So three 22 µF X7R external MLCCs in parallel are added to the input filter in order to get about 1% peak-to-peak input voltage ripple. The spikes caused by the ESL of the input capacitors are decoupled with low ESL 100 nF ceramic capacitors.

3. Calculate capacitors' RMS current,$I_{Ci,RMS}$, by Equation (5) or FPD phase spreading function

$$I_{Ci,\text{RMS}} = I_o \cdot \sqrt{D \cdot (1-D)} = 11.37\ \text{A} \quad \text{(E:13)}$$

The distribution of the input RMS current on each single capacitor depends on component characteristics and module design. The ripple current is assumed to divide between capacitors in proportion to their capacitance. So the RMS current through one of the three 22 µF MLCCs will approximately be 1.84 A (11.37 A * 22 µF / 136 µF). In the data sheet, the capacitor manufacturer specifies the maximum RMS current through that capacitor as 4.55 A which is above the calculated value.

Therefore, there should be no problem with the ripple current flowing through the capacitors.

4. Calculate the minimum required input bulk capacitance, $C_{i,tr,min}$, to determine 100 mV voltage deviation due to 50% load transient, see Equations (6) and (7):

$$\Delta I_i = \frac{V_o}{V_i \cdot \eta} \cdot \Delta I_o = 3.657\ \text{A} \quad \text{(E:14)}$$

(E:15)

$$C_{i,tr,\min} = \frac{1.21 \cdot (\Delta I_i)^2 \cdot L_{ftotal}}{(\Delta V_{tr})^2} = \frac{1.21 \cdot (\Delta I_i)^2 \cdot (L_f + L_{src})}{(\Delta V_{tr})^2} = 80.91\,\mu\text{F}$$

It is assumed that there is no series filter inductor and a value of 50 nH is used for $L_{src}$ in the calculation to account for stray inductance in the input supply path. According to the calculation we need 80.91 µF of bulk capacitance as a minimum. We would use the standard value of 180 µF. Use low ESR capacitors to implement the bulk network. Capacitors with high ESR induce voltage drops of their own due to the current flowing in them. Care must be taken when using very low ESR capacitors together with an input inductor as it may cause instability.

5. Check stability of the system.

The minimum input impedance of the PoL, $Z_{i,POL,min}$, under the above operating conditions can be calculated using Equation (2).

The peak output impedance of the input filter, $Z_{o,max}$, is

It's obvious that $Z_{i,POL} >> Z_{o,max}$, so stability of the system is guaranteed.

$$Z_{i,\mathrm{POL,min}} = \frac{V_i^2}{\eta \cdot V_o \cdot I_o} = 1.857\,\Omega \qquad \text{(E:16)}$$

$$Z_{o,\max} = \sqrt{\frac{L_{ftotal}}{C_{ftotal}}} = \sqrt{\frac{L_f + L_{src}}{C_{i,\mathrm{int}} + C_{i,\mathrm{ext}}}} = \sqrt{\frac{0+50}{70+(66+180)}} = 0.0126\,\Omega \qquad \text{(E:17)}$$

## Simulation results

The simulated input ripple waveforms at $V_i$ = 12 V, $V_o$ = 3.3 V and $I_o$ = 25 A are shown in Figs. 10 and 11. The simulation indicates a ripple voltage of the module is about 103 $mV_{p-p}$ which is below 1% of the input DC bus due to adding a 180 µF bulk capacitor. The peak to peak input ripple current is about 1 A. If reflected current ripple is a concern, use a small input inductor. This is the single most effective way to confine ripple currents to the local input bypass capacitors. An input inductor can reduce the reflected ripple current by an order of magnitude. A single input inductor can be shared by multiple PoL modules.

For example, if a 250 nH inductor is used as an input inductor in this example, the input current ripple is reduced to about 150 mA.

Note that simulation model also helps to plot impedance curves and calculate the RMS current flowing in each capacitor.

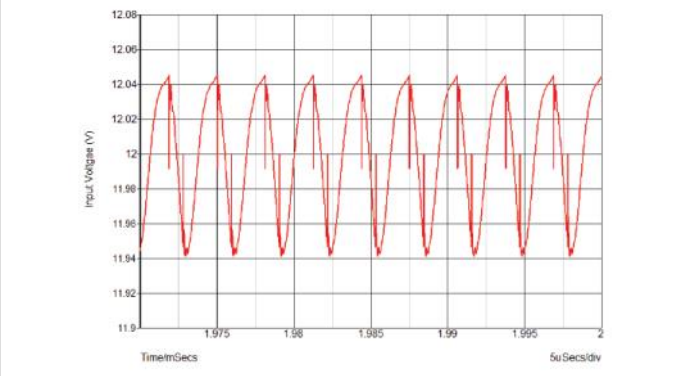



*Figure 10: Input voltage ripple for single-phase standalone module at $V_i$= 12 V, $V_o$ = 3.3 V and $I_o$ = 25 A*

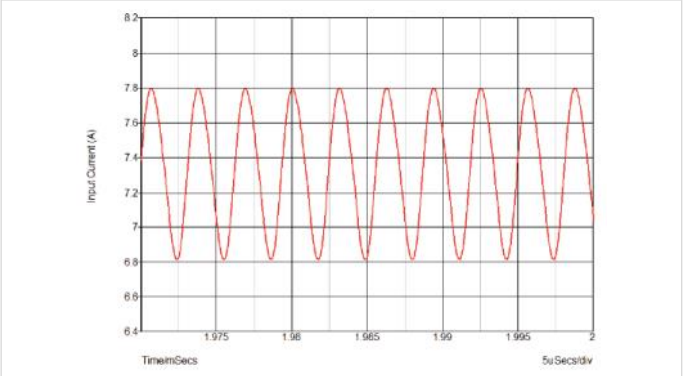



*Figure 11: Input current ripple for single-phase standalone module at $V_i$ = 12 V, $V_o$ = 3.3 V and $I_o$ = 25 A*

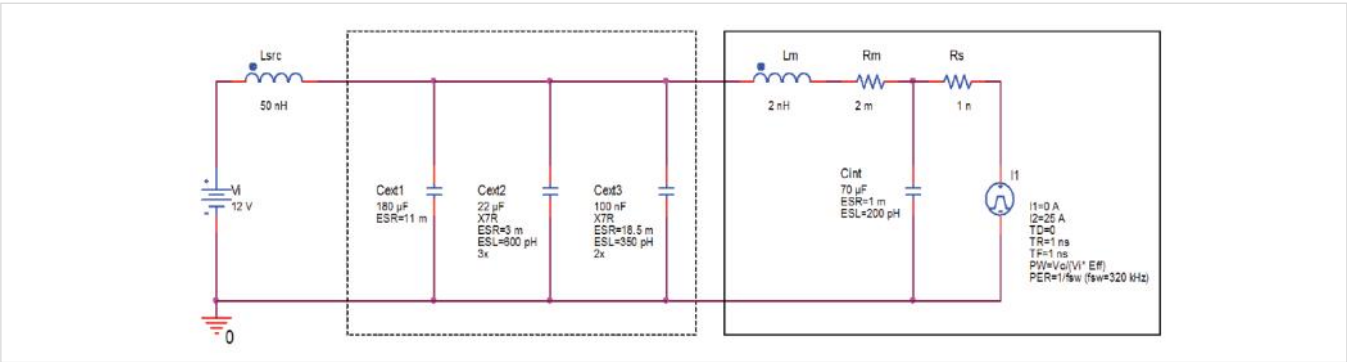



*Figure 9: PSpice simulation model for single-phase BMR463 PoL*

## Two-phase system (paralleled products)

Assume two BMR4630008/001 PoL modules are working in a current sharing group. It is also assumed that input filter should limit the peak-to-peak input voltage ripple to 0.5% of its DC value, i.e., $\Delta V_{i,pp}$ = 60 mV and allowable voltage deviation due to 50% output transient current is $\Delta V_{tr}$ = 100 mV at $V_i$ = 12 V and $V_o$ = 3.3 V and $I_o$ = 50 A and $f_{sw}$ = 320 kHz. Note that N = 2 and m = 0.

1. Calculate the total input filter capacitance needed based on the required peak-to-

$$C_i = I_o \cdot \frac{D \cdot (0.5 - D)}{\Delta V_{i,pp} \cdot f_{sw}} = 158.05\,\mu F \quad \text{(E:18)}$$

peak input voltage ripple, see Equation (9):

Since the system has 140 µF internal capacitors, minimum required external ceramic input capacitance will be 18.05 µF. Then only one 22 µF X7R ceramic capacitor is added to the input filter.

2. Calculate capacitor's RMS current by Equation (8) or FPD phase spreading function

3. Calculate the minimum required bulk capacitance to

$$I_{Ci,RMS} = I_o \cdot \sqrt{D \cdot (0.5 - D)} = 12.32\,A \quad \text{(E:19)}$$

determine $\Delta V_{tr}$ = 100 mV voltage deviation due to load transient, see Equations (6) and (7):

$$\Delta I_i = \frac{V_o}{V_i \cdot \eta} \cdot \Delta I_o = 7.314\,A \quad \text{(E:20)}$$

$$C_{i,tr} = \frac{1.21 \cdot (\Delta I_i)^2 \cdot L_{ftotal}}{(\Delta V_{tr})^2} = \frac{1.21 \cdot (\Delta I_i)^2 \cdot (L_f + L_{src})}{(\Delta V_{tr})^2} = 323.63\,\mu F \quad \text{(E:21)}$$

A value of 50 nH is used for $L_{src}$ in the calculation like the single-phase operation. According to the calculation, minimum required bulk capacitance is 323.63 µF. We would use the nearest standard value of 470 µF.

### Simulation results

PSpice simulation model of the system is shown in Fig. 14. The simulated input ripple waveforms at $V_i$ = 12 V, $V_o$ = 3.3 V and full load are plotted in Figs. 12 and 13. is about 50 $mV_{p-p}$ which is below 0.5% of the input voltage due to adding a 470 µF bulk capacitor. The peak to peak input ripple current is about 150 mA. The calculations show that by reducing the ripple voltage amplitude the ripple current will be reduced substantially. With interleaving, the input ripple frequency will be twice higher than that of single-phase operation as expected.

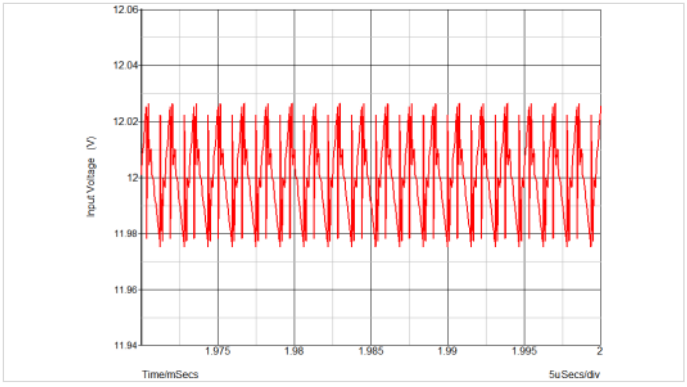



*Figure 12: Input voltage ripple for dual-phase operation at $V_i$ = 12 V, $V_o$ = 3.3 V and $I_o$ = 50 A.*

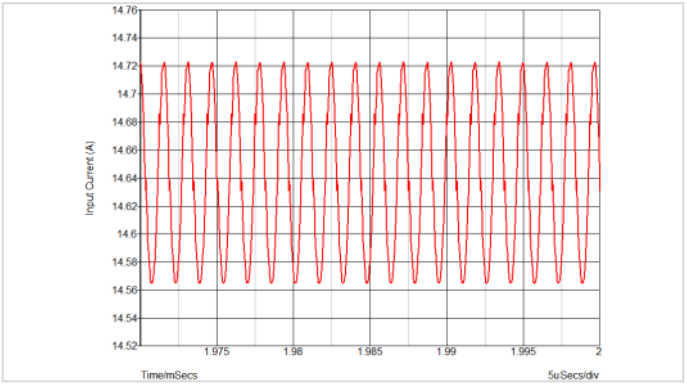



*Figure 13: Input current ripple for dual-phase operation at $V_i$ = 12 V, $V_o$ = 3.3 V and $I_o$ = 50 A*

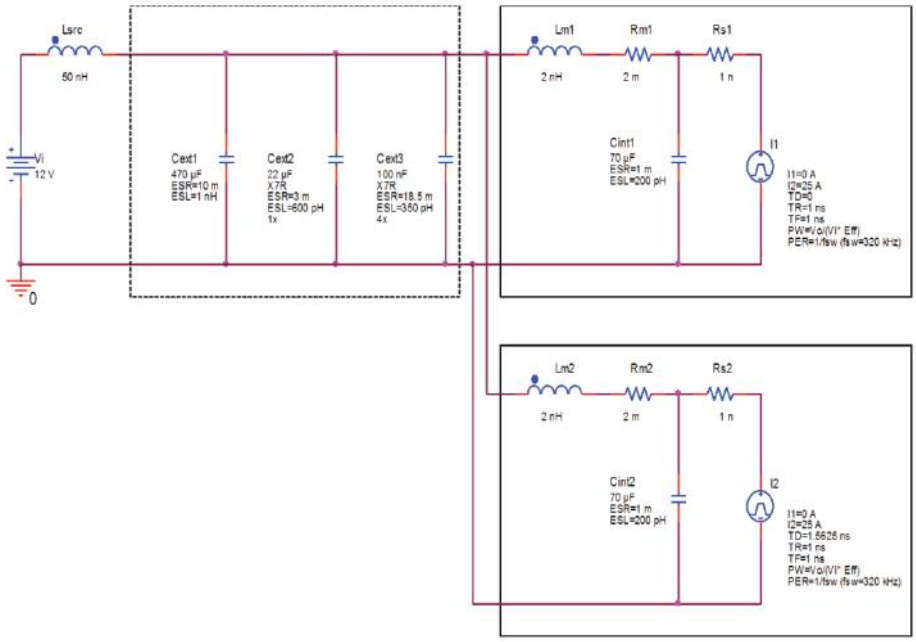



*Figure 14: PSpice simulation model for dual-phase BMR463 PoL*

# Appendices

## Appendix A - input impedance of a buck converter

Equation (22) permits calculation of the input impedance of a buck converter, $Z_{i,buck}$, operating in continuous conduction mode at any particular frequency *f*. It is assumed that the load of the converter is resistive, where DCR is DC resistance of an inductor L, $R_L$ is resistive load and w = 2πf.

(E:22)

$$Z_{i,\text{buck}} = \frac{-1}{D^2} \cdot \left( \left[ \frac{R_L}{1+(\omega \cdot R_L \cdot C_o)^2} + DCR \right] + j\omega \left[ L - \frac{R_L^2 \cdot C_o}{1+(\omega \cdot R_L \cdot C_o)^2} \right] \right)$$

## Appendix B – LC filter design

As said in Section (4), the combination of a small inductor and capacitors is used to reduce noise proliferation across the board; however it reduces effectiveness of synchronization and phase spreading in reducing of ripple current stress to local capacitors and also might require increase in a total amount of bulk capacitors.

### Undamped LC filter

The first simple filter solution is an undamped LC passive filter shown in Fig. 15. It can be seen that impedance of the filter is given by parallel combination of the inductor and the capacitor. Construction of the Bode diagram of this parallel resonant circuit says that the magnitude is dominated by the inductor impedance at low frequency and by the capacitor impedance at high frequency. The inductor and capacitor asymptotes intersect at the filter resonance (cut-off) frequency, $f_0$.

Since the input filter is undamped, its Q-factor, QF, is ideally infinite. In practice, parasitic elements such as inductor loss and capacitor ESR limit the value of QF. Nonetheless, the impedance is very large close to the filter resonant frequency $f_0$.

$$f_0 = \frac{1}{2\pi\sqrt{L_f \cdot C_f}} \qquad \text{(E:23)}$$

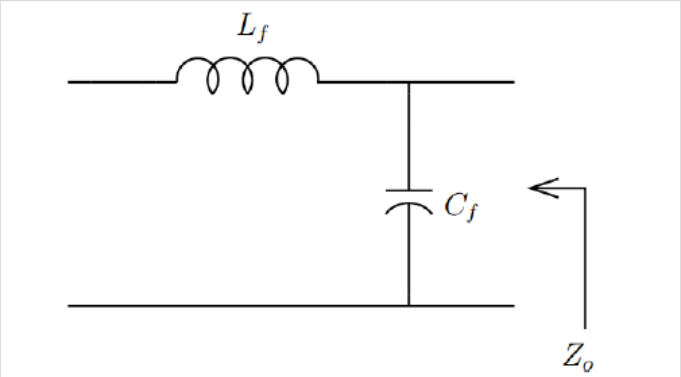



*Figure 15: Undamped LC filter*

Since the input filter is undamped, it is impossible to satisfy the Equation (1) close to the input filter cut-off frequency $f_0$. Regardless of the choice of element values, the input filter changes transfer function of the feedback control loop in the vicinity of frequency $f_0$ and causes some oscillations at the regulator.

To meet the noise filtering requirements the input filter has to have the cut-off frequency $f_0$ around one decade below the bandwidth of the feedback loop of the PoL regulator.

### Damped LC filter

The resonance of the input filter has to be damped so that Equation (1) is satisfied at all frequencies. Fig. 16 shows a damped filter made with a resistor $R_d$ in series with a capacitor $C_d$, all connected in parallel with the filter's capacitor $C_f$. The purpose of resistor $R_d$ is to reduce the output peak impedance of the filter at the cut-off frequency. The capacitor $C_d$ blocks the DC component of the input voltage and avoids the power dissipation on $R_d$. The capacitor $C_d$ should have lower impedance than $R_d$ at the resonant frequency and be a bigger value than the filter capacitor in order not to affect the cut-off point of the main filter.

The optimum damping resistance value, $R_d$, and DC blocking capacitor, $C_d$, can be approximated as

$$R_d = \sqrt{\frac{L_f}{C_f}} \;\&\; C_d = 4 \cdot C_f \qquad \text{(E:24)}$$

**Note** that for the damping block ($C_d$ and $R_d$), a capacitor with ESR = $R_d$ and C ≥ $C_d$ can be a good choice.

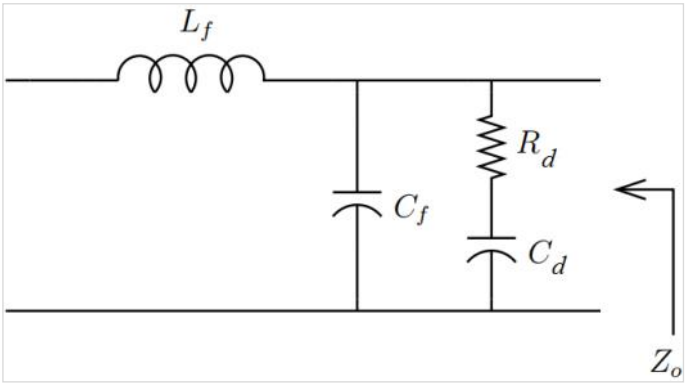



*Figure 16: Damped filter*

### Multi-stage LC filter

Most of the time, a multi-stage filter allows higher attenuation at high frequencies with less volume and cost, because if the number of single components is increased, it allows the use of smaller inductance and capacitance values, see Fig. 17. Filter inductors should be designed to reduce parasitic capacitance as much as possible, the input and output leads should be kept as far apart as possible and single layer or banked windings are preferred.

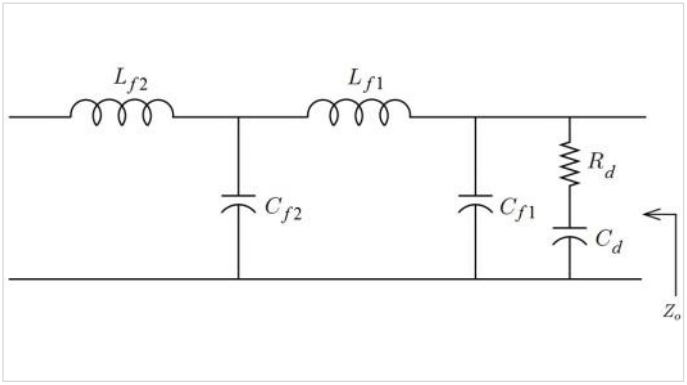



*Figure 17: Two stage input filter*

Flex Power Modules

Flex Power Modules, a business line of Flex, is a leading manufacturer and solution provider of scalable DC/DC power converters primarily serving the data processing, communications, industrial and transportation markets. Offering a wide range of both isolated and non-isolated solutions, its digitally-enabled DC/DC converters include PMBus compatibility supported by the powerful Flex Power Designer.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