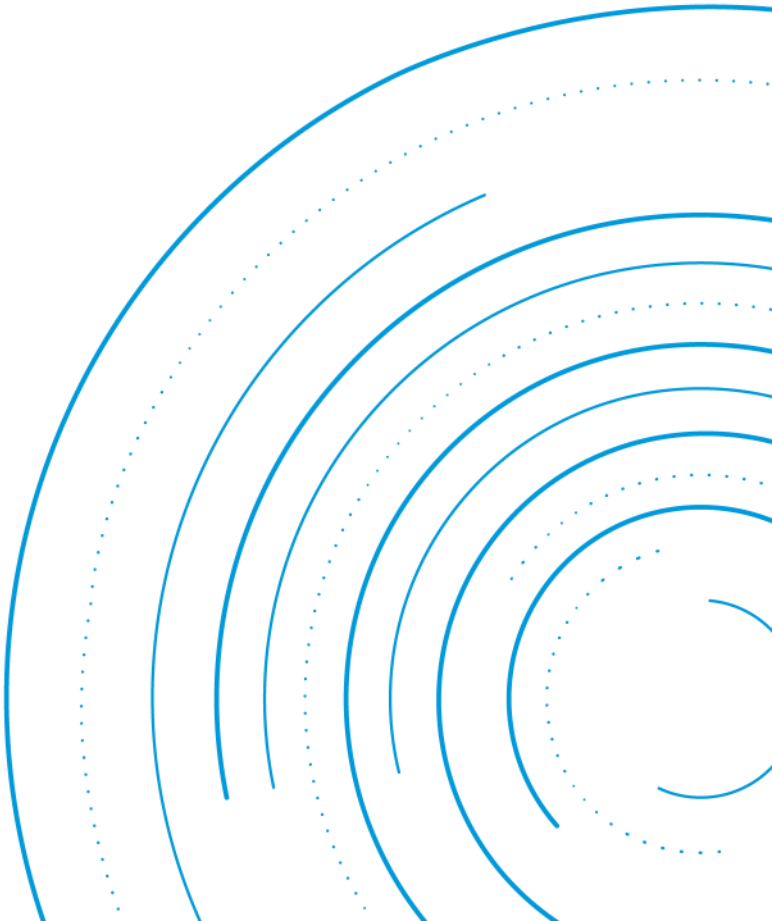
flex Power Modules

APPLICATION NOTE 324

Parallel operation with Droop Load Sharing (DLS)



Abstract

The BMR458, BMR480, BMR490 and BMR491 offer load sharing capabilities allowing multiple products to be connected in parallel. This feature is typically used to increase power output on the same rail, providing redundancy against a product failure, or distribute thermal heat over a larger board area. Paralleling may also help in streamlining your Bill of Materials by replacing the need for separate products with higher power requirements .

Contents

Introduction

This Application Note describes parallel operation and load sharing of BMR458, BMR480, BMR490 and BMR491 products. It also describes the design considerations to be made in order to optimize the current sharing for maximum output power. Finally, the steps are presented how to perform current sharing PMBus configurations in Flex Power Designer.

These products offer two types of paralleling modes: Passive current sharing which is also known as Droop Load Share (DLS), and Active Current Share (ACS).

In this application note, the DLS mode is described.

BMR458 xxxx/017, BMR458 xxxx/018, BMR458xxxx/019, BMR458 xxxx/020, BMR480x100/017, BMR491x511/858, BMR491xx06/855 and BMR491xx03/851 are pre-configured variants for DLS operation.

For definitions & specifications, see Technical Specification for these products.

Current sharing modes

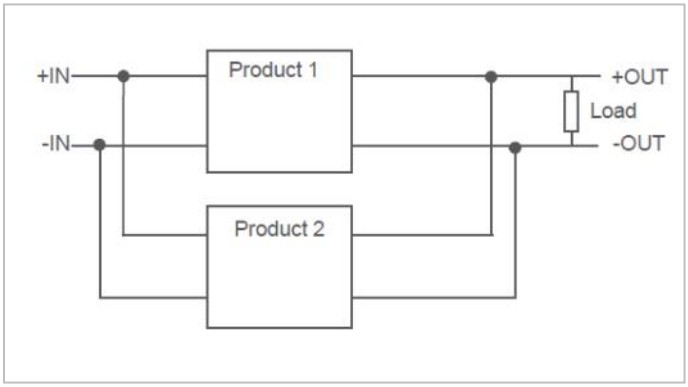
BMR458, BMR480, BMR490 and BMR491 platforms offer two major types of current sharing modes. One mode is passive, also known as Droop Load Share (DLS). The second mode is Active Current Sharing (ACS).

The DLS mode, design considerations and flow are further described in the following sections.
In Pictures 1 and 2 DLS is illustrated.

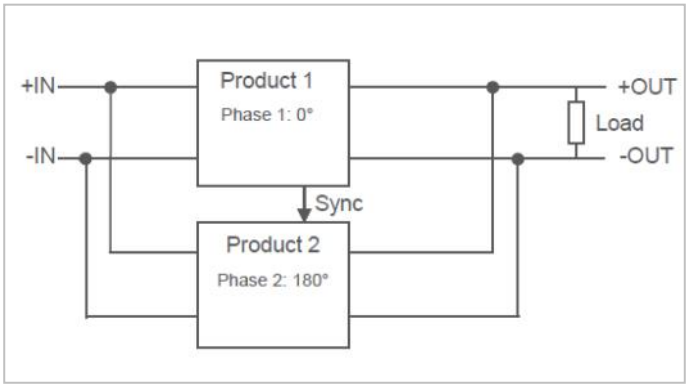
The ACS mode is illustrated in Pictures 3 and 4. The ACS mode is however not further described in this application note.

In order to prepare for a future DLS-to-ACS transition in your application, the same routing as for a DLS mode application can be used. Since ACS requires Current Share signals (CONTROL pins) to be connected to all current sharing products, the application board must be prepared for this.

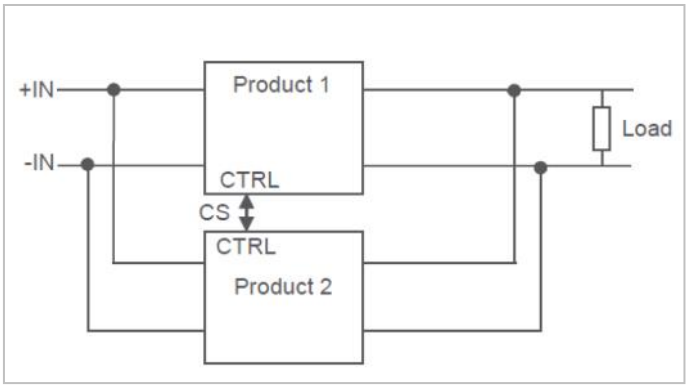
Note: Dynamic bus voltage (DBV), dynamic load compensation (DLC) and adaptive ramp-up time (ART) functionality must be disabled in all Current Sharing modes. In addition, it is not recommended to use Hybrid Regulated Ratio (HRR) functionality for devices operating in parallel configuration.



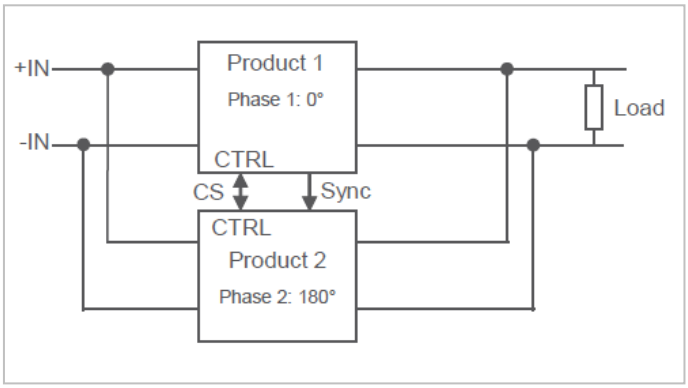
Picture 1: Current sharing mode 1a: DLS without synchronization



Picture 2: Current sharing mode 1b: DLS with synchronization



Picture 3: Current sharing mode 2a: ACS without synchronization



Picture 4: Current sharing mode 2b: ACS with synchronization

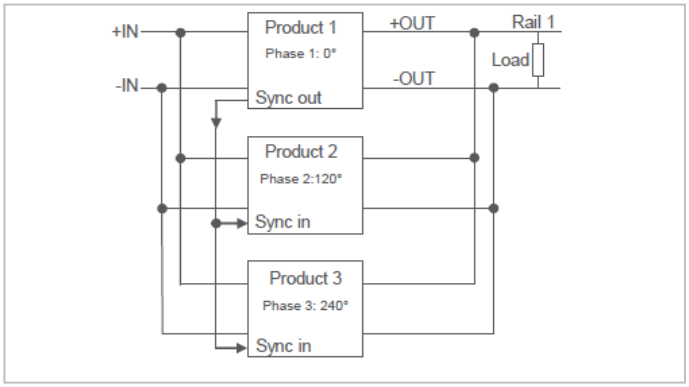
Droop Load Sharing

For DLS there is no difference between the current sharing products' configurations: All DLS products shall be configured in the same way and the external components shall be the same as well.

Note: If synchronization is used, then one of the devices must be configured for sync-out, whereas the rest of the current sharing products must be configured for sync-in. Also, the INTERLEAVE PMBus command shall be used to achieve phase spreading. This will minimize the input current/voltage ripple.

In Picture 5, a typical current sharing case with three pieces of suitable products are paralleled to deliver its power to Rail 1.

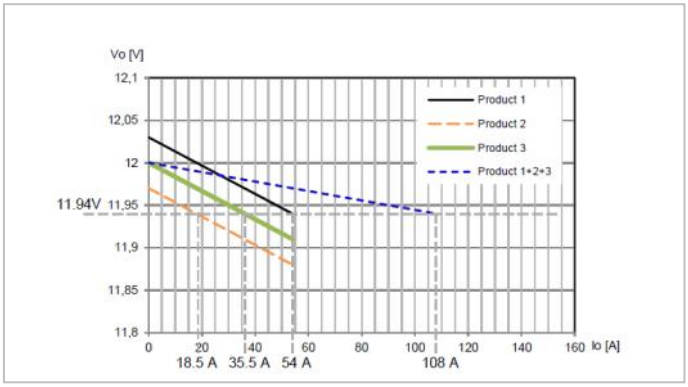
Understanding Droop



Picture 5: Example of a three-phase current sharing group. Note: The SYNC signal connection is optional.

In most load-sharing applications there needs to be a way for the individual phases to share the load in proportion to their capacity. Ideally, the voltages across phases would operate at exactly the same voltage at all times. In practice though, manufacturing variations and the board design can lead to small differences in the actual output voltage. These small differences, when applied to regulators operating in parallel, creates current loss where one product with a higher voltage is supplying current to the other product(s).

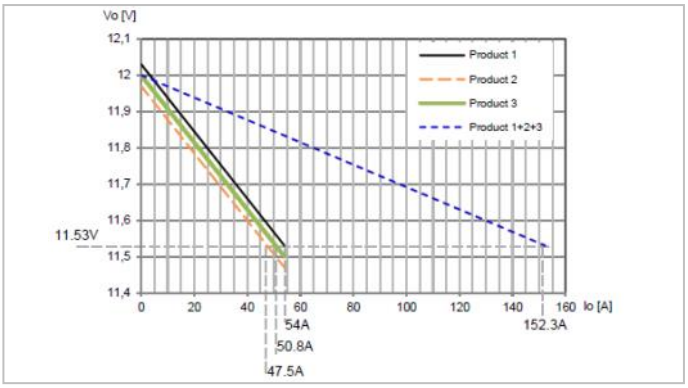
Assume the setup-of three BMR458 54A products in parallel as shown in Picture 5. Now also assume the situation as shown in Picture 6. It shows a simple example where all BMR458 products have small output voltage differences: 12.03V, 12.00V and 11.97V respectively.
Note: When the products are connected in parallel, they will share the same output voltage.



Picture 6: Poor usage of the output current from three products with 12V output voltage initial setting tolerances, equal output resistance, and VOUT_DROOP set to 90 mV. Maximum total current is only 108 A in this case

If we assume that the products have the same droop settings, 90 mV over the whole output current range is assumed, and the mother board have zero (or the same) wire resistances to the Rail 1 node from each output, the BMR458 product with the highest output voltage level will deliver maximum current, whereas the other two products deliver only 35.5A and 18.5 A respectively. In Picture 6, it is seen that the maximum total current will not be 3 x 54A = 162 A, but 18.5 A + 35.5A + 54A = 108A. The maximum power is then 11.94V x 108A = 1289W . Hence, only 66% of the maximum theoretical power can be delivered in this case.

If the output voltage variation can be accepted to increase, the droop can be increased to increase the maximum power delivered. A 500 mV droop is illustrated in Picture 7. As seen, the maximum current delivered is now 54A + 50.8A + 47.5A = 152.3A. Compared to 90 mV droop, the maximum power has increased from 1289W to 11.53V x 152.3A = 1756W.

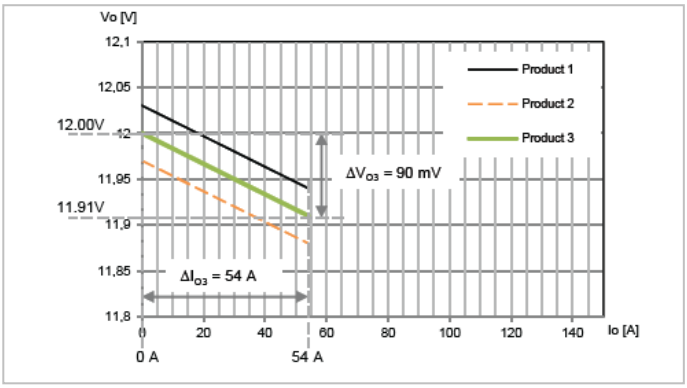


Picture 7: Improved maximum output current from three products with 12V output voltage initial setting tolerances. equal output resistance, and VOUT_DROOP set to 500 mV. Maximum total current is increased to 152.3 A due to a larger droop

As seen in the pictures 6 and 7 passive current sharing is achieved by having a droop load share (DLS), i.e. the output voltage of the product will decrease when the load current is increased.

Modelling of Droop

The droop can also be expressed as an output resistance of the product, as demonstrated below.



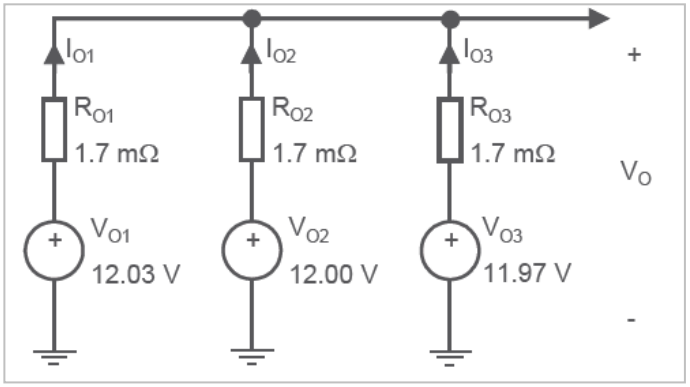
Picture 8: Three parallel BMR458—calculation of output resistance R_O

In picture 8 (same example as in picture6), all three BMR458 products have the same output resistance, $R_O = R_{O1} = R_{O2} = R_{O3}$, since the slopes are constant and parallel.

$$R_O = C_O \frac{\Delta V_{O3}}{\Delta I_{O3}} = \frac{12.00 - 11.91\ V}{54 - 0\ A} = \frac{90\ mV}{54\ A} \approx 1.7\ m\Omega$$

Equation 1

R_O can be estimated directly from picture 8 by, using for example, product 3 as shown in *Equation 1:*



Picture 9: A simplified model of 3 BMR458 in parallel

A simplified schematic representation of this DLS example with three BMR458 products can be expressed as in picture 9.

DLS in Different Operation States

Steady State

Difference in output voltage initial setting (V_o at 0A), output resistance and difference in output resistance are the parameters that defines the current sharing accuracy. The long-term drift is negligible.

If the droop is very low, the products will not share current well due to different initial voltage setting. A too high droop on the other hand will make current sharing well but limit the available output power. The droop should be chosen such that the available output power for parallel products is optimized.

Since the output currents of paralleled products are not identical, one of the products will reach max current before the other, therefore the expected total output current is less than twice the output current of a single product. In practice the maximum output current could also be limited by the maximum allowed operating temperature of the warmest product.

Turn-On

In addition to the parameters already listed in the Steady State section, the level of differences in delay and ramp-up times defines the current sharing accuracy during turn-on.

The maximum load at start-up is also affected by the output capacitance, C_O. To keep the limit of the maximum output current during ramp-up as high as possible it is recommended to set the output voltage ramp-up time, t_r, to 200 ms: The current into the external capacitor. I_{CO}, during ramp-up can be calculated as in *Equation 2,* assuming $\Delta Vo = Vo = 12V$ and $t_r = 200$ ms

$$I_{CO} = C_O \cdot \frac{\Delta V_O}{\Delta t_r} = C_O \cdot \frac{12\ V}{200\ ms} = C_O \cdot 60\ [A]$$

Equation 2

Now, with an output capacitance of for example 10 mF, the current into the output capacitance during ramp-up is as low as 0.6A. Therefore, the maximum available output load current during start-up will be reduced by only 0.6A. Instead, if the ramp-up time is set to 20 ms, the maximum available output load current during start-up will be reduced by 6A.

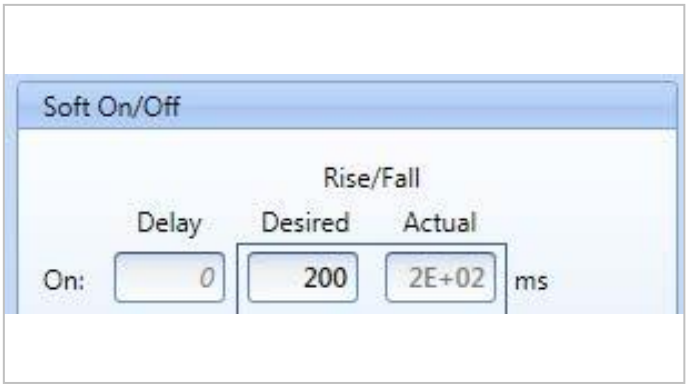
Note, a slow ramp is also beneficial for the current sharing balance during ramp-up.

Also note that a start-up of parallel products with slow ramp-up time (i.e. slow slew rate) on the input voltage, can cause one product to start before the other due to different turn-on voltages. The available output current during the time of single product operation will then be reduced to the single product rating.

When using the Flex Power Designer, the recommended turn-on time settings (TON_RISE) will be presented by default, see picture 10.

Pre-bias

No special configuration for a current sharing group of BMR458 is needed for taking care of pre-bias.



Picture 10: Turn-on settings in Flex Power Designer

Turn-Off

In DLS operation the products shall be configured for *Immediate Off* (CONTROL pin) and *Quick Off* (RC pin).

Load Transient Response/Output capacitance

A proper load transient response for a parallel group of products requires the control loop parameters to be adjusted (This is however not needed for products that are pre-configured for DLS operation). Therefore, the current sharing products' control loop parameters shall be set to a verified loop compensation filter using PMBus command MFR_FILTER_COEFF (0xE8). For further details about which loop compensation filter for use in DLS mode, see Appendix. You should design for the same amount of output capacitance for a member in a parallel group as you do for a single module.

Input Ripple/Input Capacitance

The input voltage/current ripple design for a parallel group of products can be designed as they were all single.

General

BMR458, BMR480, BMR490 and BMR491 are verified with up to six parallel products. In the next section, DLS current sharing will be further described.

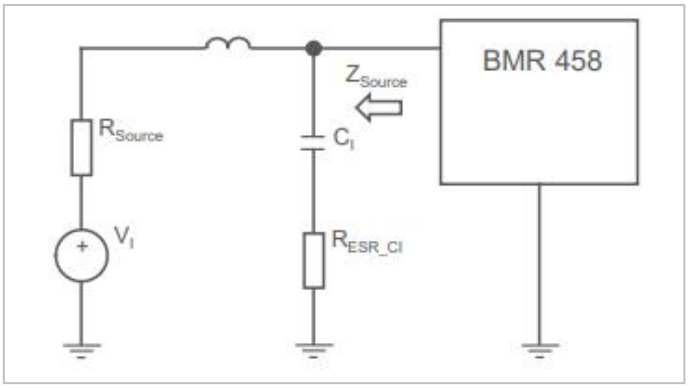
Design Considerations

Layout and cooling

You shall connect the outputs together as close to the load as possible. Never connect diodes or other current blocking devices between the inputs of paralleled products and keep the resistance and inductance between the inputs as low as possible. The product also uses its pins for cooling by transferring heat to the mother board. For efficient heat transfer, it is recommended that the pins are connected to copper planes in the mother board. For best current sharing performance, i.e. for minimizing the output current differences between the current sharing products, it is important to have the same thermal situation for all products. For an air-cooled application, the air flow shall be the same for all current sharing products.

Input capacitance

The recommended input capacitance, C_I , is found in the Technical Specifications of each product and it should be placed close to the input of each product. If an external input filter is used, the recommended peak source impedance seen at the input of each product, Z_{source_peak}, shall be below the module's input impedance (for example below 2 Ω per product for BMR458). Otherwise input oscillations may occur at start-up, or at a high output current transients. The source resistance, R_{source} should be checked to avoid the under-voltage lockout being activated. For example, for the BMR458 the source resistance should be less than 100 mΩ per product to avoid the under voltage lockout being activated. So, for two parallel products, R_{source} should be less than 50 mΩ and Z_{source_peak} should be below 1 Ω.



Picture 11: Source resistance, R_{source}, source impedance seen at the input at each product, Z_{source}, and the external input capacitance, C_{IN}. and its ESR, R_{ESR_CIN}

Output capacitance

he output capacitors of ceramic type should be placed close to the load for efficient decoupling and also to reduce the Q-value of the output filter. As stated earlier, the Flex Power Designer software supports the design of both the output filter for current sharing products. You can read more about the theory of *Output Filter Design and Loop Compensation in TP022*.

Current balance

The actual current supplied by each module in a sharing group in steady state will not always be equal due to the current monitoring accuracy. The current monitoring accuracy (see Technical Specification for each product) in turn will depend on the trimming of each device in production as well as varying with operating conditions such as input voltage, output voltage and temperature. The products have been designed to operate up-to the products rated output current.
This means that the maximum output current from the current sharing group will be limited to the product delivering the highest current, which is also the product having the highest output voltage.

Also, the current monitoring accuracy should be taken into account when considering the thermal operating conditions of a current sharing group. By using the Flex Power Designer (presented in next chapter) the current balance can be optimized for your specific application.

Synchronization

The DLS current sharing products do not need any synchronization for proper operation. However, by using syncronization and the INTERLEAVE command the phases of the products can be spread. This in turn can be used for reducing the input filter and/or reducing the input ripple (see Input Capacitance section above). The Technical Specifications should be checked to understand what pin(s) can be configured for synchronization. For example, in BMR458 either pin 9 or 12 can be configured for synchronization.

Fault handling and phase add/drop

If one or more devices in a DLS current sharing group fault the remaining devices will continue to operate, unless an overcurrent situation is created resulting in an OCP fault event. Phases can be added or dropped on the fly using RC pin, CONTROL pin or with the OPERATION command. **Note:** during turn-on/ramp-up, neither phase adding nor dropping is allowed.

Beat frequency

When paralleling a beat frequency can be noticed on the output. This is due to slightly different switching frequencies between the products. If the beat frequency is a problem, then synchronization can be used. By using synchronization the beat frequency can be significantly reduced.

Paralleling with Flex Power Designer

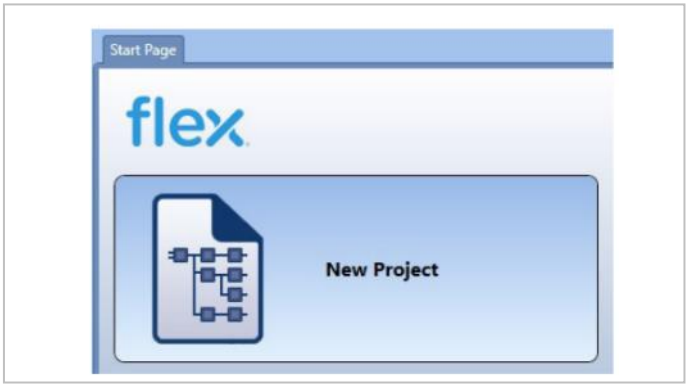
Introduction

Paralleling of products requires setting up a number of PMBus commands. While this can be done manually by setting individual commands, it is significantly easier to use the Flex Power Designer software to quickly create parallel rails. The software is available for download at flexpowerdesigner.com. The information below explains how to create a BMR458 DLS rail using the Flex Power Designer. The same walkthrough can be used for the BMR480 , BMR490 and BMR491.

Creating a parallel rail

This section walks through creating a BMR458 DLS parallel rail using the Flex Power Designer. No hardware is required, but this walkthrough project can be loaded onto two BMR458s using, for example, the BMR458 paralleling reference board (ROA 170 87).

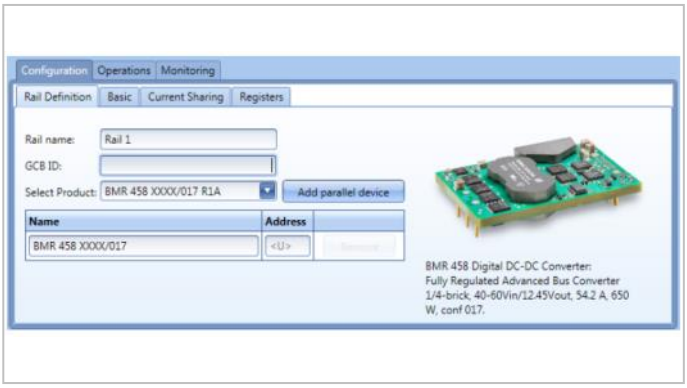
Step 1. Open the Flex Power Designer and create a new project.



Picture 12: Creating a project

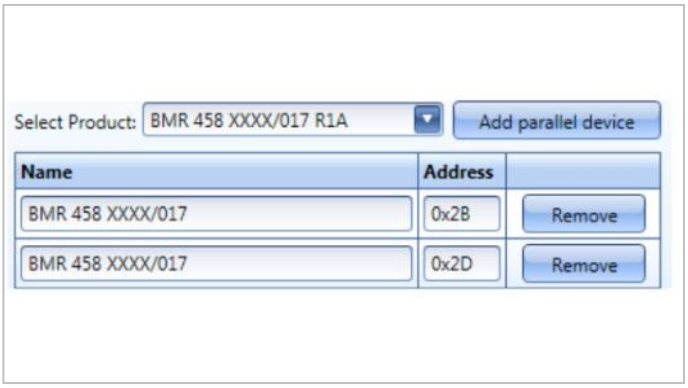
Picture 13: Adding a rail with BMR458

Step 2. Add a parallel rail and member phases. First, expand the BMR458 list and then left-click on the product you need in the Available Products list. After adding the rail, add the requested phases: Click the *Add Parallel device* button to add one phase.



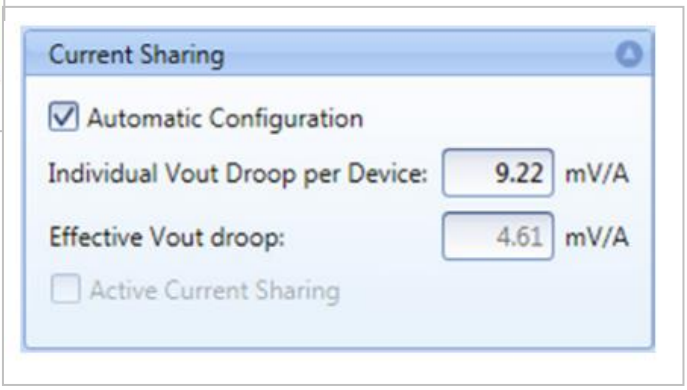
Picture 14: Adding parallel phases with the 'add paralle device' button

In this example, add another phase and then set the addresses of the two phases to 0x2B and 0x2D, as shown in picture 15. After adding the parallel devices, your rails configuration should look as shown in picture 15.



Picture 14: Adding parallel phases with the 'add paralle device' button

Step 3. Now, when the parallel rail is defined we just need to configure its droop settings. Go to the *Current Sharing* tab and make the necessary settings. In this case 9.22 mV/A droop is configured. Please note by default the tool gives you an optimum value.



Picture 16: Current sharing droop settings

Step 4. If synchronization is used, then make your manual synchronization settings using the MFR_MULTI_PIN_CONFIG and INTERLEAVE PMBus registers.
Note: The Flex Power Designer will select pin 9 (SA1_Sync) pin to be the SYNC pin by default. If you prefer to use pin 12 (PG_Sync) as SYNC pin, you make the change in MFR_MULTI_PIN_CONFIG PMBus register.

Step 5. Optional settings are preferably made in the Basic view.

Step 6. If you are going through this walkthrough with a BMR458 reference board (ROA 170 87), you can now load the project onto the BMR458 devices. Connect the USB-PMBus adapter (KEP91017) to the board. After the board is powered and connected, check that the PMBus addresses are correct and ensure that the RC switch is off before loading configuration. To load the project configuration to devices, use the Write Project to RAM & Store to NVM button in the Flex Power Designer toolbar.

A full explanation of both automatically and manually set commands is provided in the Appendix.

Appendix

Note: The following design flow is explicitly for current sharing operation additions. Hence, it assumed that the products are configured with correct hardware (as for example input and output filter capacitors) and with correct PMBus settings (for example Vout adjustments).
Note: FPD is short for Flex Power Designer.

Design Flow (DLS)

1. PMBus Configuration for BMR458 DLS operation (This is handled automatically in FPD as soon as current sharing is activated)

MFR_SPECIAL_OPTIONS (0xE0)
Set value to 0x20
(Non-linear droop DLC/ART disabled DBV disabled)
VOUT_DROOP (0x28)
Set value to 9.22 mV/A.
(This value is derived from 500 mV/54 A.)
MFR_ADDED_DROOP_DURING_ RAMP(0xFC)
Set value to 10 mW.(min. is 0 mW)
IOUT_OC_FAULT_RESPONSE (0x47)
Default value: 0x81 (Disable and Do not retry, 2 ms delay before disable)
MFR_RESPONSE_UNIT_CFG (0xD2)
Default value, bit 3:2 = 00 (1 ms range)
TON_RISE (0x61)
Set value to 200 ms (min. is 25 ms)
ON_OFF_CONFIG (0x02)
Set bit 0 to 0 (Immediate Off)
MFR_REMOTE_CTRL (0xE3)
Set bit 0 to 0 (Quick Off)
MFR_FILTER_COEFF (0xE8)
Set value to "DLS"*
* Using FPD:
0x01B60267FF00000000550355030000000180018000
00035013501
Using SMBus Tool:
013501350000000180018000000000355035500000000F
F6702B601

2. Synchronisation settings (This is performed manually in FPD Register view)

If Synchronization is selected, the following additional configurations shall be made

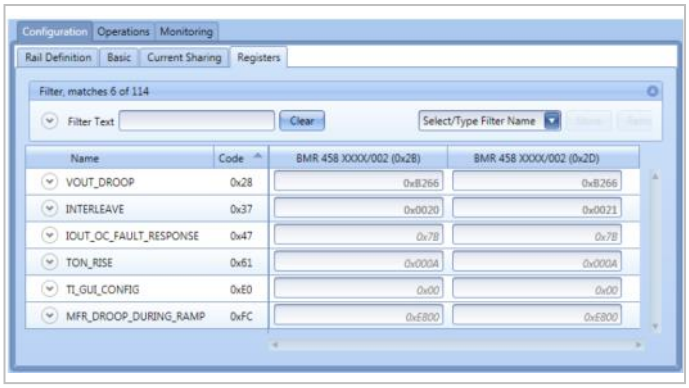
MFR_MULTI_PIN_CONFIG (0xF9)
"Sync out":
Set bit 6:5 to 10 (Sync out)
"Sync in"
Set bit 6:5 to 01 (Sync in)
"Sync out" and "Sync in":

Set bit 3 to 1
(pin 9 -->SYNC pin)
INTERLEAVE (0x37)
Main idea: Spread phases evenly
"Sync out":
Set value as first member in the current sharing group
"Sync in":
Set value as next member in the current sharing group
Note: If no sync, INTERLEAVE shall be un-set.
FREQUENCY_SWITCH (0x33)
Same frequency must be set for all phases.
VIN_ON(0x35) and VIN_OFF(0x36)
Same thresholds must be set for all phases

3. Make additional manual settings (if needed)

SYNC is allocated to pin 9 (SA1_Sync) by default. If pin 12 (PG_Sync) shall be used for SYNC, then bit 3 in MFR_MULTI_PIN_CONFIG (0xF9). shall be set to 0.
If linear droop is requested, then set bit 5 in MFR_SPECIAL_OPTIONS (0xE0) to 0.
Other manual settings shall be performed in the Basic view in the Flex Power Designer for a quick and safe configuration.

4. Check settings
Ensure that the values are the same across all phases using the Register view in the Flex Power Designer.



Picture A1: PMBus Registers configured and/or locked in BMR458 in parallel operation using DLS.

5. Check that your hardware connections and component selections are consistent with your PMBus configurations.

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