TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

OPERATING INFORMATION

Input Voltage

The input voltage range 38 to 60 V (dc) meets the requirements for normal input voltage range in 48 V systems, 40.5 to 57.0 V.

Short duration transient disturbances can occur on the DC distribution and input of the product when a short circuit fault occurs on the equipment side of a protective device (fuse or circuit breaker). The voltage level, duration and energy of the disturbance are dependent on the particular DC distribution network characteristics and can be sufficient to damage the product unless measures are taken to suppress or absorb this energy. The transient voltage can be limited by capacitors and other energy absorbing devices like zener diodes connected across the positive and negative input conductors at strategic points in the distribution network. The end-user must secure that the transient voltage will not exceed the value stated in the Absolute maximum ratings. ETSI TR 100 283 examines the parameters of DC distribution networks and provides guidelines for controlling the transient and reduce its harmful effect.

Turn on and off input voltage

The product monitors the input voltage and will turn on and turn off at configured thresholds (see Electrical Specification). The turn-on input voltage voltage threshold, defined by command VIN_ON (0x35), is set higher than the corresponding turn-off threshold, defined by command VIN_UV_FAULT_LIMIT (0x59). Hence, there is a hysteresis between turn-on and turn-off input voltage levels.

Input voltage transient

The end-user must secure that the transient voltage will not exceed the value stated in the *Datasheet under Absolute maximum ratings* of each product. ETSI TR 100 283 examines the parameters of DC distribution networks and provides guidelines for controlling the transient and reduce its harmful effect.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. Minimum recommended external input capacitance is 100 µF. The electrolytic capacitors will be degraded in low temperature. The needed input capacitance in low temperature should be equivalent to 100 µF at 20 °C.

External decoupling capacitors

When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load.

The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several parallel capacitors to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. It is equally important to use low resistance and low inductance PCB layouts and cabling.

Enabling Output Voltage

The output voltage is controlled by the EN pin and/or the PMBus command OPERATION, depending on the settings of the standard PMBus command ON_OFF_CONFIG. Both active high and active low logic of the EN pin is supported.

By default the output voltage is enabled by the EN pin only (OPERATION is ignored), using active high logic.

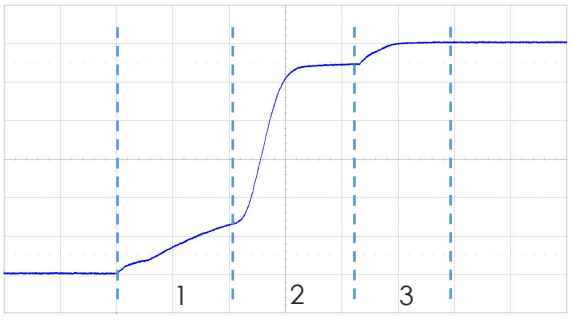
The EN pin has an internal 56 kΩ pull-up resistor to 5 V. The external device must have a sufficient sink current ability to be able pull EN pin voltage down below logic low threshold level (see Electrical Characteristics).

Care must be taken not to toggle EN pin when Vin < VIN_ON (PMBus register) and the unit is not operating. If this is done, the PG logic will be locked to low and will not be asserted when Vout is good.

Soft-start

Once enabled, the output voltage will ramp up to a 4:1 ratio of the input voltage. The ramp up is controlled monotonic and performed in three steps:

1. A small constant phase shift with low energy transfer. The linear ramp is monitored to detect a short circuit on the output. If the output voltage is not rising as expected, switching will stop.
2. Primary side FETs ramp-up. A slow soft increase of duty cycle until the phase shift reaches 50%.
3. Approaching the end of the soft start, the secondary FETs are enabled, slowly increasing the on duration of the FETs.



Ramp up waveform

Pre-bias start-up

The product has a pre-bias start up functionality and will not sink current during start up if a pre-bias source is present at the output terminals. If the pre-bias voltage is lower than the target value, the product will ramp up to the target value. If the pre-bias voltage is higher than the target value, the product will ramp down to the target value and in this case sink current.

Over temperature protection (OTP)

The product is protected from thermal overload by an internal over temperature shutdown function. The temperature sensor is located to provide a temperature representative of the module hot spot P1, see section Thermal Considerations in the datasheet.

The temperature is continuously monitored and when the temperature rises above the configured fault threshold level the product will respond as configured. The product can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.
3. Automatic restart (hiccup).

Default response is option 1. The default OTP limit is specified in section Electrical Characteristics in the datasheet.

The OTP fault and warning limits and response are configured using the PMBus commands OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE.

Input Voltage Protections (IUVP, IOVP)

The product monitors the input voltage continuously. If the output voltage is enabled, and the input voltage falls below or rises above the configured threshold levels (see Electrical Specification) the product will respond as configured. The response can be configured in different ways:

1. Immediate and definite shutdown of output voltage until the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.
3. Automatic restart (hiccup).

The default response is option 1.

The protections are configured using the PMBus commands: VIN_UV_FAULT_LIMIT, VIN_UV_FAULT_RESPONSE, VIN_OV_FAULT_LIMIT and VIN_OV_FAULT_RESPONSE.

Output Voltage Protection (UVP, OVP)

The product includes functionality for under and over voltage warnings and protection of the output voltage. The product can be configured to respond in different ways when the UVP/OVP fault limit is passed:

1. Immediate and definite shutdown of output voltage until the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.
3. Automatic restart (hiccup).

The default response is option 1.

The limits and fault responses are configured using the PMBus commands VOUT_UV_FAULT_LIMIT, VOUT_OV_FAULT_LIMIT, VOUT_UV_WARN_LIMIT, VOUT_OV_WARN_LIMIT, VOUT_UV_FAULT_RESPONSE and VOUT_OV_FAULT_RESPONSE.

Over current protection (OCP)

The product includes robust current limiting functionality for protection at overload transients during peak power operation. The OCP function has three parts:

A. Comparator OCP. Fast detection by an analog comparator that reacts on pulses down to a microsecond.

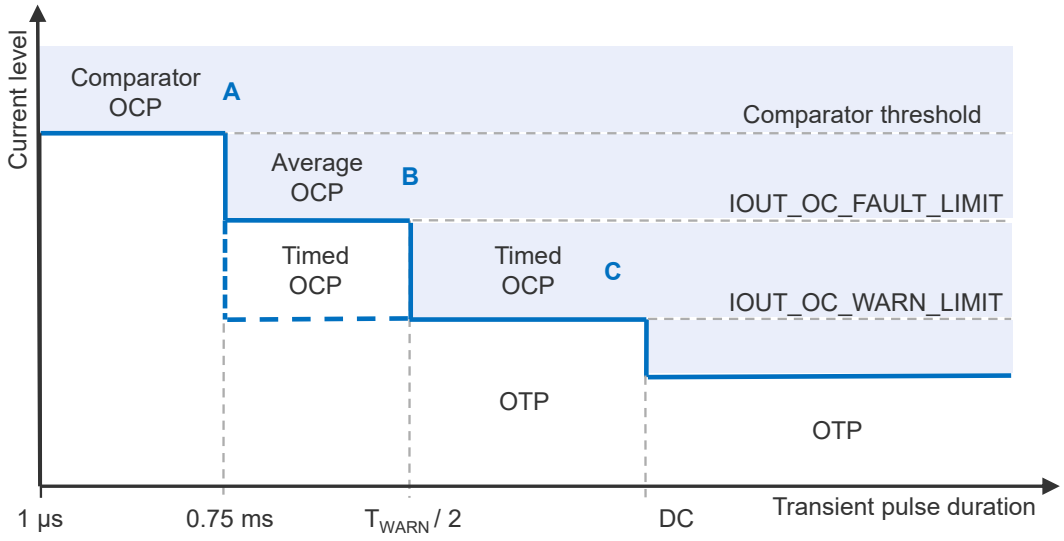
B. Average OCP. The threshold, set by PMBus command IOUT_OC_FAULT_LIMIT, is compared against the average value of the four last samples of the output current, with 250 µs sampling interval.

C. Timed OCP. A timed protection that ensures that component hotspot never exceeds the maximum rated temperature, for transients where the OTP protection is not fast enough. During any time interval T_{WARN} the output current is allowed to be over the threshold Io_{WARN} for a maximum accumulated period of half the time of T_{WARN}, or an OCP fault will be triggered.

Io_{WARN} is configured by PMBus command IOUT_OC_WARN_LIMIT, and the time T_{WARN} is configured by PMBus command MFR_IOUT_WARN_TIME.

Below figure summarizes the impact of the OCP functions:

- Transients with a duration up to 0.75 ms must be below the comparator threshold level.
- Transients with a duration in the range 0.75 ms to $T_{WARN}/2$ must be below the average OCP threshold. If the transients are too frequent, they must also be below the timed OCP threshold.
- Transients with a duration above $T_{WARN}/2$ must be below the timed OCP threshold.
- OTP will protect the unit at longer pulses and DC operation.



Max current level vs transient pulse duration and areas where OCP and OTP protections affect operation.

The pulse durations specified below are theoretical values at constant temperature. In practise, a current transient will cause a temperature rise of the current sensing element. The consequence of this is that a longer transient duration than the specified response time (1 µs, 0.75 ms or $T_{WARN}/2$) may be required before the corresponding OCP is triggered.

The default values of the OCP protection thresholds and T_{WARN} time are listed in section Electrical Specification – Control and Monitoring.

The comparator OCP is always enabled with a latched response, while for the average OCP and timed OCP different response options are available:

1. Immediate and definite shutdown of output voltage until the output voltage is re-enabled (latch).

2. Ignore fault and continue operation.

3. Automatic restart (hiccup).

The default response is option 1. The response options are configured using the PMBus command IOUT_OC_FAULT_RESPONSE.

Short circuit protection

During soft start the output voltage ramp is continuously monitored to detect a short circuit on the output. If the output voltage is not rising as expected, switching will stop.

Power good

The power good pin (PG) indicates when the product is ready to provide output voltage to the load. After initialization, the PG pin is asserted low (open drain) until the output voltage is enabled and the soft-start procedure has finalized. The product also provides a power good flag in the STATUS_WORD command.

Note on PG pin:
Care must be taken not to toggle EN pin when Vin < VIN_ON (PMBus register) and the unit is not operating. If this is done, the PG logic will be locked to low and will not be asserted when Vout is good.

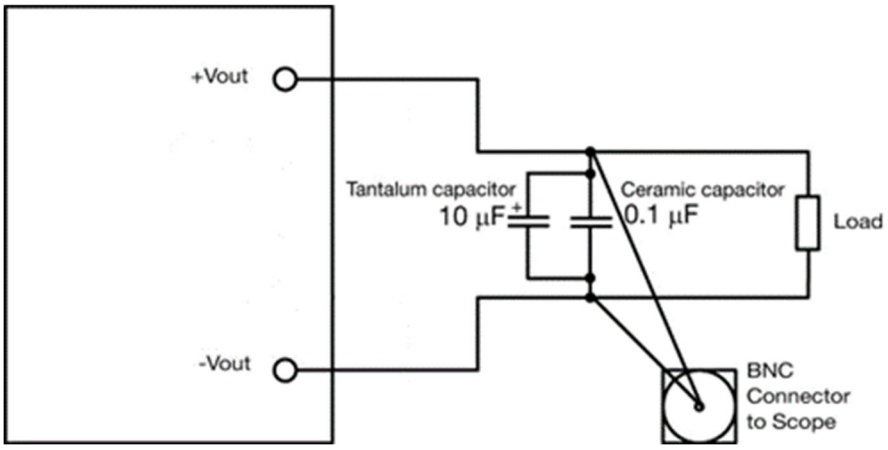
Temperature and current alert

The ALERT pin will be asserted low (open drain) when an over temperature warning condition or an over current warning condition occurs. The ALERT pin will be de-asserted automatically after the timer duration specified by the PMBus command MFR_IOUT_WARN_TIME. If the warning condition remains when the timer has expired, the timer restarts, and the ALERT pin will remain asserted. The over temperature warning and over current warning thresholds are defined by the PMBus commands OT_WARN_LIMIT and IOUT_OC_WARN_LIMIT.

Note that the MFR_IOUT_WARN_TIME setting also affects the timed OCP, see section Over Current Protection in this document.

Output ripple and noise

Output ripple and noise measured according to figure below using *evaluation board ROA 170256*.
See Design Note 022 for detailed information



Output ripple and noise test setup

Non-Volatile Memory (NVM)

The product incorporates a Non-Volatile Memory implemented with OTP (One-Time Programmable) technology. However, the memory structure imitates a multi-time programmable memory and can hold 32 updates.

The NVM is pre-loaded with Flex factory default values. The values in NVM are loaded to RAM during initialization after application of input voltage, whereafter commands can be changed through the PMBus Interface. Changes can be stored to NVM using the command OTP_UPLOAD (0xD6) which writes configuration changes in RAM to the OTP memory.

The user can read the command OTP_WRITE (0xCF) to find out the remaning number of possible store cycles, before OTP_UPLOAD (0xD6) is used.

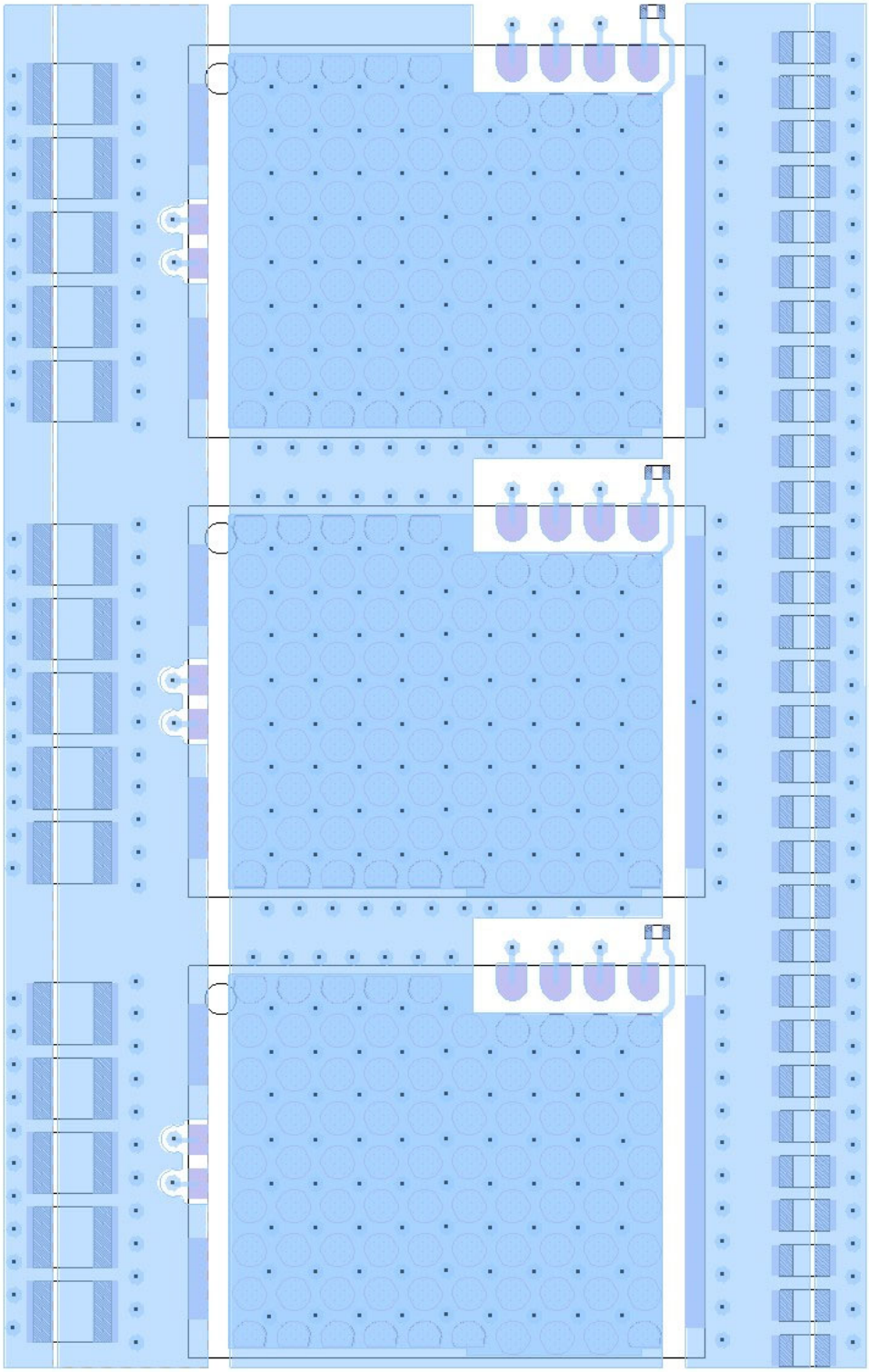
Parallel operation

Two or more products may be paralleled for redundancy. The products provide output voltage droop resistance in secondary transformer winding, which enables direct paralleling. To achieve optimum operation when paralleling modules, it is important to ensure the same PCB routing path resistances between the input terminals and merged output terminals. The output voltage will decrease with increased load current. This feature allows the product to be connected in parallel and share current within 10% accuracy at max output power. This means that up to 90% of max rated current from each module can be utilized.

In applications with several modules in parallel, the PG signal of all modules should be connected together. Further, load shall not be applied unless PG signal is high (= all modules have successfully ramped up).

For further information please contact your local Flex Power Modules' representative or email us at pm.info@flex.com.

Layout recommendation for parallelling



Layout for paralleling

POWER MANAGEMENT

PMBUS overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin. The following product parameters can continuously be monitored by a host: Input voltage, output voltage/ current and internal temperature.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface.

Throughout this document, different PMBus commands are referenced. The Flex Power Designer software suite can be used to configure and monitor this product via the PMBus interface. More information is found on our website.

SMBus interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I²C (master must allow for clock stretching) or SMBus host device. In addition, the product is compatible with SMBus version 3.0 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports 100 kHz and 400 kHz bus clock frequency only. The SMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\tau = R_p C_p \leq 1\ \mu s$$

where R_p is the pull-up resistor value and C_p is the bus load. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply between 2.7 to 3.8 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

PEC (Packet Error Check) is not supported.

PMBus addressing

The PMBus address is configured with a resistor, RADDR, connected between the ADDR pin and GND. The value of the resistor decides an index according to the table below. The tolerance of the resistor must be 1% or better.

Index	R_{ADDR} [kΩ]	Suggested 1% RADDR [kΩ]
0	0 – 0.143	0
1	0.418 – 0.658	0.47
2	0.959 – 1.165	1
3	1.494 – 1.753	1.6
4	2.114 – 2.497	2.2
5	2.899 – 3.448	3.3
6	3.903 – 4.701	4.3
7	5.228 – 6.373	5.6

Index	R_{ADDR} [kΩ]	Suggested 1% RADDR [kΩ]
8	7.000 – 8.645	8.2
9	9.413 – 11.819	10
10	12.796 – 16.328	15
11	17.626 – 22.982	22
12	24.802 – 34.857	33
13	37.761 – 59.808	47
14	65.637 – 119.177	100
15	135.731 - open	open

The PMBus address is calculated as:

PMBus Address = Base Address + Index

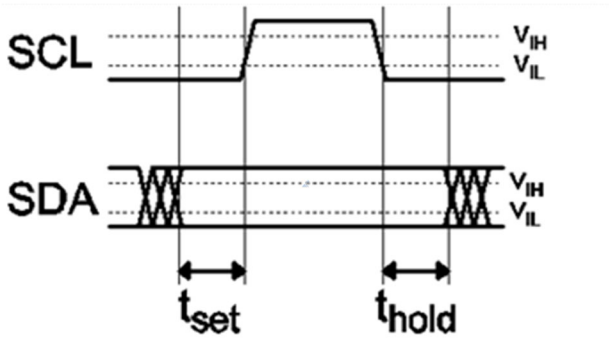
where the base address is defined by bits [7:5] in the PMBus command PMBUS_ADDRESS (0xE0). The standard default value for the base address is 0x20, giving an address range from 0x20 to 0x2F. Specific product variants may have a different default value.

If changing the base address, the change will take effect after the input voltage is cycled.

I2C/SMBus timing

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the rising edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching.

This product supports the BUSY flag in the status commands to indicate product being too busy for SMBus response. A bus-free time delay between every SMBus transmission (between every stop & start condition) must occur. Refer to the SMBus specification, for SMBus electrical and timing requirements.



Set-up and hold timing diagram

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Output current	READ_IOUT
Output power	READ_POUT
Temperature	READ_TEMPERATURE_1

These PMBus commands are updated every 0.25 ms.

The temperature sensor is located to provide a temperature reading representative of the module hot spot P1, see section Thermal Considerations in the datasheet.

Monitoring faults

The user may read PMBus status commands to find out what fault or warning condition occurred, see table below:

Fault and warning status	PMBus command
Overview, Power Good	STATUS_BYTE STATUS_WORD
Output voltage level	STATUS _VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

Status bits are asserted until faults and/or warnings are cleared by the CLEAR_FAULTS (0x03) command. A re-enable of the output voltage will not clear the status bits.

General PMBus comand summary

PMBus signal interfaces characteristics

Characteristic	conditions	minimum	typical	maximum	unit
PMBus signal interface characteristics					
External sync pulse width		150			ns
Input clock frequency drift tolerance	External sync.	-4		4	%
Initialization time	From V_{in} > 27 V to ready to be enabled		30		ms
Output voltage total on delay time	Enable by input voltage		T_{INIT} + T_{ONdel}		
	Enable by RC or CTRL pin		T_{ONdel}		
Logic output low signal level	SCL, DA, SYNC, GCB, SALERT, PG, sink/source current = 4 mA			0.25	V
Logic output high signal level		2.7			V
Logic output low sink current				4	mA
Logic output high source current				4	mA
Logic input low threshold	SCL, SDA, CTRL, SYNC			1.1	V
Logic input high threshold		2.1			V
Logic pin input capacitance	SCL, SDA, CTRL, SYNC		10		pF
Supported SMBus operating frequency		100		400	kHz
SMBus bus free time	STOP bit to START bit		1.3		µs
SMBus SDA setup time from SCL			100		µs
SMDBus SDA hold time from SCL			0		ns
SMBus START/STOP condition setup/hold time from SCL			600		ns
SCL low period		1.3			µs
SCL high period			0.6	50	µs