TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

OPERATING INFORMATION: COMMON FEATURES

The features listed in the following pages are common to DC/DC converters.

VCC

A separate 5V Vcc voltage needs to be applied to the module in order to power the controller and driver circuits.

Turn on and off input voltage

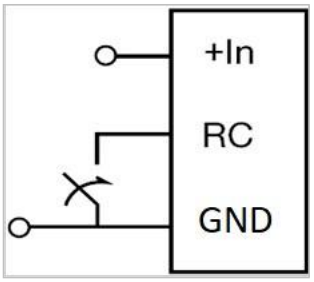
The product monitors the input voltage and will turn on and turn off at configured thresholds (see Technical *Specification: part 1 - Electrical Specification*). The turn-on input voltage threshold is set higher than the corresponding turn-off threshold. Hence, there is a hysteresis between turn-on and turn-off input voltage levels.

Input voltage transient

The end-user must secure that the transient voltage will not exceed the value stated in the Technical Specification under Absolute maximum ratings of each product. ETSI TR 100 283 examines the parameters of DC distribution networks and provides guidelines for controlling the transient and reduce its harmful effect.

Remote control (RC)

The products are fitted with a remote control function referenced to the ground (GND), with negative and positive logic options available. The RC function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. The RC pin has an internal pull up resistor.
The 5V Vcc auxiliary power, and Vin should be ready before the remote control pin is set enable.
The minimum allowed time from where Vcc is applied to when RC is activated is 50ms.



Remote control

The external device must provide a minimum required sink current >0.5 mA to guarantee a voltage not higher than maximum voltage on the RC pin. Please refer to the Technical Specification/Electrical specifications of the product. When the RC pin is left open, the voltage on the RC pin is max 5 V. The standard product is provided with "positive logic" RC and will be off as long as the RC pin is connected to GND. To turn on the product the RC pin should be open.

Input and output impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. Minimum recommended external input capacitance is given in the *Technical Specification*. Electrolytic capacitors will be degraded in low temperature. The needed input capacitance in low temperature should be equivalent to the value stated in the Technical Specification at 25°C. The performance in some applications can be enhanced by addition of external capacitance as described under External decoupling capacitors (next paragraph). If the input voltage source contains significant inductance, the addition of a low ESR ceramic capacitor of 22 – 100 µF capacitor across the input of the product will ensure stable operation. Input Voltage and output power changes the need of input capacitance whereas higher power requires increased input capacitance.

External decoupling capacitors

Add low ESR ceramic and electrolytic capacitors as close to the load as possible, using several parallel capacitors is a good way to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. It is equally important to use low resistance and low inductance PWB layouts and cabling.

For further information please contact your local Flex Power Modules' representative or email us at pm.info@flex.com.

Output voltage adjust and Margin using PMBus

As this device is unregulated no Output voltage adjust or Margin capabilities exists.

Startup sequencing

This module can be started in two defined sequences.

1. Vcc is applied before Vin and finally the RC is activated.
2. Second sequency is to allow Vin applied before Vcc and finally activate the RC.

In both cases it is absolutely vital that the time from where Vcc is applied to when RC is activated is minimum 50ms.

This timing is very important in order to allow the controller to start the module in correct way.

Violating this requirement will result in catastrophic module failure.

Soft start power up

The module has a built in soft start with a rise time of typically 10 ms. This is used to control inrush current.

The rise time is the time taken for the output to ramp to its target voltage. The soft start is not configurable.

Pre-bias start-up

The product has a pre-bias start up functionality and will not sink current during start up if a pre-bias source is present at the output terminals. If the pre-bias voltage is lower than the output voltage, the product will ramp up to the target value.

Over temperature protection (OTP)

The product is protected from thermal overload by an internal over temperature sensor.
If the temperature exceeds the over-temperature threshold the module will shut down and enter latch mode.
The OTP warning, fault limit and fault response can be configured via the PMBus.
Note: using the fault response "ignore fault event" may cause permanent damage to the product.

Input over/under voltage protection

The product can be protected from high input voltage and low input voltage by pre-configured values.
The over/under-voltage fault level and fault response is easily configured via the PMBus.
For more information, see *Technical Reference Document: PMBus*.

Output Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. If the output voltage exceeds the OVP limit, the product *can respond in different ways*.
The default response from an over voltage fault is to immediately shut down and enter latch mode.
OVP fault level and fault response can be configured via the PMBus.
For more information, see *Technical Reference Document: PMBus*.

Over current protection (OCP)

The product includes robust current limiting functionality for protection at overload transients during peak power operation. The OCP function has three parts:

A. Comparator OCP. Fast detection by an analog comparator that reacts on pulses down to a microsecond.

B. Average OCP. The threshold, set by PMBus command IOUT_OC_FAULT_LIMIT, is compared against the average value of the four last samples of the output current, with 250 µs sampling interval.

C. Timed OCP. A timed protection that ensures that component hotspot never exceeds the maximum rated temperature, for transients where the OTP protection is not fast enough. During any time interval T_{WARN} the output current is allowed to be over the threshold I_{OWARN} for a maximum accumulated period of half the time of T_{WARN}, or an OCP fault will be triggered.

Below figure summarizes the impact of the OCP functions:

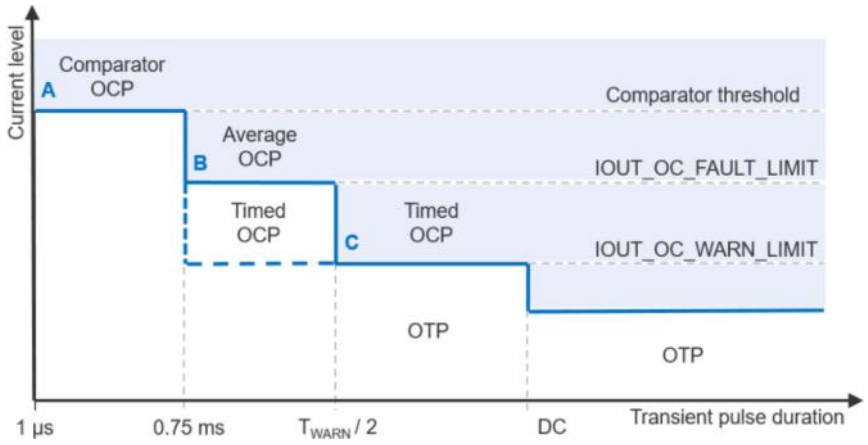
- Transients with a duration up to 0.75 ms must be below the comparator threshold level.

- Transients with a duration in the range 0.75 ms to $T_{WARN}/2$ must be below the average OCP threshold. If the transients are too frequent, they must also be below the timed OCP threshold.

- Transients with a duration above $T_{WARN}/2$ must be below the timed OCP threshold.

- OTP will protect the unit at longer pulses and DC operation.

Max current level vs transient pulse duration and areas where



OCP and OTP protections affect operation.

The pulse durations specified below are theoretical values at constant temperature. In practice, a current transient will cause a temperature rise of the current sensing element. The consequence of this is that a longer transient duration than the specified response time (1 µs, 0.75 ms or $T_{WARN}/2$) may be required before the corresponding OCP is triggered.

The default values of the OCP protection thresholds and T_{WARN} time are listed in section Electrical Specification – Protection features.

The comparator OCP is always enabled with a latched response, while for the average OCP and timed OCP different response options are available:

1. Immediate and definite shutdown of output voltage until the output voltage is re-enabled (latch).

2. Ignore fault and continue operation.

3. Automatic restart (hiccup).

The default response is option 1. The response options are configured using the PMBus command

IOUT_OC_FAULT_RESPONSE.

Short Circuit Protection

During soft start the output voltage ramp is continuously monitored to detect a short circuit on the output. If the output voltage is not rising as expected, switching will stop.

Switching frequency

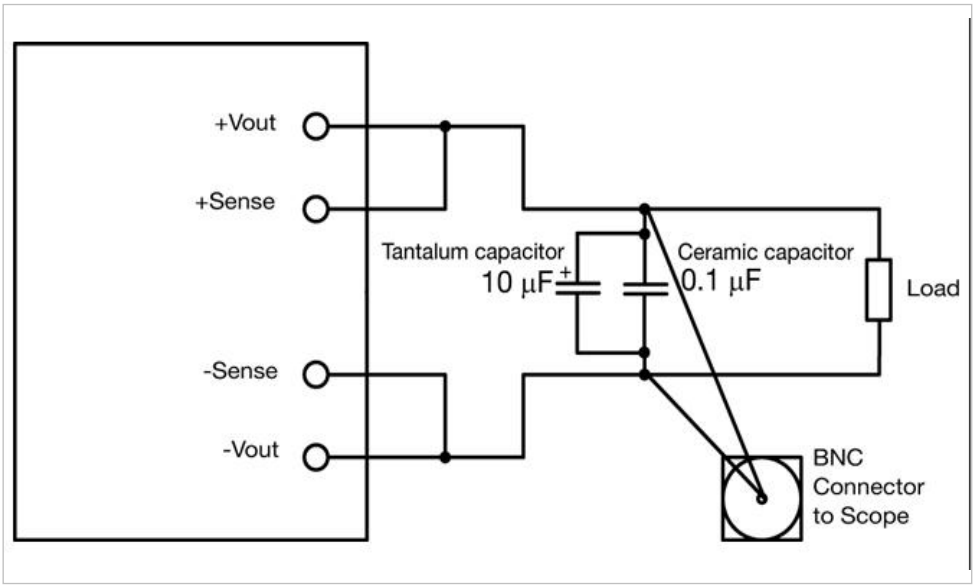
The product is optimized at the frequency given in the Technical Specification under part 1- Electrical Specification. The frequency can not be changed by the user. Please contact your local Flex Power Modules FAE for more details.

Address offset

It is possible to change the Address offset. Please contact your local Flex Power Modules FAE for more details.

Output ripple and noise

Output ripple and noise measured according to figure below.
See Design Note 022 for detailed information.



Output ripple and noise test set-up

OPERATING INFORMATION: PRODUCT SPECIFIC FEATURES

Parallel operation

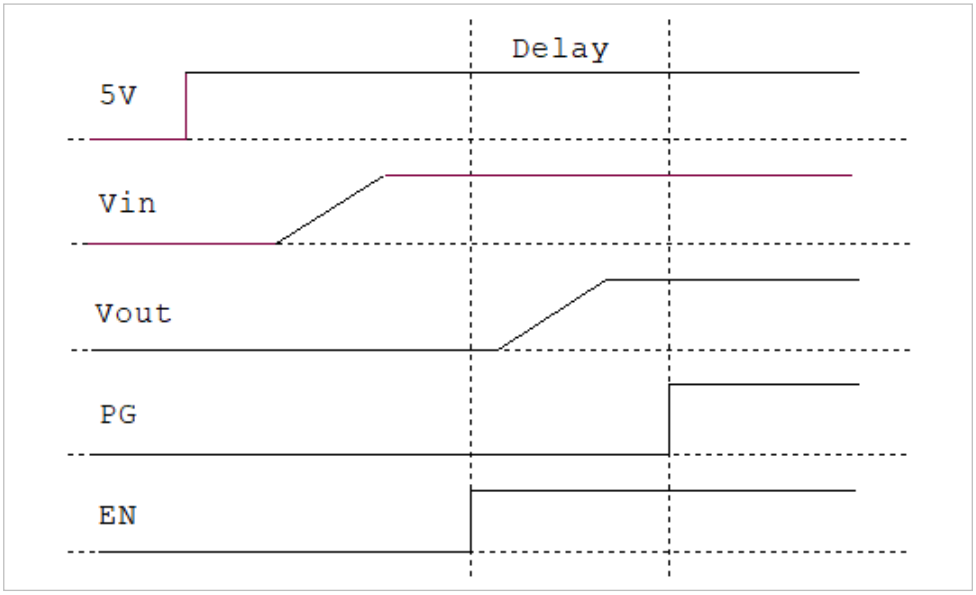
Two or more products may be paralleled for redundancy. The products provide output voltage droop resistance in secondary transformer winding, which enables direct paralleling. To achieve optimum operation when paralleling modules, it is important to ensure the same PCB routing path resistances between the input terminals and merged output terminals. The output voltage will decrease with increased load current. This feature allows the product to be connected in parallel and share current within 10% accuracy at max output power. This means that up to 90% of max rated current from each module can be utilized.

For further information please contact your local Flex Power Modules' representative or email us at pm.info@flex.com.

Power good

The power good pin (PG) indicates when the product is within the output voltage range. During ramp-up and any fault condition, PG is held low. By default PG is asserted high after the soft start is finished. The PG pin is configured as open drain and requires an external pull-up to Vcc.

The polarity is by default configured to active high.
When Vcc is first applied the module initialize the MCU and PG will be held low.
After input voltage is applied, the EN pin is set and the soft start sequence is initiated.
When the module completes its output ramp up and the output voltage is correct and stable, the PG signal will be set high.
Please refer to below sequence waveform.



Power Good implementation

The product provides a Power Good flag in the Status Word register that indicates the output voltage is in correct level and no-fault condition.

For more information, see *Technical Reference Document: PMBus*.

Non-Volatile Memory (NVM)

The product incorporates a Non-Volatile Memory implemented as with one-time programmable technology (OTP) for storage of the PMBus command values. Control registers are pre-loaded with Flex factory default values. The User may reprogram the user control registers through the PMBus Interface a limited amount of times.

For further information please contact your local Flex Power Modules' representative or email us at pm.info@flex.com.

POWER MANAGEMENT

PMBUS overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. The following product parameters can continuously be monitored by a host: Input voltage, output voltage/current and internal temperature.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). Power management functions can be reconfigured using PMBus.

Throughout this document, different PMBus commands are referenced. The Flex Power Designer software suite can be used to configure and monitor this product via PMBus.

More information is found on our website.

SMBus interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I²C (master must allow for clock stretching) or SMBus host device. In addition, the product is compatible with PMBus version 1.3.
The product supports 100 kHz and 400 kHz bus clock frequency only. The PMBus signals, SCL and SDA require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\tau = R_p C_p \leq 1us$$

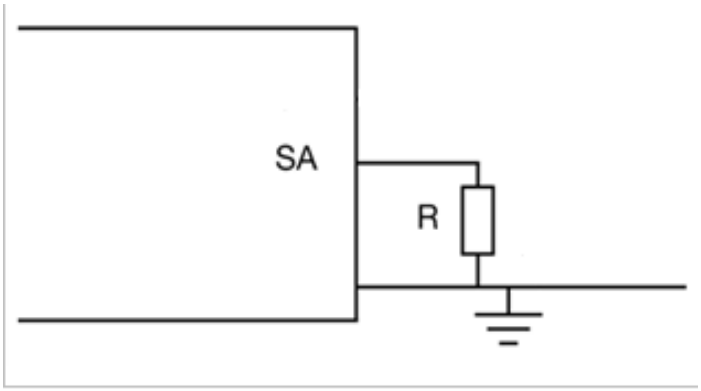
R_p is the pull-up resistor value and C_p is the bus load. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply between 2.7 to 3.8 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied.

This module requires communication disabling PEC (Packet Error Check) when communicating via PMBus.

PMBus addressing

The following figure and table show recommended resistor values with min and max range for hard-wiring PMBus addresses (series E96, 1% tolerance resistor suggested).

The SA pin can be configured with a resistor to GND according to the following table.



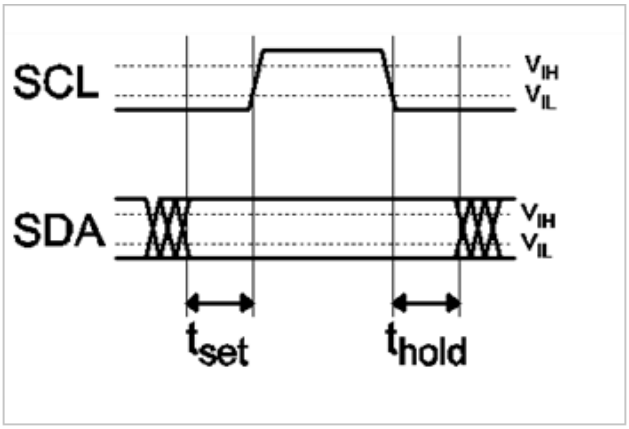
Schematic of connection address resistor

	Range of Rext [kOhm]		
Adress	Min	Typ	Max
20h	0	0	0,147
21h	0,415	0,576	0,661
22h	0,956	1,05	1,168
23h	1,490	1,62	1,756
24h	2,110	2,26	2,500
25h	2,896	3,16	3,451
26h	3,900	4,22	4,704
27h	5,225	5,76	6,375
28h	6,996	7,68	8,647
29h	9,410	10,5	11,820
2Ah	12,793	14,3	16,328
2Bh	17,623	20	22,978
2Ch	24,800	28,4	34,840
2Dh	37,756	46,4	59,753
2Eh	65,633	86,6	118,984
2Fh	135,766	205	Open

I2C/SMBus timing

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the rising edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. This product supports the BUSY flag in the status commands to indicate product being too busy for SMBus response. A bus-free time delay between every SMBus transmission (between every stop & start condition) must occur. Refer to the SMBus specification, for SMBus electrical and timing requirements.

Note that an additional delay of 300 ms has to be inserted in case of storing the RAM content into the internal non-volatile memory.



Set-up and hold timing diagramm

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Output current	READ_IOUT
Temperature*	READ_TEMPERATURE_1

* reports the temperture from temperature sensor.

Monitoring faults

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Fault and warning	PMBus command
Overview, Power Good	STATUS_BYTE STATUS_WORD
Output voltage level	STATUS _VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

General PMBus comand summary

PMBus signal interfaces characteristics

Characteristic	conditions	minimum	typical	maximum	unit
PMBus signal interface characteristics					
External sync pulse width		150			ns
Input clock frequency drift	External sync.	-4		4	%
Initialization time	From VI > 27 V to ready to		30		ms
Output voltage total on delay time	Enable by input voltage		T_{INIT} + T_{ONdel}		
	Enable by RC or CTRL pin		T_{ONdel}		
Logic output low signal	SCL, DA, SYNC, GCB, SALERT, PG, sink/source current = 4 mA			0.25	V
Logic output high signal		2.7			V
Logic output low sink				4	mA
Logic output high source				4	mA
Logic input low threshold	SCL, SDA, CTRL, SYNC			1.1	V
Logic input high threshold		2.1			V
Logic pin input	SCL, SDA, CTRL, SYNC		10		pF
Supported SMBus		100		400	kHz
SMBus bus free time	STOP bit to START bit		1.3		µs
SMBus SDA setup time from SCL			100		µs
SMDBus SDA hold time			0		ns
SMBus START/STOP condition setup/hold time			600		ns
SCL low period		1.3			µs
SCL high period			0.6	50	µs