TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

OPERATING INFORMATION

Input Voltage

The input voltage range 40 to 60 V (DC) meets the requirements for normal input voltage range in 48 V systems, 40.5V to 57.0 V.

Short duration transient disturbances can occur on the DC distribution and input of the product when a short circuit fault occurs on the equipment side of a protective device (fuse or circuit breaker). The voltage level, duration and energy of the disturbance are dependent on the particular DC distribution network characteristics and can be sufficient to damage the product unless measures are taken to suppress or absorb this energy. The transient voltage can be limited by capacitors and other energy absorbing devices like zener diodes connected across the positive and negative input conductors at strategic points in the distribution network. The end-user must secure that the transient voltage will not exceed the value stated in the Absolute maximum ratings. ETSI TR 100 283 examines the parameters of DC distribution networks and provides guidelines for controlling the transient and reduce its harmful effect.

Turn on and off input voltage

The product monitors the input voltage and will turn on and turn off at configured thresholds (see Electrical Specification). The turn-on input voltage threshold, defined by command VIN_ON (0x35), is set higher than the corresponding turn-off threshold, defined by command VIN_OFF (0x36). Hence, there is a hysteresis between turn-on and turn-off input voltage levels.

Input voltage transient

The end-user must secure that the transient voltage will not exceed the value stated in the *Datasheet under Absolute maximum ratings* of each product. ETSI TR 100 283 examines the parameters of DC distribution networks and provides guidelines for controlling the transient and reduce its harmful effect.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. The electrolytic capacitors will be degraded in low temperature. The needed input capacitance in low temperature should be equivalent to minimum recommended input and output capacitance at 20 °C. The performance in some applications can be enhanced by addition of external capacitance as described under External decoupling capacitors. If the input voltage source contains significant inductance, the addition of a low ESR ceramic capacitor of 22 – 100 µF capacitor across the input of the product will ensure stable operation. The minimum required capacitance value depends on the output power and the input voltage. The higher output power the higher input capacitance is needed.

External decoupling capacitors

The voltage at the load can be improved by adding decoupling capacitors at the load if loads with significant dynamic currents are required. The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several parallel capacitors to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. It is equally important to use low resistance and low inductance PCB layouts and cabling.

Enabling Output Voltage

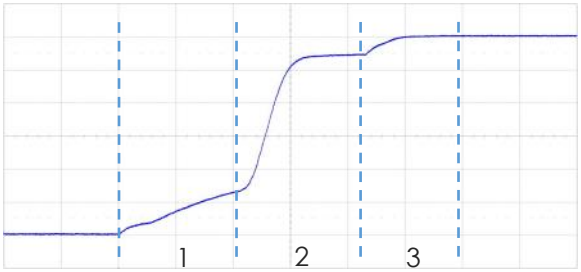
The output voltage is controlled by the EN pin and/or the PMBus command OPERATION, depending on the settings of the standard PMBus command ON_OFF_CONFIG. Both active high and active low logic of the EN pin is supported. By default the output voltage is enabled by the EN pin using active low logic (OPERATION is ignored).

The EN pin has open collector circuit. The external pull-up resistor and device must have a sufficient sink current ability to be able pull EN pin voltage down below logic low threshold level (see Electrical Characteristics).

Soft-start and soft stop

Once enabled, the output voltage will ramp up to a 8:1 ratio of the input voltage. The ramp up is controlled monotonic and performed in three steps:

1. FETs start switching at minimum Duty cycle and switching frequency and updated based on Vout/ Vin ratio with low energy transfer. The ramp is monitored to detect short circuits on the output.
2. The output voltage starts ramping up slowly by increasing the switching frequency to nom.
3. Approaching the end of the soft start, the duty cycle is slowly increasing the duty cycle to nom.



Ramp up waveform

Soft-stop can be disabled through the PMBus command ON_OFF_CONFIG (0x02). The BMR 321 start-up sequence does not allow to load the module more than 2A at startup. To fully load the BMR321 (750W) it needs to have ended the startup sequence and be in continuous operation mode and have initiated a Power Good signal. The load during startup is output capacitor dependent and a max allowed output capacitor is 6mF.

Note: The soft-start sequence can not be changed by the user.

Over temperature protection (OTP)

The product is protected from thermal overload by an internal over temperature shutdown function. The temperature sensor is located to provide a temperature representative of the module hot spot, see section Thermal Considerations in the datasheet.

The temperature is continuously monitored and when the temperature rises above the configured fault threshold level the product will respond as configured. The product can respond in several ways as follows:

1. Immediate shutdown of output voltage until the output voltage is re-enabled (latch). Default setting.
2. Ignore fault and continue operation. Not recommended.

The default OTP limit is specified in section Electrical Characteristics in the datasheet. The OTP fault and warning limits and response are configured using the PMBus commands OT_FAULT_LIMIT(0x4F), OT_WARN_LIMIT(0x51) and OT_FAULT_RESPONSE(0x50).

Input Voltage Protections (IUVP, IOVP)

The product monitors the input voltage continuously. If the output voltage is enabled, and the input voltage falls below or rises above the configured threshold levels (see Electrical Specification) the product will respond as configured. The response can be configured in different ways:

1. Immediate shutdown of output voltage until the output voltage is re-enabled (latch). Default setting.
2. Ignore fault and continue operation. Not recommended.

The protections are configured using the PMBus commands: VIN_UV_FAULT_LIMIT(0x59), VIN_UV_FAULT_RESPONSE(0x5A), VIN_OV_FAULT_LIMIT(0x55) and VIN_OV_FAULT_RESPONSE(0x56).

Output Voltage Protection (UVP, OVP)

The product includes functionality for under and over voltage warnings and protection of the output voltage. The product can be configured to respond in different ways when the UVP/OVP fault limit is passed:

1. Immediate shutdown of output voltage until the output voltage is re-enabled (latch). Default setting.
2. Ignore fault and continue operation. Not recommended.

The limits and fault responses are configured using the PMBus commands VOUT_UV_FAULT_LIMIT(0x44), VOUT_OV_FAULT_LIMIT(0x40), VOUT_UV_WARN_LIMIT(0x43), VOUT_OV_WARN_LIMIT(0x42), VOUT_UV_FAULT_RESPONSE(0x45) and VOUT_OV_FAULT_RESPONSE(0x41).

For more information, see *Technical Reference Document: PMBus*.

Pre-bias start-up

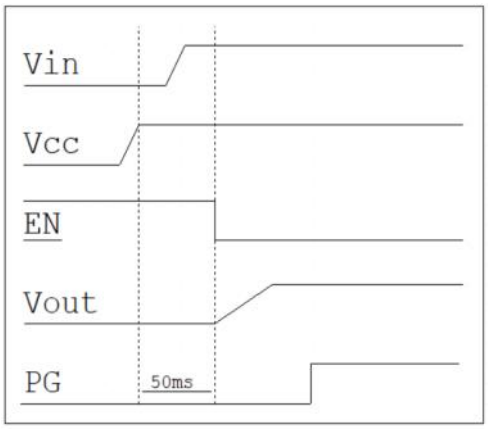
The product has a pre-bias start up functionality and will not sink current during start up if a pre-bias source is present at the output terminals. If the pre-bias voltage is lower than the target value, the product will ramp up to the target value.

Startup sequencing

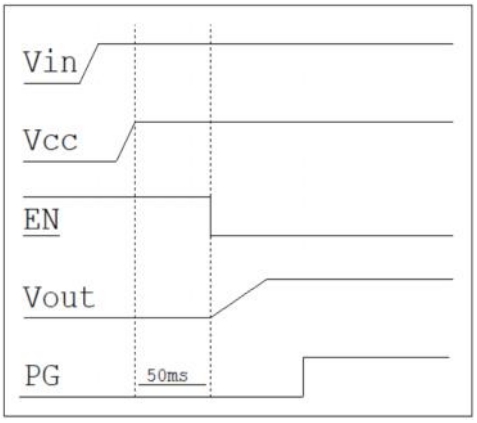
This module can be started in two defined sequences.

1. Vcc is applied before Vin and finally the EN is activated.
2. Second sequency is to allow Vin applied before Vcc and finally activate the EN.

In both cases it is absolutely vital that the time from where Vcc is applied to when EN is activated is minimum 50ms.



Case 1



Case 2

Power good

The power good pin (PG) indicates when the product is ready to provide output voltage to the load. After initialization, the PG pin is asserted low (open drain) until the output voltage is enabled and the soft-start procedure has finalized. The product also provides a power good flag in the STATUS_WORD command that indicates the output voltage is within a specified tolerance of its target level and no-fault condition exists.

By default, the PG pin is configured as open drain output, but it is also possible to set the output in push/pull mode by the command MFR_MULTI_PIN_CONFIG (0xF9). The polarity is by default configured to active high, the polarity of PG can be set to active low using the command FW_CONFIG_PMBUS (0xC9).

Note on PG pin:
It is not recommended to use push-pull when paralleling PG-pins.

Short circuit protection

During soft start the output voltage ramp is continuously monitored to detect a short circuit on the output. If the output voltage is not rising as expected, switching will stop and raise Startup OC fault. When there is a short circuit during operation, the module is protected by Over Current Protection.

Over current protection (OCP)

The product includes robust current limiting functionality for protection at overload at continuous operation as well as transients during peak power operation. The OCP function has 4 parts:

1. Fast OCP that reacts on pulses from a few microseconds to approximately 100us, and used for protection at very fast peak power operation.
2. Normal standard PMBus OCP triggers from 100us up to approximately 20ms
3. From 20ms and to continous max TDP, a slow OCP protection is enabled based on averaging power over time. The function is configured to allow a load step from TDP to Peak Power level between 20ms and 200ms
4. After 200ms the protection level is configured for continuous operation.

Peak power considerations

The DC/DC converter has a peak power level set in the technical specification with a time limit. This in order to handle higher power than the thermal design power (TDP) for the converter. The Peak power level is also set in consideration of overshoot from a fast transient, tested from base to peak current with a specified di/dt. Thus a higher peak power can be achieved but for a shorter period of time. Faster di/dt and higher peak load than specified, might cause current overshoot resulting in OCP fault.

For further assistance, contact your local Flex Power Modules' representative or email us to pm.info@flex.com

Switching frequency

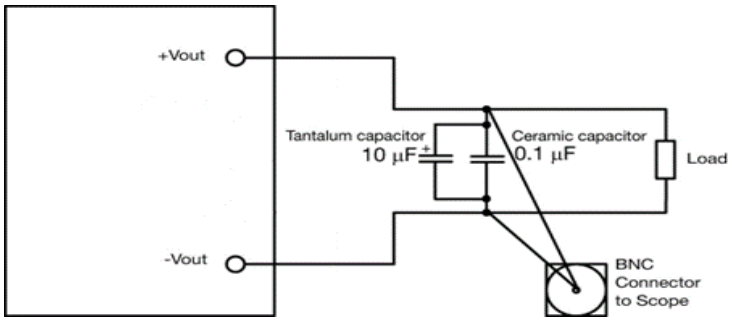
The product is optimized at the frequency given in the Technical Specification under part 1- Electrical Specification. The frequency can not be changed by the user. Please contact your local Flex Power Modules FAE for more details.

Multi pin configurations

The MFR_MULTI_PIN_CONFIG (0xF9) command can be re-configured using the PMBus interface to enable or disable different functions and set the pin configuration of the digital header.
The MULTI_PIN_CONFIG is easily configured using Flex Power Designer.
For more information, see *Technical Reference Document: PMBus*.

Output ripple and noise

Output ripple and noise measured according to figure below using *evaluation board ROA 170286*.
See Design Note 022 for detailed information



Output ripple and noise test setup

Non-Volatile Memory (NVM)

The product incorporates two Non-Volatile Memory areas for storage of the PMBus command values; the Default NVM and the User NVM. The Default NVM is pre-loaded with Flex factory default values. The Default NVM is write-protected and can be used to restore the Flex factory default values through the command RESTORE_DEFAULT_ALL (0x12).

The User NVM is pre-loaded with Flex factory default values. The User NVM is writable and open for customization. The values in NVM are loaded during initialization according to section Initialization Procedure, where after commands can be changed through the PMBus Interface.

The module contains a one-time programmable memory (OTP) used to store configuration settings, which will not be programmed into the device OTP automatically. The STORE_USER_ALL(0x15) commands must be used to commit the current settings are transferred from RAM to OTP as device defaults.

Note: The one-time programmable memory (OTP) has limited storing times, frequent use of STORE_USER_ALL command can lead to memory space exhaustion. Remaining available memory is displayed in Flex Power Designer.

Parallel operation Droop Load Share (DLS)

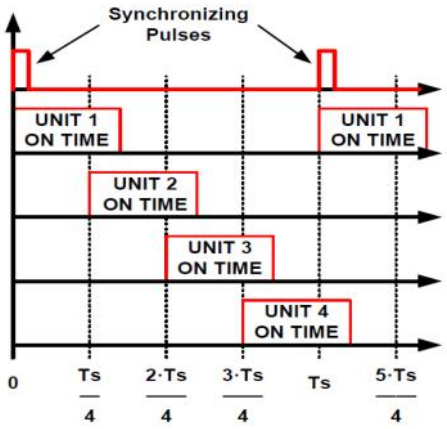
Two or more products may be paralleled for redundancy. The products provide output voltage droop resistance in secondary transformer winding, which enables direct paralleling. The output voltage will decrease with increased load current. This feature allows the product to be connected in parallel and share current within 10% accuracy at max output power. This means that up to 90% of max rated current from each module can be utilized.

In applications with several modules in parallel, the PG signal of all modules should be connected together. Further, load shall not be applied unless PG signal is high (all modules have successfully ramped up).

For further information please contact your local Flex Power Modules' representative or email us at pm.info@flex.com.

SYNC

Synchronizing multiple converters to the same frequency with proper phase shift is often used to reduce the filter cost, lower the EMI and reduce the voltage and current ripple. The SYNC allows to synchronize the PWM outputs to an external signal or provide a sync signal for other converters to act in synchronization. The INTERLEAVE command is used to configure the phase of interleaved topologies or the phase of multiple devices in parallel unit applications. SYNC is supported by BMR321 module. It is applied by connecting $n_{modules}$ SYNC pins together and programming interleave parallelable module. SYNC pin is open collector circuit.



Example SYNC function

Output Voltage leakage

BMR321 has an internal voltage leakage of approximately 2V on the Vout connector when the module is switched off with Vin present. The module is non-isolated and has some of internal circuit which create this leakage. Leakage current is small, a few mA. If customer would like to have 0V to output it is enough to have bleeder resistor 1kOm.

POWER MANAGEMENT

PMBus overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. The following product parameters can continuously be monitored by a host: Input voltage, output voltage/current and internal temperature.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface.

Throughout this document, different PMBus commands are referenced. The Flex Power Designer software suite can be used to configure and monitor this product via the PMBus interface. More information is found on our website.

SMBus interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I²C (master must allow for clock stretching) or SMBus host device. The product supports 100 kHz and 400 kHz bus clock frequency only. The SMBus signals, SCL, SDA require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\tau = R_p C_p \leq 1\ \mu s$$

where R_p is the pull-up resistor value and C_p is the bus load. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply between 2.7V to 3.7V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

PMBus addressing

The PMBus address is configured with a resistor, RADDR, connected between the ADDR pin and GND. The value of the resistor decides an index according to the table below. The tolerance of the resistor must be 1% or better.

Index	R_{ADDR} [kΩ]	Suggested 1% RADDR [kΩ]
F	0.70-0.85	0.78
E	0.99-1.21	1.1
D	1.35-1.65	1.5
C	1.81-2.22	2.02
B	2.43-2.97	2.7
A	3.16-3.87	3.52
9	4.23-5.17	4.7
8	5.46-6.67	6.07

Index	R_{ADDR} [kΩ]	Suggested 1% RADDR [kΩ]
7	7.20-8.80	8.0
6	9.18-11.22	10.2
5	11.88-14.52	13.2
4	15.48-18.92	17.2
3	20.22-24.71	22.47
2	26.28-32.12	29.2
1	35.10-42.90	39.0
0	50.40-61.60	56k (or open)

The PMBus address is calculated as:

PMBus Address = Base Address + Index

where the base address is defined by bits [7:5] in the PMBus command PMBUS_ADDRESS (0xC9). Standard default value for the base address is (0x4n), (0x6n), giving an address range from (0xnF) to (0xn0). Specific product variants may have a different default value.

If changing the base address, the change will take effect after the input voltage is cycled.

I2C/SMBus timing

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the rising edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching.

This product supports the BUSY flag in the status commands to indicate product being too busy for SMBus response. A bus-free time delay between every SMBus transmission (between every stop & start condition) must occur. Refer to the SMBus specification, for SMBus electrical and timing requirements.

Set-up and hold timing diagram

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Output current	READ_IOUT
Temperature	READ_TEMPERATURE_1

These PMBus commands are updated every 0.25 ms.

The temperature sensor is located to provide a temperature reading representative of the module. See section Thermal Considerations in the datasheet.

Monitoring faults

The user may read PMBus status commands to find out what fault or warning condition occurred, see table below:

Fault and warning status	PMBus command
Overview, Power Good	STATUS_BYTE STATUS_WORD
Output voltage level	STATUS _VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

Status bits are asserted until faults and/or warnings are cleared by the CLEAR_FAULTS (0x03) command. A re-enable of the output voltage will not clear the status bits.

General PMBus comand summary

PMBus signal interfaces characteristics

Characteristic	conditions	minimum	typical	maximum	unit
PMBus signal interface characteristics					
External sync pulse width		150			ns
Input clock frequency drift tolerance	External sync.	-4		4	%
Initialization time	From V_{in} > 27 V to ready to be enabled		30		ms
Output voltage total on delay time	Enable by input voltage		T_{INIT} + T_{ONdel}		
	Enable by RC or CTRL pin		T_{ONdel}		
Logic output low signal level	SCL, DA, SYNC, GCB, SALERT, PG, sink/source current = 4 mA			0.25	V
Logic output high signal level		2.7			V
Logic output low sink current				4	mA
Logic output high source current				4	mA
Logic input low threshold	SCL, SDA, CTRL, SYNC			1.1	V
Logic input high threshold		2.1			V
Logic pin input capacitance	SCL, SDA, CTRL, SYNC		10		pF
Supported SMBus operating frequency		100		400	kHz
SMBus bus free time	STOP bit to START bit		1.3		µs
SMBus SDA setup time from SCL			100		µs
SMDBus SDA hold time from SCL			0		ns
SMBus START/STOP condition setup/hold time from SCL			600		ns
SCL low period		1.3			µs
SCL high period			0.6	50	µs