flex Power Modules

DESIGN NOTE 006

Using analog isolated power modules in parallel configurations

Abstract

Flex Power Modules offers a very wide selection of power modules encompassing the most commonly desired values of output voltages and power levels. These offerings normally enable the system designer to implement the desired power functions by using one or more power modules in a "stand-alone" or "parallel" configuration. This design note provides an overview of why paralleling is sometimes necessary, the capabilities of the various power module families and suggestions on how to successfully implement such a connection.

Contents

Reasons for paralleling

Many situations demand a load current which is higher than what a single power module can provide. In these cases, two or more power modules may be connected in parallel to meet this current requirement. Using two power modules in parallel, the current available to the load may be effectively doubled.

Why not just use a big power module instead of paralleling two or more? Bigger power modules might be less efficient than their smaller counterparts. Bigger passives will be required, which take up space. Designing power systems is not straightforward, therefore sometimes paralleling is the easier and quicker option. Also, using two smaller DC/DCs in place of one big one will spread the heat dissipated across a larger area on the PCB which improves reliability.

Other reasons for using power modules in parallel include providing redundancy in high-reliability systems. These set-ups use additional DC/DC converters, which means there are always more converters available than required to provide the total load current. If one fails, the same amount of current can still be provided. Popular schemes are N+1 (where there is one redundant converter), N+M or even 2N for high levels of redundancy.

Reducing the number of different power module types used in a system by implementing higher power requirements with lower power modules in parallel is another reason for paralleling.

In the remainder of this design note, we will describe how to implement the parallel connections using our power modules.

Factors affecting ability to parallel converters

Never assume modules can be paralleled. When selecting DC/DC converter modules for an application in which they will be paralleled, it is important to check carefully to ensure that the modules you are looking at are designed for operation in parallel. Not all modern DC/DC converters have this capability or may be limited to paralleling for redundancy rather than current sharing. This should be stated in the manufacturer's datasheets or contact your Flex Power Modules sales representative for advice.

Two DC/DC converters connected in parallel will not automatically share the load equally. Even if they are identical, the output voltages will be slightly different due to component tolerances. The one with the higher output voltage will typically provide the entire load current, operating at its limit while its partner is doing relatively little work.

This will provide the required amount of power, but it it not the preferred optimal.

The converter doing the bigger share of the work will create a thermal hot spot, which could be problematic, and it will have a shorter expected lifetime under these conditions. Forcing DC/DC converters to share the load equally mitigates hot spots and optimizes lifetime for all the modules.

For parallel DC/DC converters operating in redundant configurations, if one module fails, the others must increase their output to compensate. If the modules are loaded unequally and the one providing most of the current fails, its partner must quickly increase its load from minimal to the maximum to compensate, which causes undesirable transients and a temporary drop in the output. Sharing the load equally minimizes the dynamic response required from each converter, which results in less disruption to the output.

Converters that are designed for parallel current sharing generally use one of two types of methods to ensure that any single converter is not overloaded:

- Droop Load Sharing (DLS) – the converter is designed with a "soft" output voltage vs. current characteristic. This causes the output voltage of each converter to automatically adjust downward as its current increases so that each converter approximately shares the total output current.

This is illustrated in Fig. 1 with the slopes and output voltage difference exaggerated to illustrate the concept. As the load current is increased from 0A, V_{OUT1} delivers all the current until V_{OUT1} has drooped to the zero-load voltage for V_{OUT2}. Increasing the current further results in V_{OUT1} and V_{OUT2} delivering the same current with an offset, $I_{OUT2} = I_{OUT1} + I_{Offset}$.

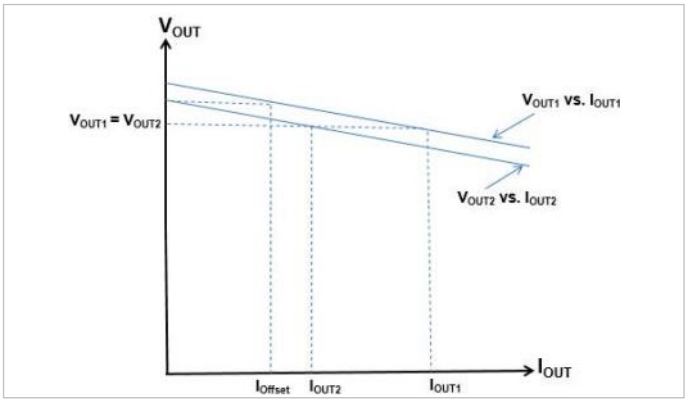

Figure 1: 2 modules in Droop Load Share (DLS) mode

The advantage for DLS is simplicity. The modules are just connected in parallel. The disadvantage is the droop voltage from no load to full load. The load sharing accuracy is based on the unit to unit output voltage setpoint range and the droop slope.

- Active Current Sharing (ACS) – this is normall a more complex design used on higher power converters. A signal line connects the paralleled converters and actively controls their internal switching operation as a function of the sensed current level in each converter, see Fig. 2.

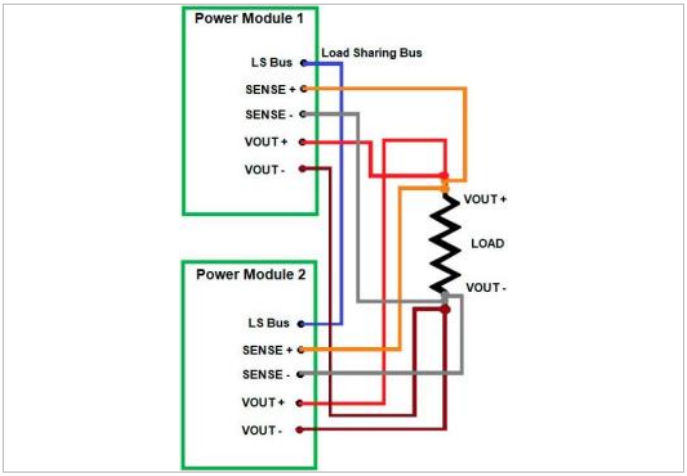

Figure2: Active Current Share (ACS)

Another option exists when using converters without current-sharing provisions but with the capability of external voltage adjustment. There are "load sharing" integrated circuits available that can be connected externally to provide for current sharing by means of adjusting the converter output voltages to achieve the desired sharing of current. The Texas Instruments (TI) UCC29002 and Analog Devices (ADI) LTC4370 are examples of such circuits.

Paralleling capability of power modules

PKE, PKE-A, PKU-A, PKU-E and PKV series of power modules are not recommended for paralleling. PKM4817LNH is designed for very easy paralleling. They use the slope compensation method to achieve current sharing without the need for any external components or connections. The AN318 describes the parallel operation and load sharing of the product in greater detail. It also describes the design considerations to be made in order to optimize the current sharing for maximum output power.

PKB-C, PKB-D, PKJ, PKM-A, PKM-D, PKM-NH (except PKM4817LNH), PKU-C, PKU-D and PKU-S series of power modules rely upon an external current sharing integrated circuit when paralleled. Because of the active rectification used internally to the module to achieve high efficiency, an ORing circuit (diode or MOSFET) must always be used on the output of each module, even when paralleling for increased power. Without this component, the rectifier MOSFET internal to the module will be damaged due to reverse current.

When selecting the ORing circuit, it should be sized to handle the maximum output current of the power module with enough margin to ensure reliability. The best ORing circuit comprises an ORing controller that is fast and accurate in detection and fast in response, together with a MOSFET offering the lowest possible $R_{DS(ON)}$. These attributes allow minimized losses and dependence on thermal management, with smaller size and greater ease of use.

The paralleling capabilities of power modules are found in the Technical Specifications of each product.

Layout and cooling

The outputs should be connected together as close as possible to the load. Never connect diodes or other current blocking devices between the inputs of paralleled products and keep the resistance and inductance between the inputs as low as possible.

The products usually use their pins for cooling by transferring heat to the motherboard. For efficient heat transfer, it is recommended that the pins are connected to copper planes in the motherboard. For best current sharing performance, i.e. for minimizing the output current differences between the current sharing products, it is important to have the same thermal situation for all products. For air-cooled application, the air flow shall be the same for all current sharing products.

Paralleling for Redundancy

So far, we have addressed paralleling of power modules to increase the total power available. Paralleling for redundancy is similar in concept but entails some additional complexity.

It should be noted that parallel configurations only for the sake of redundancy don't necessarily utilize DLS nor ACS.

When paralleling for redundancy, one power module in the paralleled configuration must be capable of failing without disrupting delivery of power to the load. This means that the remaining module(s) must be able to meet the full demand of the load circuits. Also, the failed module must not "pull-down" the voltage buses – either on the input or the output.

The output bus is typically protected using an ORing circuit in series with the output of each power module. These are selected to pass the full output current of the module with derating to give good reliability. In the event of a module failure, this ORing circuit will become back biased and prevent current from the other modules from flowing into the inactive module.

Any common alarm or control circuits on the secondary side of the paralleled power modules should be either isolated or implemented with high impedance components to minimize leakage currents.

Some of the failure modes of a power module result in a short across the input to the module. If no precautions are taken, this short will draw excessive current from the DC intermediate voltage input bus and depress the DC input voltage. This in turns can disrupt power delivery to the remaining modules.

This condition is prevented by using a fuse at the input to each power module that is being paralleled for redundancy The fuse should be sized to conduct the worst-case input current to the module at the lower extreme of the input bus voltage.

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As with paralleling for increased power capability, the power module DC distribution networks should be as symmetrical as possible and the load decoupling capacitors should be located close to the load.

Reference design with TI UCC29002

The UCC29002 device is an advanced and high-performance load share controller that provides all necessary functions to parallel multiple independent DC/DC modules. It is based on the automatic main / secondary architecture. According to the device datasheet, it provides better than 1% current share error between modules at full load by using a very low offset post-package trimmed current sense amplifier and a high- gain negative feedback loop.

This section features the UCC29002 load-share controller and specifically illustrates equal current sharing between two PKB4111C (53V_{DC} to 5V_{DC} power modules), each rated for 12A maximum output current, paralleled to supply a load of up to 24A.

To accurately current share between power modules, specific parameters must be known. Among these parameters are the nominal output voltage of the modules (V_{out}), the maximum output current of each module ($I_{out(max)}$), the maximum voltage adjustment range of each module (V_{adj}) and the transfer function of the power modules between their positive voltage sense and power output terminals.

For this particular example, as stated in the PKB4111C technical specification:

V_{in}= 36-75V | V_{out}= 5V | $I_{out\ (max)}$ = 28 A | $V_{adj\ (max)}$ = 200mV

Step 1: Check bias supply to the device

The UCC29002 requires a bias voltage of 4.375V to turn on, but the bias should not exceed 15V. Due to the 5V output of the modules, direct bias from the output voltage of the modules is possible.

V_{dd}=5V

Note 1: According to the controller's datasheet, V_{ADJ} needs to be greater than V_{EAO} + 1. The value of V_{EAO} is clamped at 3V, so V_{ADJ} needs to be greater than about V. It means that if the output voltage of a module is lower than 4V, this controller cannot be used.

Note 2: For higher-voltage applications (output voltage greater than 15V), use the application solution as recommended in Fig. 3 (use voltage divider by R_{BIAS1} and R_{BIAS2} resistors and the NPN transistor Q1).

Note 3: The NPN transistor's collector-emitter voltage (V_{CEO}) should be larger than the output voltage (and collector current- continuous (I_C) should be greater than 7mA).

Note 4: V_{dd} must be decoupled with a good-quality ceramic capacitor returned directly to GND. The device is optimized for a capacitor value of 0.1 µF to 1 µF.

C_{BIAS} = 0.47 µF

Step 2: Determine the current sense resistor

The selection of the shunt resistor is limited by its voltage drop at maximum module output current. This voltage drop should be much less than the voltage adjustment range of the module. Other limitations for the sense resistor are the desired minimum power dissipation and available component ratings. We assume that desired maximum power dissipation of the current sense resistor is 1W.

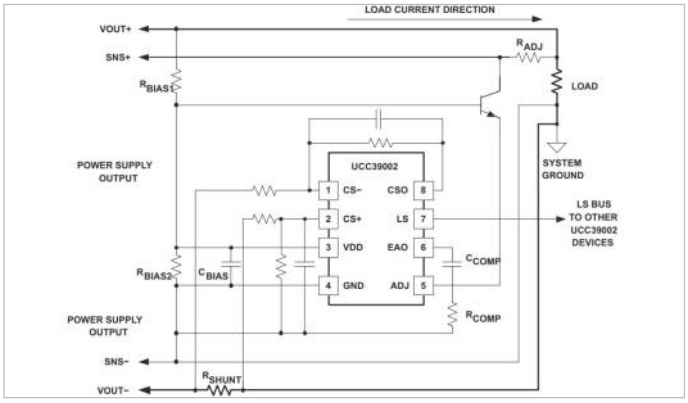

Figure 3: High voltage application (V_{out} is greater than 15V)

$$R_{SHUNT(max)} = \frac{P_{RSHUNT(max)}}{I^2_{OUT(max)}} = 1.275\ m\Omega$$

Standard resistor value used for current sensing is 1 mΩ.

Make sure voltage drop across sense resistor is less than the voltage adjustment range of the module and is much greater than the input voltage offset, 100 µV, of the current sense amplifier.

$V_{RSHUNT} = R_{SHUNT} * I_{OUT(max)} = 28\ mV < 200mV$

Step 3: Set up the current sense amplifier

The voltage at the CSO pin is limited by the saturation voltage of the internal current sense amplifier and must be at least two volts less than V_{dd}.

$V_{CSAO(max)} = V_{dd} - 2 = 3V$

The maximum current sense amplifier gain is

$$A_{CSA(max)} = \frac{R_1}{R_3} = \frac{V_{CSAO(max)}}{R_{SHUNT} * I_{OUT(max)}} = 107.14$$

As can be seen from the above equation (E:5), the gain is equal to R1/R3 and a high-frequency pole, configured with C2, is used for noise filtering. This impedance is mirrored at the CS+ pin of the differential amplifier as shown.

Chosen current sense gain for this design, keeping well below the theoretical maximum calculated above:

$$A_{CSA} = \frac{R_1}{R_3} = 100$$

R1 = R2 = 27.4 kΩ
R3 = R4 = 274 Ω

Add a "high frequency" pole for noise roll-off (assume high frequency pole is 50 kHz):

$$C_1 = \frac{1}{2 * \pi * R1 * f_{pole}} = 116.17\ pF$$

C1 = C2 = 120 pF

Note: The bandwidth of current share loop is generally a few dozen to a few hundred Hz, so the high frequency pole for noise filtering should be larger than 1 kHz. It is recommended to use a value larger than 5 kHz (5 kHz to 100 kHz).

Step 4: Determine the adjust resistor

The +SENSE terminal of the module is connected to the ADJ pin of the load share controller. Placing a resistor between this ADJ pin and the load creates an artificial +SENSE voltage from the voltage drop across R_{ADJ} due to the current sunk by the internal NPN transistor. The voltage at the ADJ pin must be maintained at approximately 1V above the voltage at the EAO pin. This is necessary in order to keep the transistor at the output of the internal adjust amplifier from saturating. To fulfill this requirement, R_{ADJ} is first calculated using below equation.

$$R_{ADJ} \geq \frac{\left(\Delta V_{ADJ(max)} - I_{OUT(max)} * R_{SHUNT}\right) * 500}{\left(V_{OUT} - \Delta V_{ADJ(max)} - 1 - \left(\frac{500 * \Delta V_{ADJ(max)}}{R_{SENSE}}\right)\right)}$$

R_{SENSE} is the internal resistance between +VOUT and +SENSE within the module which is 100 Ω for PKB4111C. Please contact your local Flex sales representative to have the R_{SENSE} of a module.

The actual adjust pin current also needs to be considered. The maximum sink current for the ADJ pin, $I_{ADJ(max)}$, is 7mA as determined by the internal 500 Ω emitter resistor and 3.5V clamp. The value of adjust resistor, R_{ADJ}, is based upon the maximum adjustment range of the module, $\Delta V_{ADJ(max)}$. This adjust resistor is determined using

$$R_{ADJ} \geq \frac{\left(\Delta V_{ADJ(max)} - I_{OUT(max)} * R_{SHUNT}\right)}{I_{ADJ(max)} - \frac{\Delta V_{ADJ(max)}}{R_{SENSE}}}$$

By selecting a resistor that meets both minimum requirements, the ADJ pin will be at least 1V greater than the EAO voltage and the adjust pin sink current will not exceed its 7mA maximum. The previous 2 equations give $R_{ADJ} \geq 30.7\ \Omega$ and $R_{ADJ} \geq 34.4\ \Omega$ respectively. The selected R_{ADJ} value is to meet both requirements.

$R_{ADJ} = 47\ \Omega$

Step 5: Determine the error amplifier compensation components

The total load share loop unity-gain crossover frequency, f_{CO}, must be set at least one decade below the measured crossover frequency of the paralleled modules, $f_{CO(module)}$. It depends mostly on the capacitance connected to modules' output. The Bode plot of the module must be measured to be able to find crossover frequency of the module.

The resultant Bode plot of the loop gain yields a crossover frequency ($f_{CO(module)}$) of 35 kHz for PKB4111C. The unity gain crossover frequency is unique to the module and must be specifically measured for each module type.

For this design, the total load share loop is configured for a unity gain crossover frequency f_{CO} two decades before $T_{CO(module)}$

$f_{CO} = 300$ Hz

Compensation of the transconductance error amplifier is done by placing the compensation resistor (R_{COMP}) and capacitor (C_{COMP}) between EAO and GND. The values of these components are determined by the following loop gain equation.

$$C_{COMP} = \left(\frac{g_m}{2 * \pi * f_{co}}\right) * A_{CSA} * A_v * A_{ADJ} * (|A_{PWR}(f_{CO})|)$$

where:

- g_M is the transconductance of the error amplifier, typically 14 mS, f_{CO} is equal to the desired crossover frequency in Hz of the load share loop (300 Hz for our example)
- A_{CSA} is the CSA gain
- A_V is the voltage gain
- A_{ADJ} is the gain associated with the adjust amplifier
- $|A_{PWR}(f_{CO})|$ is the measured gain of the power module at the desired load share crossover frequency, f_{CO}, converted to V/V from dB

$$A_{CSA} = \frac{R_1}{R_3} = 100$$

$$A_v = \frac{R_{SHUNT}}{R_{LOAD}} = 0.0056$$

$$A_{ADJ} = \frac{R_{ADJ} * R_{SENSE}}{\left(R_{ADJ} + R_{SENSE}\right) * 500} = 0.157$$

$$(|A_{PWR}(f_{CO})|) = 10\left(\frac{G_{MODULE}(F_{CO})}{20}\right)$$

$G_{MODULE}(f_{CO})$ is the measured value of the gain at the desired crossover frequency which is about 20 dB for our example.

$C_{COMP} = 6.53\ \mu F$

Assign a value for C_{COMP} based upon typical available values.

$C_{COMP} = 10\ \mu F$

Once the C_{COMP} capacitor is determined, R_{COMP} is selected to achieve the desired loop response.

$$R_{COMP} = \sqrt{(\alpha^2 - \beta^2)}$$

$$\alpha = \frac{1}{g_m * A_{CSA} * A_V * A_{ADJ} * |A_{PWR}(f_{CO})|}$$

$$\beta = \frac{1}{2 * \pi * f_{CO} * C_{COMP}}$$

Calculate R_{COMP} based on above equation and assign a value for it based upon typical available values.

$R_{COMP} = 61.9\ \Omega$

Note 1: If calculated R_{COMP} is an imaginary value, select another value for C_{COMP}.

Note 2: The design with the UCC29002 is based on applications that use a remote sensing function with the power modules. However, it can be used with a power module which uses an output trim only. For further details, please contact TI.

Reference design with ADI LTC4370

The LTC4370 is a two-supply current sharing controller that incorporates MOSFET ideal diodes. The diodes block reverse and shoot-through currents during start-up and fault conditions. Their forward voltage is adjusted to share the load currents between supplies. Unlike other sharing methods, neither a share bus nor trim pins on the supply are required.

The controller operates with supplies from 2.9V to 18V. For lower rail voltages, an external supply in the 2.9V to 6V range is needed at the VCC pin. For the device to load share, the supplies must be within 500 mV of each other.

This section features the LTC4370 and specifically illustrates equal current sharing between two PKB4113C ($53V_{DC}$ to $12V_{DC}$ power modules), each rated for 12A maximum output current, paralleled to supply a load of up to 24A, see Fig. 4.

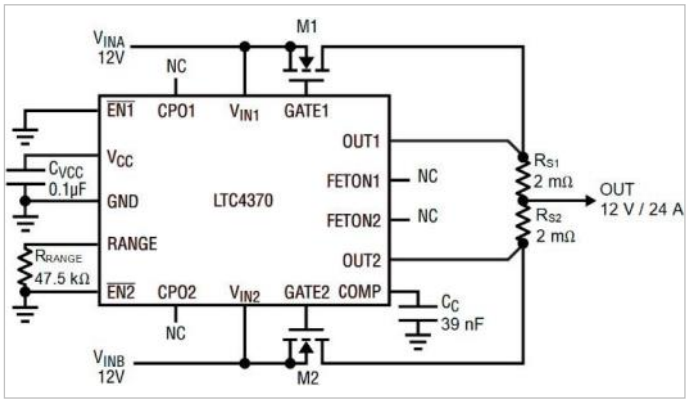

Figure 4: Current sharing using LTC4350

Step 1: Bias supply configuration

The LTC4370 can load share high side supplies down to 0V rail voltage. A 0.1 µF bypass capacitor (C_{VCC}) should also be connected between the VCC and GND pins, close to the device.

Note: If V_{CC} powers up after V_{IN}, and back feeding of V_{CC} by the internal V LDO is a concern, then a series resistor (few 100 Ω) or Schottky diode limits device power dissipation and back feeding of a low V_{CC} supply when any V_{IN} is high.

Step 2: Sense resistor selection

The sense resistor voltage drop dictates the current sharing accuracy. Sharing error, due to the error amplifier input offset, decreases with increasing sense voltage as:

$$\frac{\Delta I}{I_L} = \frac{|I_{OUT1} - I_{OUT2}|}{I_L} = \frac{|V_{EA(OS)}|}{I_L * R_S} = \frac{2mV}{I_L * R_S}$$

I_{OUT1} and I_{OUT2} are the two supply currents, I_L is the load current ($I_{OUT1} + I_{OUT2} = I_L$), R_S is the sense resistor value, and $V_{EA(OS)}$ is the input offset of the internal error amplifier. A 25mV sense resistor voltage drop with half of the load current flowing through A larger sense resistance may also be needed if there is a connector in between the OUT pins and the load to minimize the effect of its resistance. At larger sense voltages the accuracy will be limited by the sense resistor tolerance. If sharing accuracy requirements can be relaxed, power dissipated in the sense resistor can be reduced by selecting a lower resistance.

Let's use a 2 mΩ sense resistor in our PKB4113C example. A 2 mΩ sense resistor drops 48mV at full load and yields an error amplifier offset induced sharing error of about 4% (see Equation 13). At full load, the sense resistor dissipates 1.15 W.

Step 3: MOSFET selection

The LTC4370 drives N-channel MOSFETs to conduct the load current. The important parameters of the MOSFET are its maximum drain-source voltage BV_{DSS}, maximum gate-source voltage $V_{GS(MAX)}$, on-resistance $R_{DS(ON)}$, and maximum power dissipation $P_{D(MAX)}$. If an input is connected to ground, the full supply voltage can appear across the MOSFET. To survive this, the BV_{DSS} must be higher than the supply voltages. The $V_{GS(MAX)}$ rating of the MOSFET should exceed 14V since that is the upper limit of the internal gate to V_{IN} clamp.

To obtain the maximum sharing capture range, the $R_{DS(ON)}$ should be low enough to regulate the minimum forward regulation voltage across the MOSFET while it is conducting half of the load current. If it cannot, the gate voltage will be railed high. Hence, the $R_{DS(ON)}$ value in the MOSFET datasheet should be looked up for 10V or 4.5V gate drive depending on the V_{IN} voltage.
It should be noted that it is also important to design $I_L * R_{DS(ON)}$ below 75 mV for optimum performance.

The peak power dissipation in the MOSFET occurs when the entire load current is being sourced by one supply with the maximum forward regulation voltage dropped across the MOSFET. Therefore, the $P_{D(MAX)}$ rating of the MOSFET should satisfy:

$$P_{D(max)} \geq I_L * V_{FR(max)}$$

$$V_{FR(max)} = 10\ \mu A * R_{RANGE} + V_{FR(min)}$$

I_L is the load current, $V_{FR(max)}$ is the maximum forward regulation voltage, $V_{FR(min)}$ is the minimum forward regulation voltage (12 mV or 25 mV depending on supply voltage levels, see the LTC4370 datasheet) and R_{RANGE} (below 60 kΩ) is decided by the design trade-off between the sharing capture range and the power dissipated in the MOSFET. A larger R_{RANGE} increases the capture range at the expense of enhanced power dissipation and reduced load voltage. On the other hand, supplies with tight tolerances can afford a smaller capture range and therefore cooler operation of the MOSFETs. 2% of 12V is 240mV. The sharing capture range needs to be about 2 * 240mV (±480 mV) to work for most supply voltage differences. A 47.5 kΩ R_{RANGE} sets V_{RANGE} to 475mV. The above equations are used to calculate the maximum forward regulation voltage:

$V_{FR(max)} = 10\ \mu A * 47.5\ k\Omega + 25mV = 500mV$

$P_{D(max)} = 12W$

Enough PCB area with airflow needs to be provided around the MOSFET drain to keep its junction temperature below the maximum.

Calculate the $R_{DS(ON)}$ of the MOSFET to achieve the desired forward drop at full load.

$$R_{DS(ON)} \leq \frac{V_{FWD}}{I_L}$$

V_{FWD} is forward voltage drop ($V_{FW}D$ = VIN – OUT) and I_L is the load current.

Assuming a VFWD of 50 mV:

$$R_{DS(ON)} \leq \frac{50mV}{24\ A} = 2.08\ m\Omega$$

The BSC009NE2LS5 offers a good solution with a 0.9 mΩ $R_{DS(ON)}$, 25V BVDSS and 16V $V_{GS(MAX)}$.

Since 0.5 * I_L * $R_{DS(ON)}$ is 10.8mV, it is able to regulate the 25mV minimum forward regulation voltage leading to the maximum possible sharing range set by V_{RANGE}.

Step 4: CPO and COMP Capacitors Selection

As mentioned above, the maximum MOSFET voltage drop can be set with a resistor. A fast gate turn-on reduces the load voltage droop during supply switchover. If the input supply fails or is shorted, a fast turn-off minimizes reverse current transients.

The recommended value of the capacitor between the CPO and VIN pins is approximately 10 times the input capacitance (C_{ISS}) of the MOSFET. A larger capacitor takes a correspondingly longer time to be charged by the internal charge pump. A smaller capacitor suffers more voltage drop during a fast gate turn-on event as it shares charge with the MOSFET gate capacitance. In our example, since a 12V supply is large enough to tolerate a diode drop, fast gate turn-on is not needed. Hence, the CPO capacitor is omitted.

Step 5: Loop Stability

The load sharing control loop is compensated by the capacitor from the COMP pin to ground. This capacitor should be at least 50 times the input capacitance (C_{ISS}) of the MOSFET.

A larger capacitor improves stability at the expense of increased sharing closure delay, while a smaller capacitor can cause the two supply currents to switch back and forth before settling. The COMP capacitor can be just 10 times C_{ISS} when a CPO capacitor is omitted, i.e., when fast gate turn-on is not used.

In our example, since fast turn-on is not used (the CPO capacitor is omitted) and the input capacitance, C_{ISS}, of the MOSFET is 3900 pF, the COMP capacitor CC can be just 10 times CISS at 39 nF.

Input & output capacitance for pulsed loads

For pulsed loads, the load current will be shared every cycle at frequencies below 100 Hz. At higher frequencies, each cycle's current may not be shared but the time average of the currents will be. Bypassing capacitance on the inputs should be provided to minimize glitches and ripple. This is important since the controller tries to compensate for the supply voltage differences to achieve load sharing. Enough load capacitance should also be provided to enhance the DC component of the load current presented to the load share circuit. It is also important to design $I_L * R_{DS(ON)}$ below 75mV as mentioned earlier.

Note: By cascading the shared output of one LTC4370 with another LTC4370, three or more supplies can be efficiently controlled to provide equal current to the load. For more information, please contact Analog Devices.

Summary

Several power module families are designed to provide good performance when paralleled. The information contained here will enable the system designer to take advantage of these capabilities and easily develop parallel configurations of power modules that are reliable and manufacturable.

For additional information or for assistance with specific situations not addressed here, please contact your local application engineer or email to pm.support@flex.com

flex Power Modules

Flex Power Modules, a business line of Flex, is a leading manufacturer and solution provider of scalable DC/DC power converters primarily serving the data processing, communications, industrial and transportation markets. Offering a wide range of both isolated and non-isolated solutions, its digitally-enabled DC/DC converters include PMBus compatibility supported by the powerful Flex Power Designer.

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