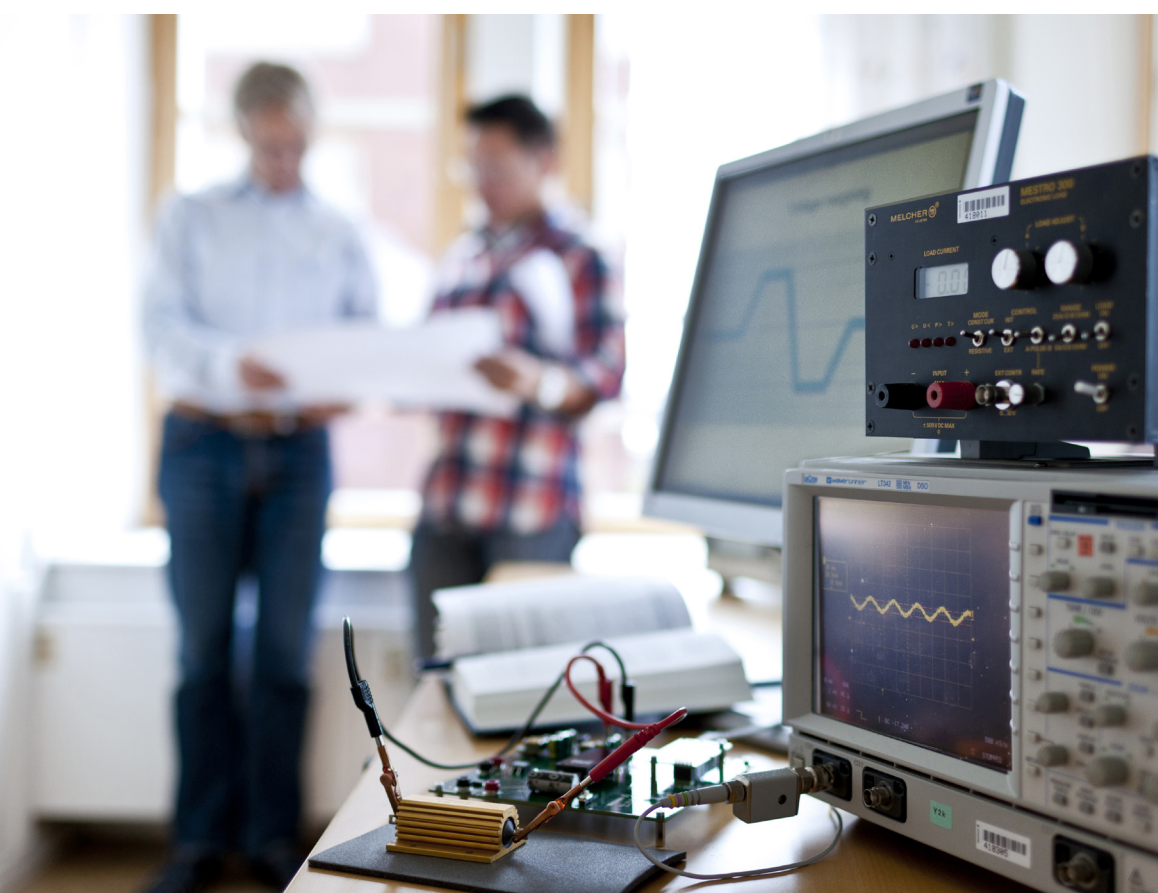


Powering FPGAs Using Digitally Controlled Point of Load Converters



Design Note 030

Flex Power Modules

Abstract

Field Programmable Gate Arrays (FPGAs) require several high quality power supply lines. Designers experience the following challenges when designing FPGA power solutions:

- low voltage and high current capability needed to power the core logic
- lack of accurate information regarding the maximum current consumption (I/O and core)
- high demands regarding the voltage tolerance
- power up and power down sequencing
- monotonic ramp up
- minimum and maximum ramp up time
- transient distortions due to rapid current changes

In addition, several FPGAs have configurable transceivers that can require “on-the-fly” reconfigurable I/O voltages. In the near future, the core voltage will also be configurable to offer the option of dynamically saving energy.

All of these challenges are much easier to accommodate when using digital power technology. Moreover, using digitally-controlled DC/DC converters dramatically reduces the time taken to design the FPGA’s power supply system.

Typical power requirements

FPGA power consumption consists of a static part and a dynamic part . The static part is primarily due to bias and leakage currents, while the dynamic part depends heavily on the individual circuit design, the chosen clock frequency, and I/O voltage selection. All FPGA vendors provide special simulation tools for estimating power needs. We strongly recommend estimating power consumption using the tools first. Actual power consumption can differ slightly from the estimate; also, the power demand during startup can be slightly higher than expected. Suitable power margins should be chosen to provide sufficient power and to accommodate any future FPGA content updates.

We will now focus on designing power supplies to satisfy the FPGA’s core logic voltage and I/O voltage requirements. These two rails require relatively high current capabilities together with appropriate ramp-up parameters.

The tables on the next page present the power requirements for two examples of a single FPGA.

Virtex 6 from Xilinx

Power Supply	Nominal Voltage [V]	Voltage tolerance [%]	Current consumption [A]	Sequencing order
Internal Vccint	0.90 / 1.00	+/- 5	4 - 21	1
Input / Output Vcco	1.2/1.5/1.8/2.5/3.3	+/- 5	3 - 10	3*
Auxiliary Vccaux	2.5	+/- 5	0.3 – 1.5	2*

* Vcco and Vccaux may also rise simultaneously

Stratix IV from Altera

Power Supply	Nominal Voltage [V]	Voltage tolerance [%]	Current consumption [A]
Core & periphery Vcc, PLL digital Vccd_pll	0.90 / 0.95	+/- 3	16
Auxiliary Vccaux, Differential clock Vccclkin, Pre-driver Vccpd, Configuration pins Vccpgm, Input/Output Vccio, analog PLL Vcca_pll	2.5	+/- 5	3
Programmable power technology Vccpt	1.50	+/- 3	0.3

Digitally controlled software configurable Point of Load converters

The BMR450 and the BMR451 series of digitally-controlled point-of-load regulators (POLs) are PMBus-configurable non-isolated DC/DC converters. The maximum output current of these products is 20 A and 40 A respectively. The input voltage range is from 4.5 V to 14 V. Both products are equipped with a PMBus interface. Detailed information is available in each product's Technical Specification.

BMR450/451 series POLs can be specially configured to meet challenging FPGA power requirements. A suitable configuration may be programmed into the product's nonvolatile memory at the vendor's factory (separate product codes will be required) or by the user when the application board is being manufactured. In the latter case, a standard product variant may be used for several applications. The required output voltage, startup, and control loop parameters may be configured via the PMBus interface during the manufacturing ATE test process.

No additional host controller is required for the digital POLs to operate. If the user wants to monitor the output voltage and current or the temperature of the product when operating in the field, the application board should have some form of PMBus manager that communicates with the BMR450/451 devices. There are several ways to implement a PMBus manager: using a dedicated simple microcontroller, a spare circuit block in an FPGA, or blocks in an existing Board Management Processor.

Output voltage accuracy and flexibility

The absolute output voltage accuracy of the BMR450 and the BMR451 is better than +/- 1.5% including temperature variations and ageing. The minimum output voltage of both products is 0.6 V. The maximum output voltage of the BMR450 is 5.5 V. The maximum output voltage of the BMR451 is 3.6 V. These parameters will meet the most demanding FPGA power specification.

The output voltage may even be adjusted "on-the-fly" (that is, during operation) via the PMBus interface. This feature may be used when needing to change the I/O voltage - such as when reconfiguring the functionality of new FPGAs (e.g. Stratix V) - or when it is possible to change the FPGA's core voltage during operation to decrease its power consumption.

Setting the startup and shutdown parameters

The startup delay and ramp up times of the BMR450/451 may be easily and precisely set using simple PMBus commands, and the shutdown parameters may be similarly configured. The Remote Control (on/off) pins of all devices can be connected together and driven from a reset circuit. Each device will then start in a controlled way, providing the necessary sequencing. A monotonic or even a linear ramp-up is guaranteed, see figure 1.

If a controlled shutdown is required, the products should be turned off using the Remote Control pins prior to shutting down the supply voltage. For more information regarding the limitations of the startup and shutdown parameters including accuracy, see the BMR450/451 Technical Specifications.

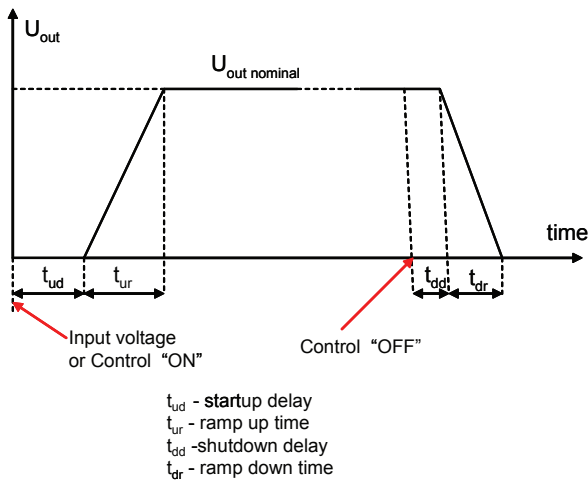


Figure 1: Configurable startup and shutdown parameters

Reducing load transient distortions

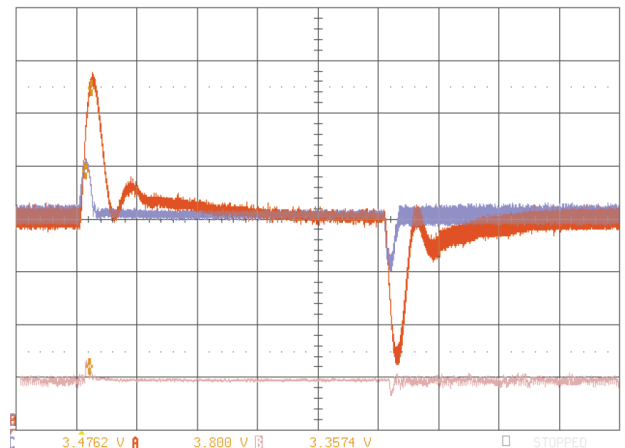
The current that an FPGA's core logic and I/O circuits consumes can change very quickly, resulting in significant distortions of the corresponding supply voltage (undershoots when the current suddenly increases and overshoots when the current promptly decreases). Most often, banks of capacitors are used to lower these load transient distortions below an acceptable level.

Recently, new technologies allow a degree of transient distortion reduction by adding a specific resistor/capacitor combination that matches the circuit's output load capacitance to some analog-controlled POL regulators. The resistor/capacitor pair becomes part of the control loop. This analog technology can

reduce the number of capacitors that are necessary to keep transient distortions within an FPGA's specification.

Similarly, the dynamic performance of digitally-controlled POLs can be significantly improved if the control loop is specially configured to match the external output capacitance and the circuit's effective ESR. In other words, the number of external capacitors that are necessary to reduce the load transient response of the BMR450/451 can be much lower if - instead of using the standard control loop configuration - the customer decides to use a specific, optimized configuration.

Moreover, the BMR450/451 feature an additional feedback mechanism - the nonlinear regulation function. This regulation mechanism is not active during static load conditions, but when a sudden load current change occurs that results in a significant output voltage distortion, the nonlinear regulation block overrides the normal switching control loop to prolong the ON time of the upper or lower side switch. This happens during the same switching cycle as the output deviation occurs. This nonlinear regulation technique dramatically reduces load transient distortions, see figure 2.



Output voltage 3.3 V
Current step: 20-5-20 A
External output capacitance 1 x 470 μ F (OS-CON)

Figure 2: Load step responses for the BMR450. Red curve - standard configuration; blue curve - configuration optimized for output load capacitance. The lower curve shows the reduction in load transients that result from an optimized control loop and the nonlinear regulation function also being active.

Design Example

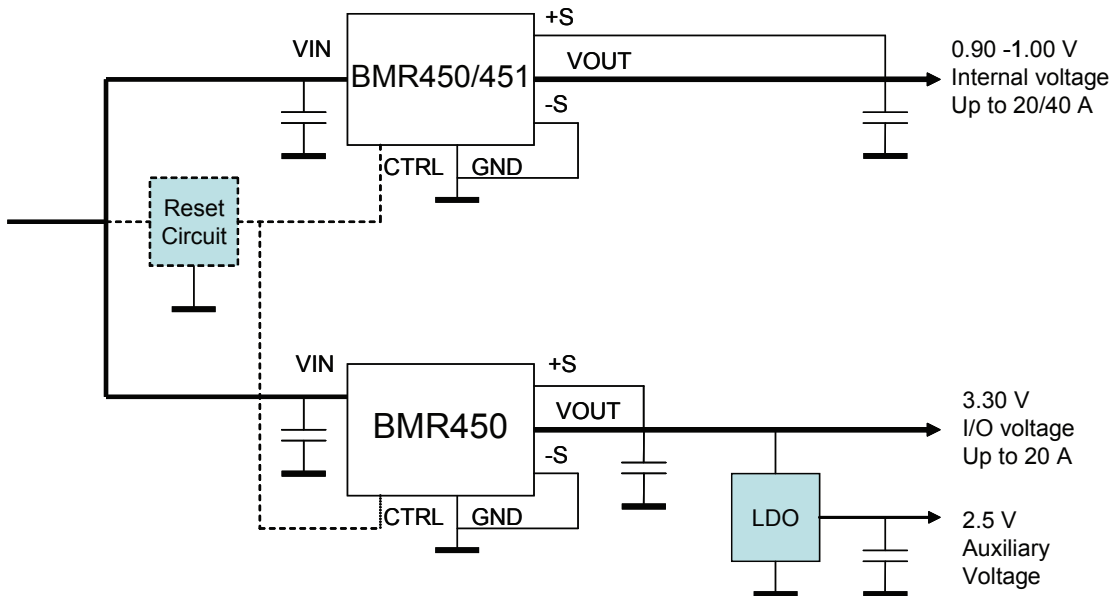


Figure 3: Example of power solution for Virtex 6 FPGA family

Virtex 6 family FPGAs require that the internal core voltage V_{ccint} comes up first. Then, the I/O voltage V_{cco} and the auxiliary voltage V_{ccaux} may come up simultaneously. To achieve proper sequencing, the product that provides the internal core voltage must have a shorter startup delay time than the product that sources the I/O and auxiliary voltages. The BMR450/451's default startup delay time is 20 ms and the ramp up time is 10 ms. It is sufficient to reconfigure the product that provides the I/O voltage to a longer startup delay time, e.g. 40 ms.

The reset circuit is optional. If not used, the minimum input voltage settings must be equal and the ramp up time of the bus voltage should not be too long. Note that contrary to the INHIBIT input of POLA regulators, the CTRL input of the BMR450/451 is TTL-level compatible. No low leakage FET is required between the reset circuit and the CTRL pins.

The minimum value of the input capacitors is 470 μ F, for more information see the BMR450/451's Technical Specifications. The minimum output capacitance depends on the maximum expected load current step and on the control loop settings. Optimized control loop

settings result in significantly lower load capacitance requirements. Control loop optimization requires special design tools that are available from Flex. If the required output I/O voltage is lower than 2.5 V, a small switched POL (e.g. PMD41180 or PMD81180) driven directly from the supply voltage (IBC bus voltage) should be used. If the input bus is 5.0 V and the required auxiliary current is below 500 mA, using an LDO may also be considered.

If 2.5 V I/O voltage is used, the auxiliary voltage can be provided directly from the I/O line product, but a filter (e.g. a small inductor) should be used.

Formed in the late seventies, Flex Power Modules is a division of Flex that primarily designs and manufactures isolated DC/DC converters and non-isolated voltage regulators such as point-of-load units ranging in output power from 1 W to 700 W. The products are aimed at (but not limited to) the new generation of ICT (information and communication technology) equipment where systems' architects are designing boards for optimized control and reduced power consumption.

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