Technical Paper 021

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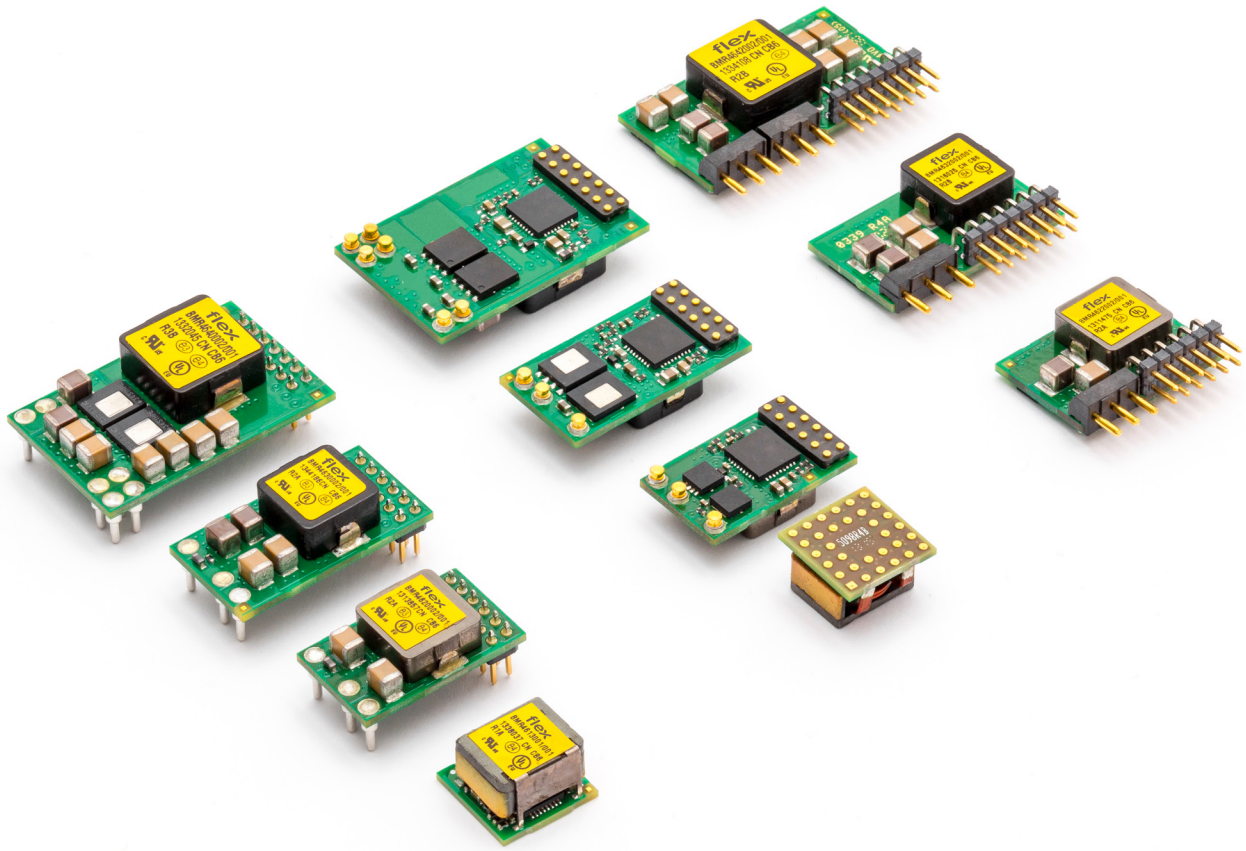
Complex Power Relationships Without All The Wires – 3E Point Of Load Regulators

CONTENTS



Abstract

In traditional power systems, requirements for system relationships such as sync clocking, sequencing, and high-current needs are codified within the design of the board, meaning any changes to the system requirements means changes to the board design. With Flex 3E Point Of Load though, the wires previously required for complex power relationships can be replaced with shared digital buses and configuration software instead.

Designing with Digital Power

Synchronization and Phase Spreading

First, let's start with the sync clock, required for any switching power system. When you have multiple rails or phases in a power system, you first need them to stay in sync. Typically this requires an external clock to drive the power modules, but a digital power system offers the option to let a digital power device output its own external clock to other phases and rails in the system. Once all the devices are using the same sync clock, then next concern for the power system is to spread the clock phase offsets across the devices to reduce peak power draw and EMI noise. With digital power, this is done just by defining the number of devices on the sync clock and assigning positions to each device. This means the system designer doesn't have to think about calculating individual phase offset angles. More information can be found in chapter Synchronization and Phase Spreading (page 4).

Sequencing Configuration

The next concern of a power system is sequencing. Today's processors and FPGAs require multiple rails with specific timing requirements for power-up and ramping. Usually sequencing is setup by committing to a board design beforehand that daisy-chains Power Good pins from one device to the Enable pin of the next device. On newer digital devices though, sequencing can instead be done over a one-wire digital bus shared across all devices, configured with PC software or in-system software. This enables flexibility in the sequencing setup after the power system has already been designed -- this is useful for modular setups, test boards, or to save one from another board revision due to incorrect sequence wiring. The one-wire buses on these devices are also used to sequence backwards - i.e. they are also used to relay faults from one rail to others for a safe power-down. More information can be found in chapter Sequencing Configuration (page 11).

Parallel Operation With Load Sharing

Finally, for high-current rails the digital power way provides a role in simplifying your BOM. Typically for a high-current rail, a different device model with multiple synchronized gate outputs must be purchased. Newer digital devices, however, can meet high-current needs by tying the output of multiple lower-current devices together and configuring them for parallel operation. The devices coordinate parallel operation across the same one-wire bus that's used for sequencing. More information can be found in chapter Parallel Operation With Load Sharing (page 23).

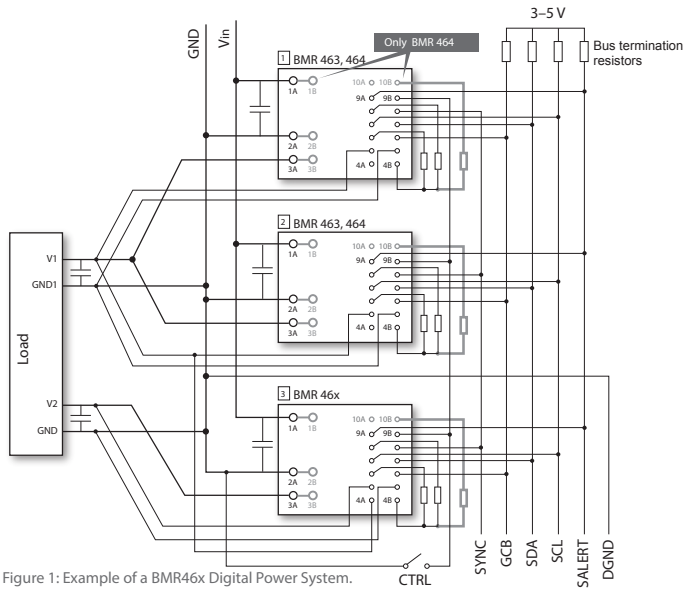


Figure 1: Example of a BMR46x Digital Power System.

In this example of a typical system that uses the BMR46x series, regulators no 1 and no 2 are in current sharing mode (only BMR463 and BMR464) supplying rail V1 with up to 80 A. Regulator no 3 is in voltage tracking mode, making rail V2 track rail V1. All three regulators are synchronized via the SYNC signal, which can be generated internally or taken from an external source. Using phase spreading will reduce the current ripple on input rail Vin.

The Group Communication Bus (GCB) handles current-share information between regulator no 1 and regulator no 2. It also handles fault spreading between all three regulators.

Chapter 1

Synchronisation and Phase Spreading

Synchronized Clock Sourcing

Synchronization of products to a single clock source can be realized by one of two methods:

1 External single clock source. The common switching clock is sourced from an external clock source within the system. The SYNC pin of each product in the group is configured as an input. See illustration in Figure 1.

2 Internal single clock source. One of the products in the group is configured to source the common switching clock by setting the SYNC pin to an output state. The SYNC pin of all other products in the group is configured as an input. See illustration in Figure 2.

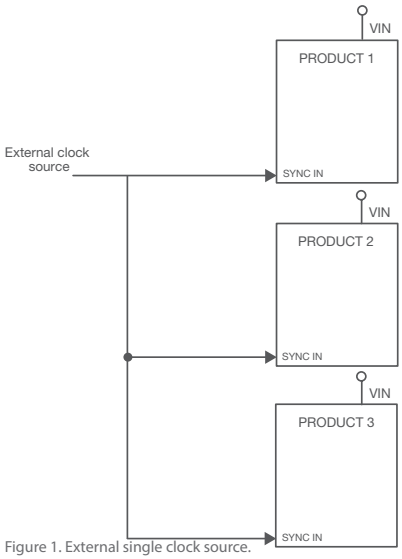


Figure 1. External single clock source.

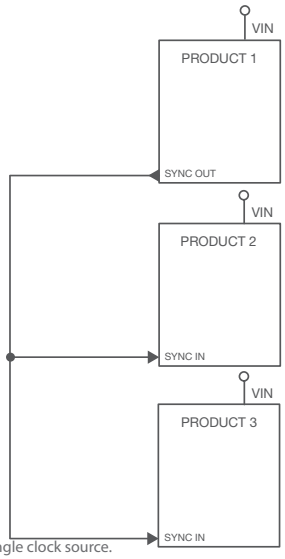


Figure 2. Internal single clock source.

Configuration of SYNC pin

The SYNC pin can be set in one of three different modes:

SYNC Input
The product will check for a clock signal on the SYNC pin each time the product is enabled. The internal oscillator will then synchronize with the rising edge of the external clock. The incoming clock must fulfil the frequency and performance requirements as specified in the Technical Specification of the product and must be stable when the product is enabled. In the event of a loss of the external clock signal, the output voltage may show transient over- and undershoots.

Note: If all products (connected to the same clock signal) are configured for SYNC Input and no external clock source is present, the output voltage of products will not ramp-up due to the lack of a clock signal for switching.

SYNC Output
The product will run from its internal oscillator and will drive the resulting internal oscillator signal onto the SYNC pin so that other products can be synchronize to it. The signal drive can be either push/pull or open drain. The SYNC pin will not be checked for an incoming clock signal while in this mode.

Note: If more than one product (connected to the same clock signal) is configured for SYNC Output, the clock signal will become distorted, resulting in unstable output voltage of the products using the clock signal.

SYNC Auto Detect (default)
In auto detect mode the product will automatically check for a clock signal on the SYNC pin when the product is enabled. If a clock signal is present, the internal oscillator will then synchronize to it as described for SYNC Input. If no incoming clock signal is present the internal oscillator will run freely. The SYNC mode is configured through the PMBus commands MFR_CONFIG and USER_CONFIG according to table 1. See AN302 for details on these commands.

To use synchronization with the BMR450/451 products the POL_ADJ_CONFIG command must be set to 0x00 in order to define the FLEX pin as a SYNC pin. Otherwise the internal oscillator will always be used and the bits in USER_CONFIG and MFR_CONFIG have no effect. When defined as a SYNC pin the FLEX pin can no longer be used for voltage adjust.

SYNC pin configuration	USER_CONFIG		MFR_CONFIG
	Bit 6	Bit 5	Bit 0
SYNC Auto Detect (default)	0	0	N/A
SYNC Input	1	0	N/A
SYNC Output Push/Pull	0	1	1
SYNC Output Open Drain	0	1	0

Table 1. SYNC mode configuration.

If SYNC pin is configured as Output (Push/Pull or Open Drain) it is possible to control the behaviour of the SYNC output during disable, through bit 11 in USER_CONFIG:

USER_CONFIG Bit 11	Function
0 (default)	SYNC pin output remains on after output is disabled
1	SYNC pin output remains on for 500ms after output is disabled

Note: The setting of bit 11 in USER_CONFIG has no effect when Precise Ramp-Up Delay is activated (MISC_CONFIG[7] = 0) for BMR462, BMR463 or BMR464, which is the default setting. In that case SYNC output always remains on after output is disabled.

Configuration of Switching Frequency

The frequency of the product's internal oscillator is set by the PMBus command FREQUENCY_SWITCH as described in AN302. For possible range of frequency see the Technical Specification of the applicable product. If an external clock signal is used (SYNC pin configured as input) the value of the FREQUENCY_SWITCH command must match the frequency of the applied external clock.

Note: The switching frequency read back using the PMBus command READ_FREQUENCY could differ slightly from the set value due to hardware quantization.

Configuration of Phase Spreading

By using the PMBus command INTERLEAVE it is possible to define a specific phase offset for each product, achieving a distribution of phase edges in time. A prerequisite is that all the products involved are synchronized to a common clock as described in the sections above.

The INTERLEAVE command includes three pieces of information:

Bits [15:12] Not used
Bits [11:8] Group ID Number, 0-15
Bits [7:4] Number In Group, 0-15
Bits [3:0] Interleave Order, 0-15

The Group ID Number can be used to assign different ID numbers if there are several phase spreading groups. However the Group ID Number has no impact on the phase offset.

Example 1
Table 2 and Figure 3 and describes a phase spreading configuration of three standalone products. The offsets are chosen to spread the phases evenly along the time line.

The phase offset is defined by the Number In Group value together with the Interleave Order and can be expressed in degrees or time according to the formulas below.

$$Offset(°) = 360 \times \frac{Interleave\_Order}{Number\_in\_group}$$

$$Offset(s) = T_{SW} \times \frac{Interleave\_Order}{Number\_in\_group}$$

where $T_{SW} = 1/F_{SW}$ is the switching period.

Note: If Number In Group = 0 a value of 16 shall be used for Number_In_Group in the formulas.

Product	Number in Group	Interleave Order	INTERLEAVE command	Phase Offset	
Product 1	3	0	0x0030	0	0
Product 2	3	1	0x0031	120°	1/3 x T_{SW}
Product 3	3	2	0x0032	240°	2/3 x T_{SW}

Table 2. Phase spreading example with three products.

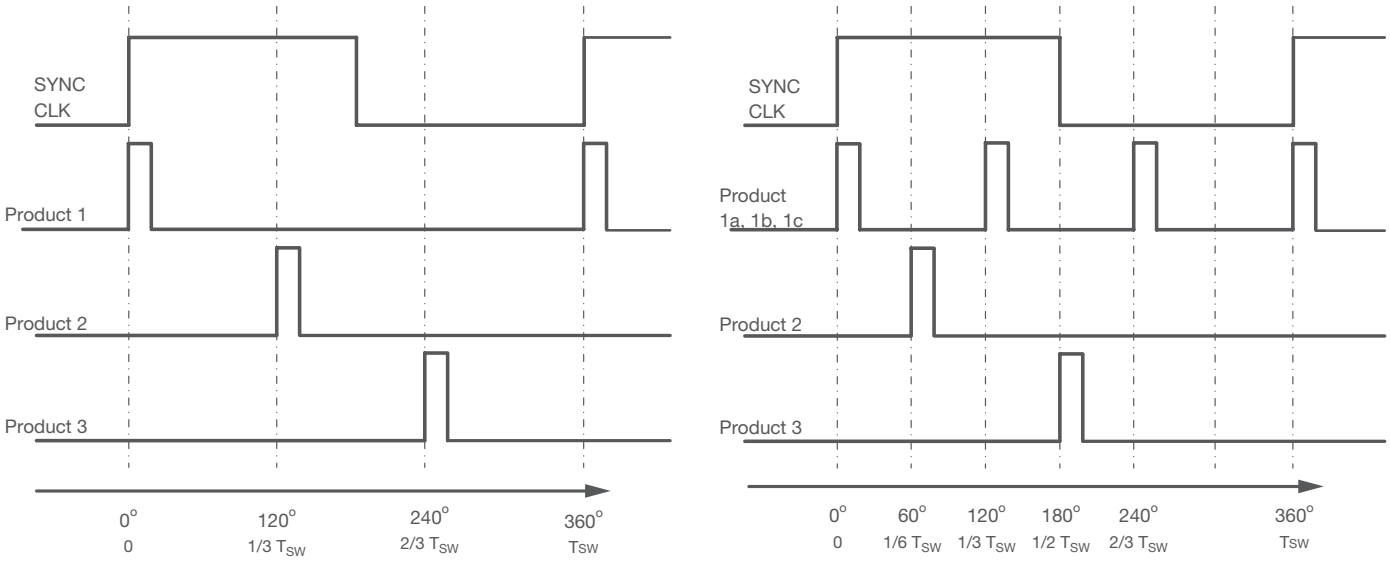


Figure 3. Phase spreading example with three products.

Example 2

Table 3 and Figure 4 describes a phase spreading configuration of five products of which three of them (Product 1a, 1b, 1c) are operated as a current sharing group. For products within current sharing groups the phase offset is set automatically without the need to use the INTERLEAVE command. The offsets can still be adjusted by the INTERLEAVE command but the offset difference between products within the current sharing group is always maintained. See AN307 for more details.

Product	Number in Group	Interleave Order	INTERLEAVE command	Phase offset	
Product 1a (parallel operation)	0	0	0x0000	0°	0
Product 1b (parallel operation)	0	0	0x0000	120°	1/3 x T_{SW}
Product 1c (parallel operation)	0	0	0x0000	240°	2/3 x T_{SW}
Product 2	6	1	0x0061	60°	1/6 x T_{SW}
Product 3	2	1	0x0021	180°	1/2 x T_{SW}

Table 3. Phase spreading example with five products.

Offset Resolution

For the applicable products the actual phase offset is limited to 16 possible values in 22.5° steps as illustrated in Figure 5. The real offset will be rounded to the closest 22.5° increment. Table 4 shows the actual offsets for Example 1 above.

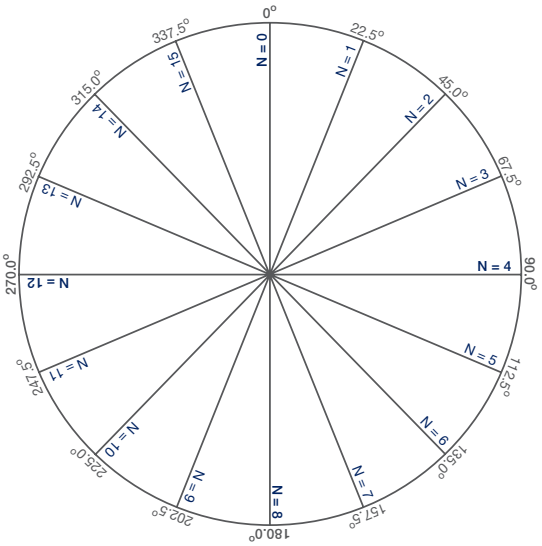


Figure 5. Phase offset resolution wheel.

	Ideal Offset	Actual Offset
Product 1	0º	0º
Product 2	120º	112.5º
Product 3	240º	247.5º

Table 4. Ideal vs actual offset.

Configuration Example

Below is a configuration example of four products in a phase spreading setup. The configuration is made using a PMBusCLI command batch file. Alternatively each command value can be set using the 3E GUI. The configuration procedure can be divided into parts:

1 Restore default configuration from Default Flash memory. This loads the factory settings of the modules.

2 Make configurations of SYNC pins.

3 Make configurations for phase spreading.

4 Make general configurations. Settings are added here only if changing values set by pin-strap (Vout, Vout max, Vout OV/UV thresholds, PG threshold, margin levels) or values set in default configuration (PG delay, rise/fall times, Vin/Iout/Temp thresholds, fault responses, PID taps etc).

5 Store complete configuration to User Flash memory.

```
@ECHO OFF

REM     Configuration file example for phase spreading of four products

REM     Products:
REM     BMR462 at address 0x20
REM     BMR463 at address 0x21 and 0x22
REM     BMR464 at address 0x23
REM
REM     BMR462 product at address 0x20 is configured to output SYNC

REM     Restore default configurations

PMBusCLI /productname=BMR462 /sendbytecommand /address=0x20 /command=RestoreDefaultAll
PMBusCLI /productname=BMR463 /sendbytecommand /address=0x21 /command=RestoreDefaultAll
PMBusCLI /productname=BMR463 /sendbytecommand /address=0x22 /command=RestoreDefaultAll
PMBusCLI /productname=BMR464 /sendbytecommand /address=0x23 /command=RestoreDefaultAll

REM     Configure SYNC pin as push/pull output for product at 0x20
REM     Configure SYNC pin as input for products at 0x21, 0x22 and 0x23

PMBusCLI /productname=BMR462 /writecommand /address=0x20 /command=UserConfig /data=0x0041
PMBusCLI /productname=BMR462 /writecommand /address=0x20 /command=MfrConfig /data=0x7F01

PMBusCLI /productname=BMR463 /writecommand /address=0x21 /command=UserConfig /data=0x0021
PMBusCLI /productname=BMR463 /writecommand /address=0x22 /command=UserConfig /data=0x0021
PMBusCLI /productname=BMR464 /writecommand /address=0x23 /command=UserConfig /data=0x0021

REM     Configure phase spreading, 90 degrees between each product

PMBusCLI /productname=BMR462 /writecommand /address=0x20 /command=Interleave /data=0x0040
PMBusCLI /productname=BMR463 /writecommand /address=0x21 /command=Interleave /data=0x0041
PMBusCLI /productname=BMR463 /writecommand /address=0x22 /command=Interleave /data=0x0042
PMBusCLI /productname=BMR464 /writecommand /address=0x23 /command=Interleave /data=0x0043

REM     General configurations

..............

REM     Store to User flash memory

PMBusCLI /productname=BMR462 /sendbytecommand /address=0x20 /command=StoreUserAll
PMBusCLI /productname=BMR463 /sendbytecommand /address=0x21 /command=StoreUserAll
PMBusCLI /productname=BMR463 /sendbytecommand /address=0x22 /command=StoreUserAll
PMBusCLI /productname=BMR464 /sendbytecommand /address=0x23 /command=StoreUserAll
```

Chapter 2

Sequencing configuration

General Information About the Global Communication Bus (GCB)

Several of the Flex Power Modules 3E products utilize a dedicated serial bus (the GCB bus) to synchronize and communicate real-time events. A 5 bit address is assigned to each GCB rail, yielding a theoretical total of 32 separate power rails, including current sharing rails (Note that each product within a current sharing rail is assigned the same GCB address thus the total number of GCB products can exceed 32). Ensure that the GCB signal integrity is maintained when using a large product count. During GCB events, all products will receive messages; however, only those products configured to respond will do so. GCB products can also transmit events if their programmed algorithm requires inter module communication. Some examples include fault spreading, sequencing, phase add/drop, broadcast margin and broadcast enable.

Multiple sequencing groups can communicate and connect to the same GCB bus.

Method One – Time Based Sequencing

Time based sequencing allows supply output ramp-up and ramp-down sequencing based on the programmed soft start delay times. The CTRL pins for all products in the sequencing group are tied together. This requires that the ON_OFF_CONFIG register is set to 0x16 (or other value as CTRL can be set as Active High or Active Low). The start-up and shut-down sequence is determined by the soft start/stop delay settings. Figure 1 shows three products prepared for time based sequencing.

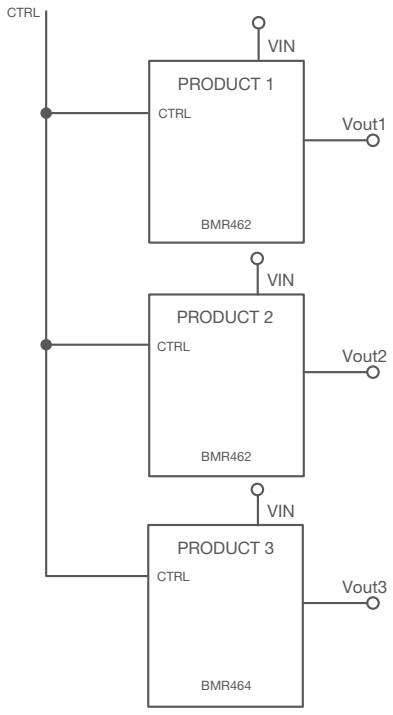


Figure 1. Time based sequencing example.

The configuration procedure for time based sequencing is straightforward. It only includes configurations of four registers, TON_DELAY, TON_RISE, TOFF_DELAY, and TOFF_FALL for all products/rails in the sequencing group.

The accuracy of the timing is defined by the accuracy of the delay and ramping timing and is specified in the product's Technical Specification. It can be affected by enabling Precise timing, i.e. MISC_CONFIG[7] set to 0 (BMR46x only). Please, see the product's Technical Specification for further information about precise timing and default settings.

Example 1

Table 1 and 2 describe a time based up-sequencing configuration and down-sequencing of three rails.

	Delay [ms] TON_DELAY	Rise [ms] TON_RISE
Vout1_2.5V	10	20
Vout2_1.2V	10	10
Vout3_1.0V	15	30

Table 1. Time based up-sequencing example with three output rails.

	Delay [ms] TOFF_DELAY	Rise [ms] TOFF_FALL
Vout3_1.0V	10	30
Vout2_1.2V	10	10
Vout1_2.5V	10	20

Table 2. Time based down-sequencing example with three output rails.

Instead of using the CTRL pin, the PMBus OPERATION command can be used. This requires that the ON_OFF_CONFIG register is set to 0x1A (or other value as CTRL can be set as Active High or Active Low). When using the OPERATION command, the Group Command Protocol as described in PMBus Specification Part II, rev 1.2, Sec 5.2.3, can also be used.

Method Two – Event Based Sequencing

Overview

GCB based and Event based sequencing of power rails are both methods of sequencing where the output of one rail provides the signal to start another rail. In the Event based sequencing the power good (PG) signal from one product is tied to the enable pin (CTRL) of the next product and is repeated throughout the sequence.

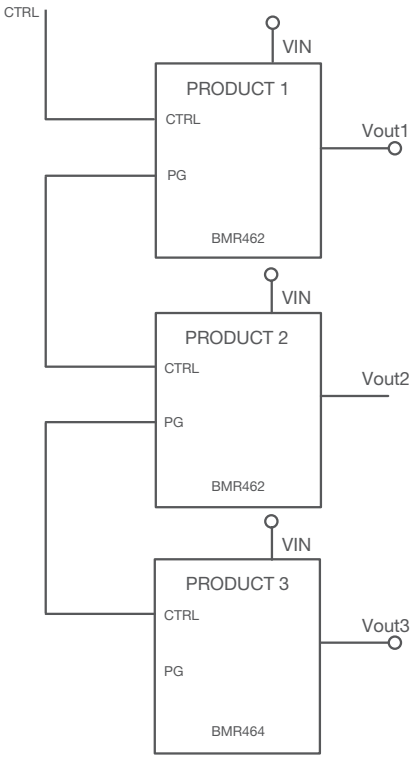


Figure 2 Event based sequencing example. A change of sequencing order will require a hardware re-configuration.

Using the Event based method, i.e. connecting PG to CTRL, as shown in Figure 2, the same order for start-up and shut-down are provided. This method requires a hardware modification if the sequence order is changed.

Configuration

The effect of different settings in the products generating, for example Vout1 and Vout2 are illustrated in Figure 3a-b. Note that the up-sequencing parts as described in Figure 3a are valid for both Event and GCB based sequencing.

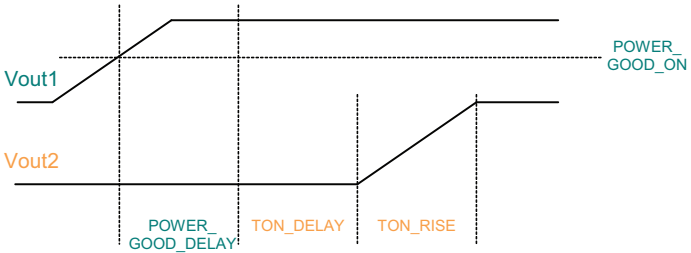


Fig 3a GCB and Event based up-sequencing – Illustration of which settings to be made in which rail. The total time between the Preceding rail, Vout1, and the following rail, Vout2, is determined as follows: Vout1 are configured using POWER_GOOD_ON and POWER_GOOD_DELAY while Vout2 are configured using TON_DELAY and TON_RISE.

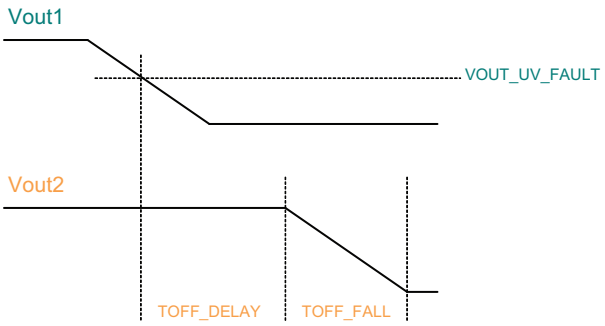


Fig 3b Event based down-sequencing – Illustration of which settings to be made in which rail. The total time between the Preceding rail, Vout1, and the following rail, Vout2, is determined as follows: Vout1 are configured using VOUT_UV_FAULT while Vout2 are configured using TOFF_DELAY and TOFF_FALL.

Example 2

Table 3 and 4 describe an event based up-sequencing configuration and down-sequencing of three rails.

	Delay [ms] TON_DELAY	Rise [ms]TON_RISE	Power Good [V] POWER_GOOD_ON	Power Good Delay [ms] POWER_GOOD_DELAY
Vout1_2.5V	10	30	2.40 V	20
Vout2_1.2V	10	10	1.15 V	10

Table 3. Event based up-sequencing example with two output rails

	Delay [ms] TOFF_DELAY	Rise [ms] TOFF_FALL	Power Good [V] VOUT_UV_FAULT_LIMIT
Vout1_2.5V	10	30	0.85 V
Vout2_1.2V	10	10	1.05 V
Vout3_2.5V	10	20	2.30 V

Table 4. Event based down-sequencing example with three output rails

Method Three – GCB Based Sequencing

Overview

As described earlier, the GCB based and Event based sequencing of power rails are both methods of sequencing where the output of one rail provides the signal to start another rail. In the GCB based sequencing, the PMBus command SEQUENCE is used to configure the order of the products in the sequence. This method is called GCB Based Sequencing, since a GCB connection and a GCB configuration are needed in this setup.

Note: GCB based sequencing is not available in BMR450 and BMR451.

Configuration

Figure 4 illustrates the GCB Based Sequencing method, i.e. the use GCB bus to communicate power good and power down events. This provides a higher level of flexibility in that the sequence order is easily changed by modifying the products' SEQUENCE registers (see Table 5). Hence, there are no restrictions in aspect of the start-up and shut-down order. The products communicate over the GCB bus.

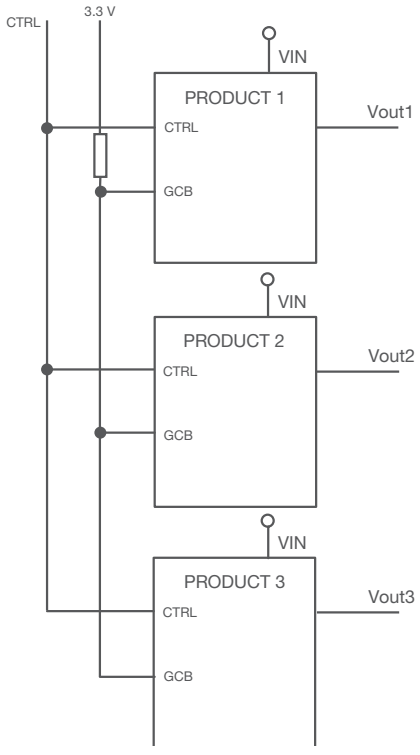


Figure 4 GCB Based Sequencing example – Enabling is generated via CTRL pin

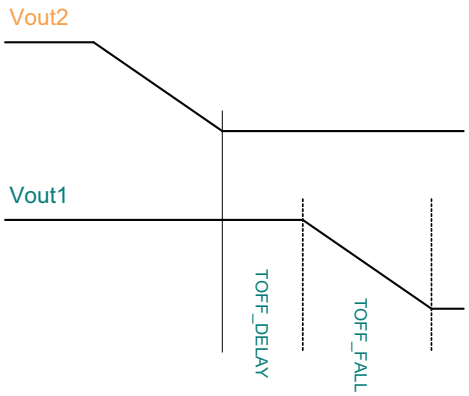


Fig 5 GCB based down-sequencing – Illustration of which settings to be made in which rail. The total time between the Preceding rail, Vout1, and the following rail, Vout2, is determined as follows: When Vout2 has reached 0 V, the start of Vout1 triggers. Vout1 are configured using TOFF_DELAY and TOFF_FALL.

The first rail in an up-sequencing group shall be disabled, i.e. set SEQUENCE[15] = 0. The other up-sequencing rails shall be set to SEQUENCE[15] = 1. The rail order is determined by the value set in SEQUENCE[12:8]. For up-sequencing, the GCB ID of the preceding rail shall be written in the following rail's SEQUENCE[12:8] register bits.

For down-sequencing the procedure is similar. The first rail in down-sequencing shall be disabled, i.e. set SEQUENCE[7] = 0. The other down-sequencing rails shall be set to SEQUENCE[7] = 1. For down-sequencing, the GCB ID of the following rail shall be written in the preceding rail's SEQUENCE[4:0] register bits.

Enabling of up- and down-sequencing can be generated via the CTRL pin or using the PMBus OPERATION command.

The products included in a GCB based sequencing group must physically be wired together on the same GCB bus. The configuration of GCB is done in the GCB_CONFIG register, see table 6.

In order to enable GCB bus communication GCB_CONFIG[5] shall be set to 0. Bits [4:0] shall be unique for all devices connected to the same GCB.

Note: The Precise Timing mode of the products must be shut off for a proper GCB-based sequence operation, i.e. MISC_CONFIG[7] shall be set to 1.

The effect of different settings in the products generating, for example Vout1 and Vout2 are illustrated in Figure 3a and 5. Note that the up-sequencing parts as described in Figure 3a are valid for both Event and GCB based sequencing

Bits	Purpose	Value	Description
15	Prequel Enable	0	Disable, no prequel preceding this rail
		1	Enable, prequel to this rail is defined by bits 12:8
14:13	Reserved	0	Reserved
12:8	Prequel Rail GCB ID	0 to 31 (0x00 to 0x1F)	Set to the Rail GCB ID of the rail that should precede this device's rail in a sequence order.
7	Sequel Enable	0	Disable, no sequel following this rail
		1	Enable, sequel to this rail is defined by bits 4:0
6:5	Reserved	0	Reserved
4:0	Sequel Rail GCB ID	0 to 31 (0x00 to 0x1F)	Set to the Rail GCB ID of the rail that should follow this device's rail in a sequence order.

Table 5. SEQUENCE command data specification for the BMR46x

Bits	Purpose	Value	Description
15:13	Reserved	0	Reserved
12:8	Broadcast Group	0 to 31	Group number used for broadcast events. (i.e. Broadcast Enable and Broadcast Margin). Set this number to the same value for all rails/devices that should respond to each other's broadcasted event. This function is enabled by the bits 15 and 14 in the MISC_CONFIG command.
7:6	Reserved	0	Reserved
5	GCB TX Inhibit	0	GCB Transmission Enabled
		1	GCB Transmission Inhibited
4:0	GCB ID	0 to 31	Sets the rail's GCB ID for sequencing and fault spreading. For the current-sharing applications, set this value the same as the ID value in ISHARE_CONFIG for all devices in the current sharing rail.

Table 6. GCB_CONFIG command data specification

Example 3

Table 7 and 8 describe a GCB-based up- and down-sequencing configuration of two rails.

	GCB_CONFIG		SEQUENCE		TON_ DELAY	TON_ RISE	POWER_ GOOD_ON	POWER_ GOOD_ DELAY	MISC_ CONFIG[7]
	GCB group Id Bit 12:8	GCB TX Inhibit Enable Bit 5	Enable up-Sequencing Bit 15	Preceding Rail Bit 12:8	Delay [ms]	Rise [ms]	Power Good [V]	Power Good Delay [ms]	Disable Precise Timing mode
Vout1 (2.5 V)	00001	0	0	0 0000 (don't care)	10	20	2.40	10	1
Vout2 (1.2 V)	00010	0	1	0 0001	10	10	1.15	10	1

Table 7. GCB-based up-sequencing example with two output rails.

	GCB_CONFIG		SEQUENCE		TOFF_ DELAY	TOFF_ FALL
	GCB group Id Bit 12:8	GCB TX Inhibit Enable Bit 5	Enable down-Sequencing Bit 7	Following Rail Bit 4:0	Delay [ms]	Fall [ms]
Vout1 (2.5 V)	0 0001	0	1	0 0010	10	20
Vout2 (1.2 V)	0 0010	0	0	0 0000 (don't care)	10	10

Table 8. GCB-based down-sequencing example with two output rails. Note: The GCB-CONFIG shall be exactly the same as for up-sequencing (see table 7).

In Figure 6a and 6b the results from configurations according to Table 7 and 8 is shown.

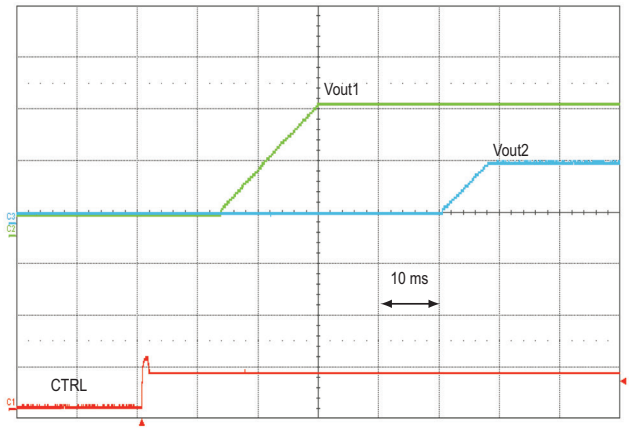


Figure 6a GCB-based sequencing example – Turn-on.

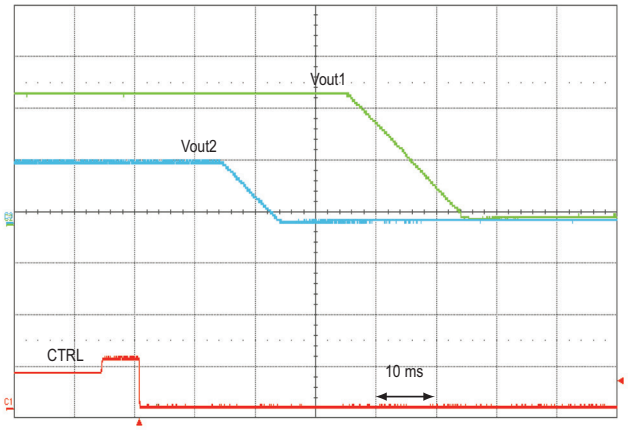


Figure 6b GCB-based sequencing example – Turn-off.

In Figure 6a, the scope is set to trigger on the CTRL event. The CTRL signal is the first to go high. The next signal to change is the turn on ramp of Vout1 since it has been configured to be the first product in the group. It occurs 10 ms = TON_DELAY after CTRL. The time of the Vout1 ramp, TON_RISE, is 20 ms. Power good for Vout1 then goes high 10 ms = POWER_GOOD_DELAY after Vout1 is above power good threshold. The power good signal is however not seen in Figure 6a. At the time of Power good for Vout1 going high, the first product communicates over the GCB bus that the next product in the group can begin its enable procedure (not shown). The delay for Vout2 to begin its turn on is set to TON_DELAY = 10 ms. The ramp time, TON_RISE, for Vout2 is 10 ms.

In Figure 6b, the scope is set to trigger on the CTRL event as well. The CTRL signal is the first to go low. The next signal to change is the Vout2 turn off ramp since it has been configured to be the first product in the group. It occurs 10 ms = TOFF_DELAY after CTRL going low. The time of the Vout1 ramp, TOFF_FALL, is 10 ms. The next signal to change is the Power Good of Vout1 which goes low after Vout1 ramp-down is completed. At the time Vout1 ramps to zero volts, the first product communicates over the GCB bus that the next product in the group can begin its disable procedure (not shown). The delay for Vout2 to begin its turn off, TOFF_DELAY, is set to 10 ms. The ramp time, TOFF_FALL, for Vout1 is 20 ms.

Comment: Instead of down-sequencing, immediate shut-down for fastest possible turn-off can be configured, with command ON_OFF_CONFIG regardless of using GCB-based up-sequencing or not.

SUMMARY OF GCB BASED SEQUENCING CONFIGURATION

General configurations:

1 If you want to start the sequence with the CTRL signal (active high), then all product's ON_OFF_CONFIG registers shall be set to 0x16. If you want to use the OPERATION command the ON_OFF_CONFIG registers shall be set to 0x1A

2 If not already done, set unique GCB IDs for all rails/products in the group using GCB_CONFIG[12:8].

3 If not already done, set GCB TX inhibit for all rails/products in the group to be enabled, i.e. set GCB_CONFIG[5] = 0

Up-sequencing configurations:

4 Disable up-sequencing for the first rail/product in the group, i.e. set SEQUENCE[15] =0

5 Enable up-sequencing for all other rails/products in the group, i.e. set SEQUENCE[15] = 1.

6 For each rail/product in the up-sequencing group, set the GCB ID of the preceding rail in SEQUENCE[12:8].

7 For up-sequencing, all rails/products in the group shall have its TON_DELAY and TON_RISE values set.

8 For up-sequencing, all rails/products in the group shall have its POWER_GOOD_ON value set.

9 For up-sequencing, all rails/products in the group may have its POWER_GOOD_DELAY value modified.

Down-sequencing configurations:

10 Disable down-sequencing for the first rail/product in the group, i.e. set SEQUENCE[7] =0

11 Enable down-sequencing for all other rails/products in the group, i.e. set SEQUENCE[7] = 1.

12 For each rail/product in the down-sequencing group, set the GCB ID of the following rail in SEQUENCE[4:0].

13 For down-sequencing, all rails/products in the group shall have its TOFF_DELAY and TOFF_FALL values set.

Method Four – Voltage Tracking

Overview

Voltage tracking allows one or more power rails to track another power rail's voltage. Products include an analog input pin, VTRK, which is used to track another voltage supply.

When a product is configured to the voltage tracking mode as shown in Figure 7, the voltage applied to the VTRK pin acts as the reference for the product's output regulation. Soft start settings are ignored and the output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin. The delay setting is only used on the turn-off end of the tracking condition. The delay setting sets the timeout for the tracking voltage to turn off in the event that the tracked voltage does not achieve zero volts. Certain tracking modes are also configurable to set the percentage of tracking and response to the power good signal.

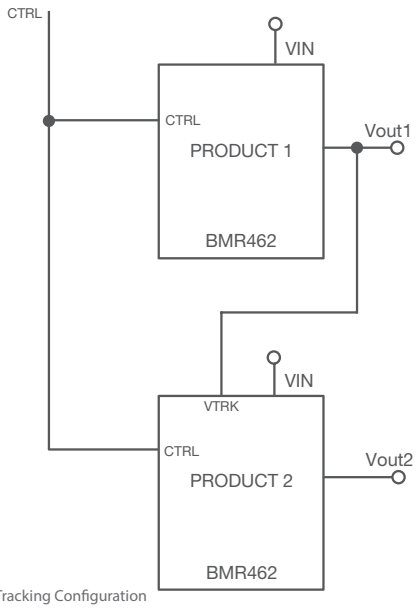


Figure 7 Voltage Tracking Configuration

In a tracking group, the product that is connected to any VTRK pin of another product is defined as the tracking master. This tracking master will control the ramp delay and ramp rate of all tracking products and is not itself placed in the tracking mode. The tracking master is configured to the highest output voltage for the group since all other product output voltages are meant to track and never exceed the tracking master output voltage. It is assumed for a tracking group, that all of the CTRL pins are connected and driven by a single logic source.

The PMBus commands for a tracking product are TRACK_CONFIG, TON_DELAY and VOUT_COMMAND.

Configuration

The TRACK_CONFIG command is used to enable the tracking mode. This command also has bit fields that set options for the tracking mode, see table 9.

Bits	Purpose	Value	Description
7	Enables Voltage Tracking	0	Tracking is disabled
		1	Tracking is enabled
6:3	Reserved	0	Reserved
2	Controls the tracking ratio	0	Output tracks 100% of VTRK
		1	Output tracks 50% of VTRK
1	Controls Upper Track Limit	0	Output is limited by target voltage
		1	Output is limited by VTRK pin
0	Controls ramp-up behavior	0	The output is not allowed to track VTRK down before power-good
		1	The output is allowed to track VTRK down before power-good

Table 9. TRACK_CONFIG command

The tracking ratio bit sets the tracking percentage to either 50% or 100%. A 50% tracking ratio is typically selected unless the target voltage of the tracking product is set to more than 50% of the target voltage of the tracking master. In that case, the 100% tracking ratio must be used. The upper track limit bit sets the output voltage limit of the tracking product. The output voltage limit can be selected to be equal to the VTRK pin, i.e. the output voltage of the tracking master multiplied by the tracking ratio, or it can be selected to be equal to the target voltage of the tracking product. The control of ramp-up behavior bit is a third possible option in the TRACK_CONFIG command. This bit sets the behavior of the output voltage during ramp-up in the case that the master voltage does not reach its target voltage and the tracking voltage does not reach the power good threshold. This option allows the tracking product to ramp-down without having to exceed the power good threshold first.

The tracking master sets the delay for the tracking group by the TON_DELAY command. In order for the tracking products to follow the complete ramps of the master, the TON_DELAY and TOFF_DELAY of the tracking products should be set according to the equations below:

$$TON\_DELAY_{Tracking} = TON\_DELAY_{Master} - 10\ ms$$

$$TOFF\_DELAY_{Tracking} = TOFF\_DELAY_{Master} + TOFF\_FALL_{Master} + 10\ ms$$

Example 4
The settings is best illustrated with an example, see Figure 8.

Rail	Is Master	Scale	Uplimit Voltage	Power Good Needed	On Delay TON_DELAY	On Rise TON_RISE	Off Delay TOFF_DELAY	Off Fall TOFF_FALL
Vout1	◉	100%	Target	☐ TRACK_CONFIG 0x80	10	20	10	20
Vout2	○	50%	Target	☑ TRACK_CONFIG 0x05	0	Don't care	40	Don't care

Figure 8 Tracking sequencing example. Vout1 is configured as tracking master, whereas Vout2 is the tracking product that tracks Vout1.

Figure 9 shows the scope set to trigger on the CTRL event. The CTRL signal is the first to go high. The next signal to change is the beginning of the Vout1 turn-on ramp since it has been configured to be the tracking master of the tracking group. It occurs 10 ms after CTRL. The time of the Vout1 ramp is 20 ms. Vout2 then begins tracking at 50% of Vout1. The ramp time for Vout2 is identical to the ramp time of Vout1.

If the power good delay time is of importance, the wanted POWER_GOOD_DELAY value shall also be configured.

Figure 10 shows the scope set to trigger on the CTRL event. The CTRL signal is the first to go low. The delay for Vout1 to begin its turn off is set to 10 ms. The ramp time for Vout1 is 20 ms. The next signal to change is the Vout2 turn off ramp since it has been configured to track 50% of Vout1.

When using products in parallel, the TON_RISE and TOFF_FALL of the tracking products must be adjusted in relation to the ramps of the tracking master. This is decribed in detail in AN307.

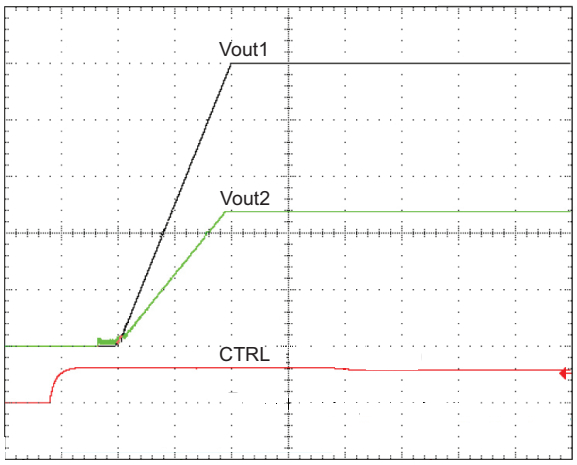


Figure 9 Tracking – Turn-on sequence example.(x-scale is 10 ms/div)

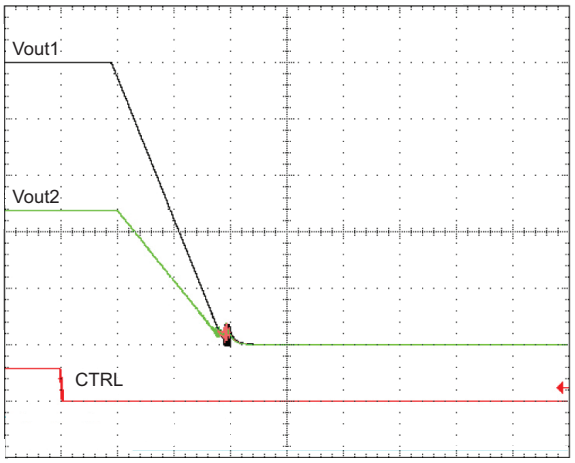


Figure 10 Tracking – Turn-on sequence example.(x-scale is 10 ms/div)

Configuration Examples

Example 1 - GCB-based Sequencing

```
#Restore factory default settings
PMBusCLI /sendbytecommand /command=RestoreDefaultAll /ADDRESS=0x4D
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4D
PMBusCLI /sendbytecommand /command=RestoreDefaultAll /ADDRESS=0x4E
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4E
PMBusCLI /sendbytecommand /command=RestoreDefaultAll /ADDRESS=0x4C
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4C

#Configure start/stop to be controlled by the CTRL pin
PMBusCLI /WRITECOMMAND /COMMAND=OnOffConfig /DATA=0x16 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=OnOffConfig /DATA=0x16 /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=OnOffConfig /DATA=0x16 /ADDRESS=0x4C

#Set the GCB ID to the Sequencing group members using GCB_CONFIG
PMBusCLI /WRITECOMMAND /COMMAND=DDCConfig /DATA=0x0000 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=DDCConfig /DATA=0x0001 /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=DDCConfig /DATA=0x0002 /ADDRESS=0x4C

#Set the up-and down-sequencing orders using SEQUENCE
PMBusCLI /WRITECOMMAND /COMMAND=Sequence /DATA=0x0081 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=Sequence /DATA=0x8082 /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=Sequence /DATA=0x8100 /ADDRESS=0x4C

#Set the up-sequencing delay times
PMBusCLI /WRITECOMMAND /COMMAND=TOnDelay /DATA=10 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=TOnDelay /DATA=20 /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=TOnDelay /DATA=10 /ADDRESS=0x4C

#Set the up-sequencing ramp-up times
PMBusCLI /WRITECOMMAND /COMMAND=TOnRise /DATA=10 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=TOnRise /DATA=10 /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=TOnRise /DATA=10 /ADDRESS=0x4C

#Set the power good on voltage levels
PMBusCLI /WRITECOMMAND /COMMAND=PowerGoodOn /DATA=< related the Vout settings> /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=PowerGoodOn /DATA=<related the Vout settings>  /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=PowerGoodOn /DATA=< elated the Vout settings>  /ADDRESS=0x4C

#Set the power good  delay times
PMBusCLI /WRITECOMMAND /COMMAND=PowerGoodDelay /DATA=10 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=PowerGoodDelay /DATA=10 /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=PowerGoodDelay /DATA=10 /ADDRESS=0x4C

#Set the down-sequencing delay times
PMBusCLI /WRITECOMMAND /COMMAND=TOffDelay /DATA=10 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=TOffDelay /DATA=20 /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=TOffDelay /DATA=10 /ADDRESS=0x4C

#Set the down-sequencing ramp-down times
PMBusCLI /WRITECOMMAND /COMMAND=TOnFall /DATA=10 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=TOnFall /DATA=10 /ADDRESS=0x4E
PMBusCLI /WRITECOMMAND /COMMAND=TOnFall /DATA=10 /ADDRESS=0x4C


# Store in User Flash and restore to RAM
PMBusCLI /sendbytecommand /command=StoreUserAll /ADDRESS=0x4D
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4D
PMBusCLI /sendbytecommand /command=StoreUserAll /ADDRESS=0x4E
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4E
PMBusCLI /sendbytecommand /command=StoreUserAll /ADDRESS=0x4C
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4C
```

Example 2 – Tracking

configuration of tracking master

```
#Restore factory default settings
PMBusCLI /sendbytecommand /command=RestoreDefaultAll /ADDRESS=0x4D
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4D

#Set output voltage to 2.5V (must be higher than Vout of the tracking product)
PMBusCLI /WRITECOMMAND /COMMAND=VOutCommand /DATA=0x5000 /ADDRESS=0x4D

#Set Ton delay and Ton Rise
PMBusCLI /WRITECOMMAND /COMMAND=TOnDelay /DATA=10 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=TOnRise /DATA=20 /ADDRESS=0x4D

#Set Toff delay
PMBusCLI /WRITECOMMAND /COMMAND=TOffDelay /DATA=10 /ADDRESS=0x4D
PMBusCLI /WRITECOMMAND /COMMAND=TOnFall /DATA=20 /ADDRESS=0x4D

# Store in User Flash and restore to RAM
PMBusCLI /sendbytecommand /command=StoreUserAll /ADDRESS=0x4D
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4D
```

configuration of tracking product

```
#Restore factory default settings
PMBusCLI /sendbytecommand /command=RestoreDefaultAll /ADDRESS=0x4E
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4E

#Set output voltage to 1.2V
PMBusCLI /WRITECOMMAND /COMMAND=VOutCommand /DATA=0x2666 /ADDRESS=0x4E

#Set Tracking mode: Enable,limit=Vtarget,50%,decrease w/o PG
PMBusCLI /WRITECOMMAND /COMMAND=TrackConfig /DATA=0x85 /ADDRESS=0x4E

#Set Toff delay = Toff delay_master + Toff fall_master + 10ms
PMBusCLI /WRITECOMMAND /COMMAND=TOffDelay /DATA=40 /ADDRESS=0x4E

#Set Ton delay = Ton_delay_master - 10 ms
PMBusCLI /WRITECOMMAND /COMMAND=TOnDelay /DATA=0 /ADDRESS=0x4E


# Store in User Flash and restore to RAM
PMBusCLI /sendbytecommand /command=StoreUserAll /ADDRESS=0x4E
PMBusCLI /sendbytecommand /command=RestoreUserAll /ADDRESS=0x4E
```

Chapter 3

Parallel operation with load sharing

GCB Bus

Flex Power Modules 3E products utilize a dedicated serial bus (the GCB bus) to synchronize and communicate real-time events. A 5 bit ID is assigned to each GCB rail, yielding a theoretical total of 32 separate power rails, including current sharing rails. Each product within a current sharing rail is assigned the same GCB ID so the total number of GCB devices can exceed 32. A maximum of 7 products or phases is allowed in a sharing group. Ensure that the GCB signal integrity is maintained when using a large product count.
During GCB events, all products will receive messages; however, only those products configured to respond will do so. GCB products can also transmit events if their programmed algorithm requires inter product communication. Some examples include fault spreading, sequencing, phase add/drop, broadcast margin and broadcast enable.

Multiple current sharing groups and power rails can communicate and connect to the same GCB bus.

Active Droop Current Sharing

Master and slave

The product with the lowest sharing group position (specified by the ISHARE_CONFIG command) is designated as the Master. The other products in the group are referred to as Slaves. The Master continuously broadcasts its inductor current over the GCB bus, while each Slave receives the message and trims its output voltage up or down until all products in the group supply the same current to the load.

Current Sharing Algorithm

A specific droop is set based on the application. The droop is set to the same value for each product in the group. Figure 1 shows an example where each product's droop, or loadline, was set to 1 mV/A. Note that the graphs and the x axis represent the individual loadline of each product, not the loadline of the group. Due to differences in layout and component variances the actual loadlines contain slope differences; they are exaggerated in this example.

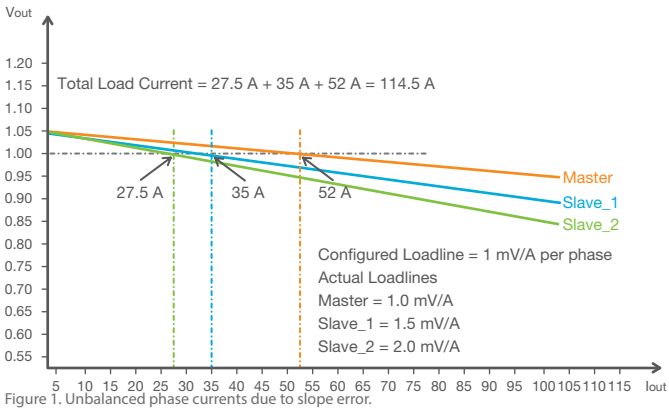


Figure 1. Unbalanced phase currents due to slope error.

The minor imbalance results in each phase contributing an unequal portion of the load current. The imbalance is detected as the Master's load current is broadcast and each Slave's reference voltage is trimmed up or down until all products in the group carry an equal portion of the load current:

$$V_{Member} = V_{OUT} + Droop_{Phase} \times (I_{Reference} - I_{Member})$$

This effect is shown in Figure 2. Notice in this case the Master initially sourced the majority of the load current. Each Slave's reference voltage was trimmed in the positive direction until all phases source equal current to the load.

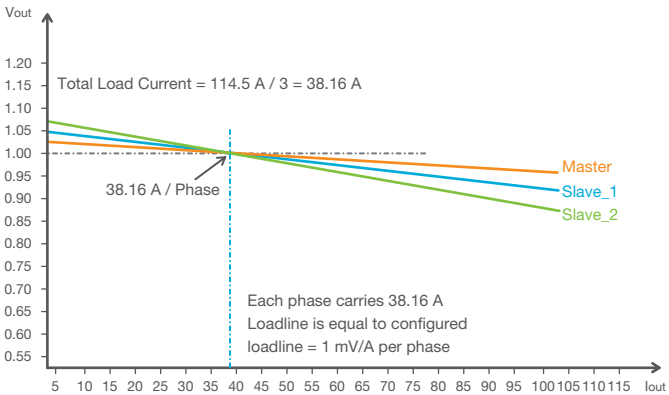


Figure 2. Balanced phase currents. Slave reference voltage(s) is trimmed until all products' currents equalize.

Current sharing equilibrium is shown in Figure 3 with a singular loadline being plotted that represents the actual static response for the sharing group. This loadline is maintained even when phases are added or dropped.

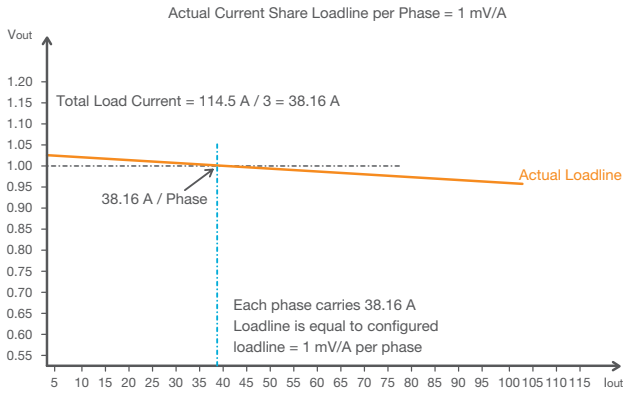


Figure 3. Current sharing phase balance is achieved.

Current Balance Accuracy

The actual current supplied by each product in a sharing group in steady state will not always be equal due to the current monitoring accuracy of each product. The current monitoring accuracy (see Technical Specification for each product) in turn will depend on the trimming of each product in production as well as varying with operating conditions such as input voltage, output voltage and temperature. The products have been designed to operate beyond rated output current in order to support 100% of rated output current from each product in a sharing group (e.g. three 40 A products in parallel support 120 A output current).

The current monitoring accuracy should be taken into account when considering the output current derating and thermal operating conditions of a current sharing group.

Phase Add/Drop

When products are configured in a current sharing group, individual products are capable of (dynamically) dropping out and adding back to the group. Phases are typically dropped or added to improve efficiency or to process a fault. Phases can be added or dropped on the fly using a separate power management host controller invoking the PHASE_CONTROL command. Even though a dropped product stops switching the operation status of the product will be Enabled and the duty cycle read (command READ_DUTY_CYCLE) will be unchanged.

Phase Drop

If the dropped phase was the group Master a new master will be reassigned based on the lowest sharing group position number of the existing operational products. However if the dropped Master was supplying the SYNC clock it will continue to do so. The group position is defined by the angular offset relative to the SYNC clock and will autonomously redistribute based on the standing phases.

Figure 4 shows an example of a functional 3-phase current sharing group prior to the dropping of the Master (Product 1). Figure 5 illustrates the new 2-phase configuration after the Master phase is dropped. Product 2 becomes the new Master for current sharing. Product 1 supplying the SYNC clock continues to do so. The timing diagram is shown in Figure 6. After the Master phase is dropped the remaining two phases are redistributed and the phase displacement changes from 120° to 180°.

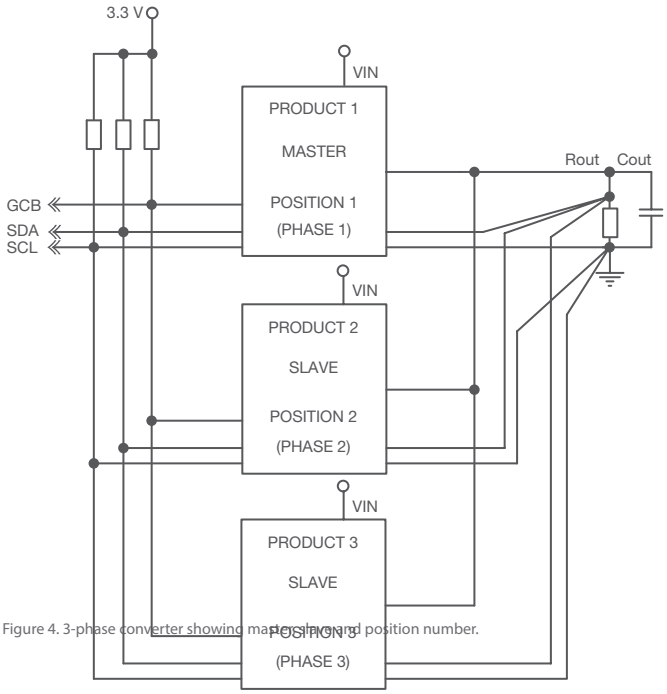


Figure 4. 3-phase converter showing master, slave and position number.

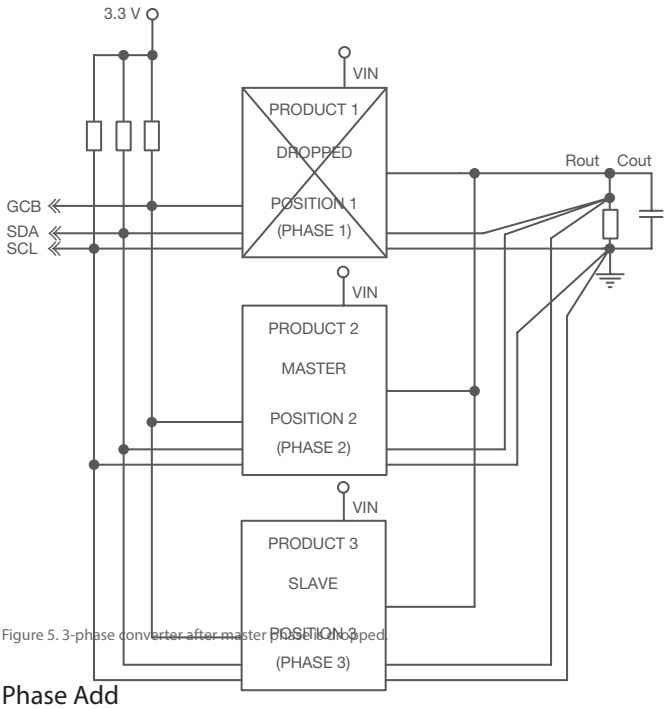


Figure 5. 3-phase converter after master phase is dropped.

Phase Add

The phase that was previously dropped may be added back into the group as determined by the power management host. When the adding is performed, the event is coordinated with the active group products over the GCB bus and the previously inactive product is added back into the group. In this example, Product 1 was made active and resumed the role of being Master, see Figure 5. The phase offset of each group product was automatically redistributed from 180° to 120° as shown in the top section of Figure 6

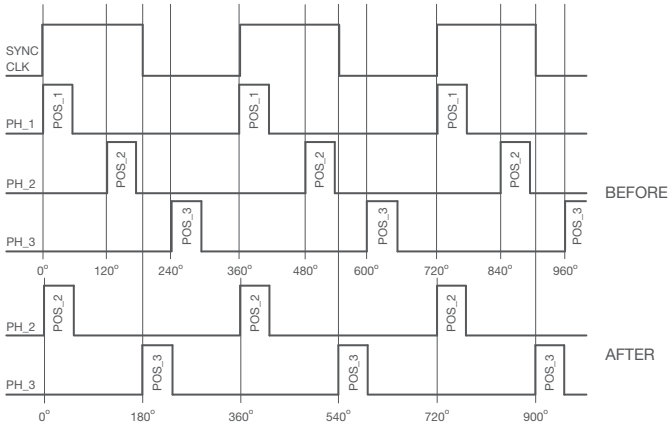


Figure 6. 3-phase converter timing diagram before and after Phase_1 (Master Phase) is dropped.

Dropped Phase and SYNC Clock

If the dropped group product was supplying the SYNC clock it will continue to do so even though it has become inactive. If the product supplying the SYNC clock dropped from the group and is no longer capable of supplying the clock, the remaining members will detect the absence of SYNC and respond according to their fault spreading configuration. If a host or power system manager is monitoring SALERT, the PMBus can be read and the products will respond with the appropriate fault management alarm as described in the PMBus Power System Mgt Protocol Specification – Part II.

Output Voltage at Phase Add/Drop

When adding or dropping a phase there will be a small deviation to the output voltage due to the droop change. Since the effective droop value for the whole group is maintained the individual droop of each phase must change. For example in a sharing group of four phases and an effective droop of 0.25 mΩ, each phase has an individual droop of 1 mΩ. When dropping one of the phases the individual droop of the still active products is maintained at 1 mΩ for a short period of time, resulting in an actual effective droop of 0.33 mΩ. Figure 7 shows the example when the output current is 100 A, giving a deviation of 8 mV. When adding a phase back to the group there will be a deviation due to the same reason but in that case the output voltage will increase instead of decrease. In any case, the deviation will always be within the voltage drop range defined by the configured total droop. Note that the output voltage is also affected by the load step that occurs for active products during a phase add or drop.

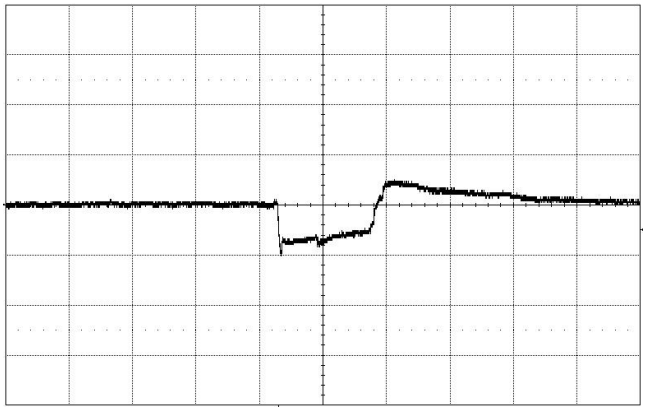


Figure 7. Example of output voltage deviation during drop (10 mV/div, 10 ms/div)

NLR Threshold Scaling

When multiple products are configured in a current sharing group, the effective output ripple is (ideally) divided by the number of active group products. This means when all products in the group are operating, the NLR (Non Linear Response) thresholds can be set to a smaller value just above the minimum ripple amplitude. When a phase is dropped the ripple amplitude will increase.

In order to avoid spurious NLR activity the products automatically adjust the NLR thresholds according to the ratio of active group products to total products of the group:

$$Threshold_{Drop} = Threshold_{Config} \times \frac{N_{All}}{N_{Active}}$$

Where
$Threshold_{Drop}$ is the NLR inner threshold setting used when some group products are dropped.

$Threshold_{Config}$ is the NLR inner threshold setting configured for the group products.
N_{All} is the total number of products in the sharing group.

N_{Active} is the number of products active in the group (products not faulted or intentionally deactivated).

N_{All} and N_{Active} are determined automatically from the group configuration parameters. No additional programming or configuration is required. Since the available thresholds are quantized to multiples of 0.5% of the configured output voltage, the next higher available threshold is used if the result of the above formula is fractional.

Automatic Phase Distribution

Products configured in current sharing groups feature the ability to autonomously perform phase offset. The offset resolution is 22.5° relative to the leading edge of the SYNC clock.

SYNC Clock
To configure a current sharing group a common SYNC clock must be provided to each product in the group. This SYNC clock can be provided internally by one of the products in the group or be provided by an external source that satisfies the electrical specifications of the SYNC pin. Note: The switching frequency of each product must be configured to the same value as the external source.

Once the SYNC source has been designated the SYNC pins of all products in the group must be connected as shown in Figure 8. Note that any of the products whose SYNC pins are physically connected can be configured to output the SYNC clock. The SYNC output can be configured as push-pull or open-drain. All other products connected to the SYNC source must be configured as SYNC inputs.

The current sharing group in Figure 8 will autonomously distribute each product's phase with respect to the SYNC clock. Since the sharing group contains 3 products, each product will be ideally offset in phase by 120°. The actual phase offset is represented by a 4 bit binary number resulting in 16 possible offset values in 22.5° steps. The real phase displacement will be rounded to the closest 22.5° increment. All possible phase displacements are shown in Figure 9. For the 3-phase example shown in Figure 8 the actual sharing group phase offset will be rounded as shown in Table 1.

Although Rail 2 is connected to the same SYNC clock it will not be autonomously offset in phase with respect to the current sharing group. Rail 2 can be offset in phase to one of the 16 possible offset values by using the INTERLEAVE command. If the INTERLEAVE command is not used, Rail 2 will simply turn on at 0° with the rising edge of the SYNC clock.

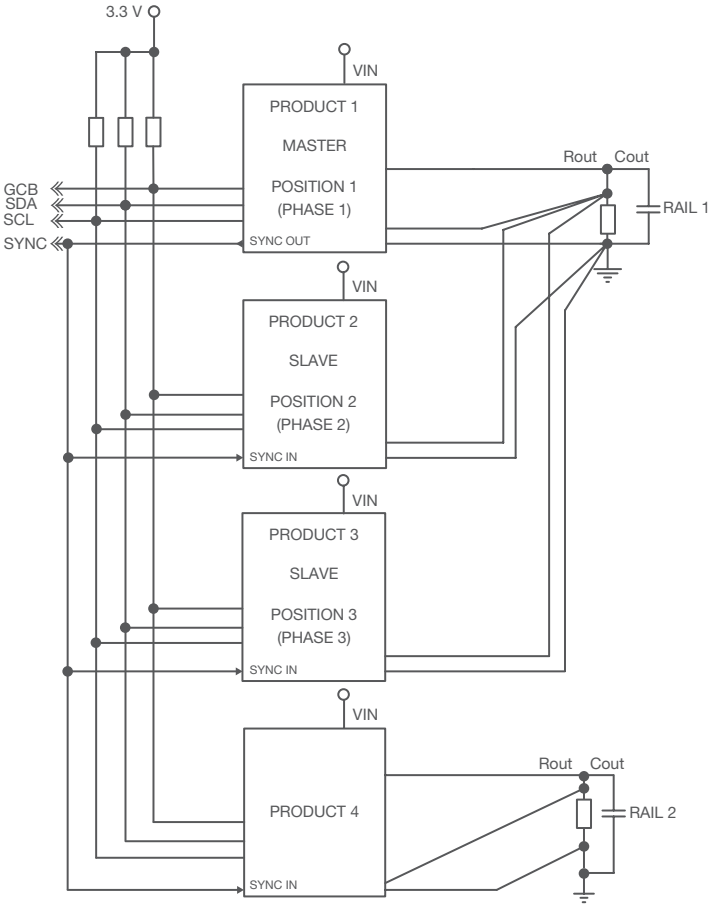


Figure 8. Example of sharing group and auxiliary output rail with a common SYNC clock.

	Ideal Offset	Actual Offset
Position_1	0º	0º
Position_2	120º	112.5º
Position_3	240º	247.5º

Table 1. Ideal vs actual phase offset.

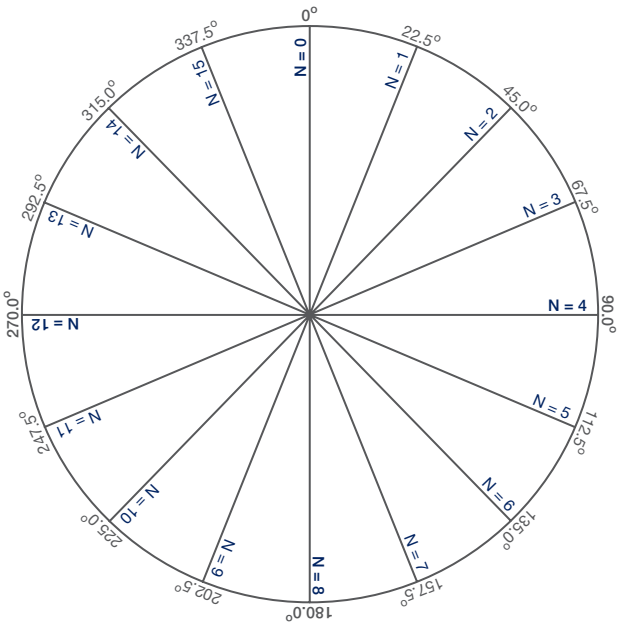


Figure 9. Phase offset resolution wheel.

INTERLEAVE Command

Current sharing groups are autonomously offset in phase with respect to each product in the group, however when there are multiple sharing groups connected to the same SYNC clock the groups will not autonomously offset from each other. Consider the two current sharing groups shown in Figure 10. This configuration consists of two output rails with each rail containing a 2-phase sharing group and a common SYNC clock. Each sharing group will autonomously phase spread within the group, but not between the two groups. The resulting timing waveform is shown in Figure 11

Notice that the positional phase equivalents in each sharing group are not offset from each other. If desired, Group 2 can be offset in phase from Group 1 by using the INTERLEAVE command. The simplest way to achieve an equal phase offset for the four devices in Figure 10 is to offset Group 2 by 90°. With the INTERLEAVE command this is done by declaring Number in Group = 4 and Interleave Order = 1. The same entries are made for both devices in Group 2. The INTERLEAVE value for Group 1 is simply 0, i.e. no phase offset. The new timing diagram shown in Figure 12 illustrates that each 2-phase sharing group is now equally offset in phase.

See application note AN309 for further information on synchronization and phase spreading.

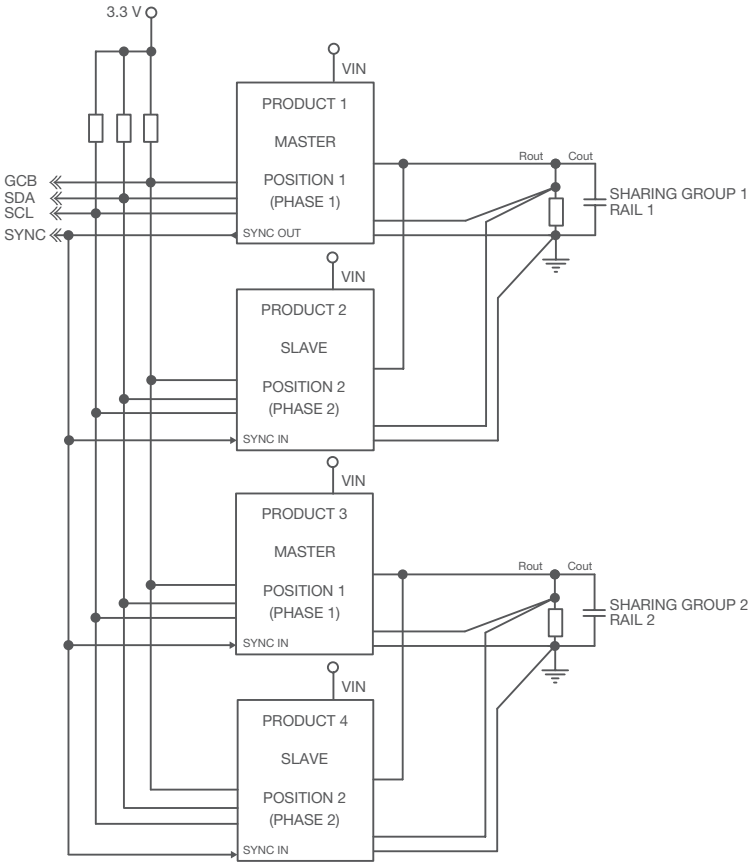


Figure 10. Example of 2 x 2-phase current sharing groups using the same SYNC clock.

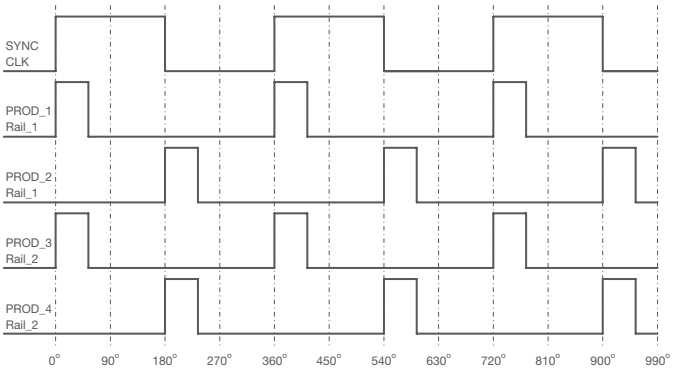


Figure 11. Timing diagram for a 2 rail x 2-phase current sharing example.

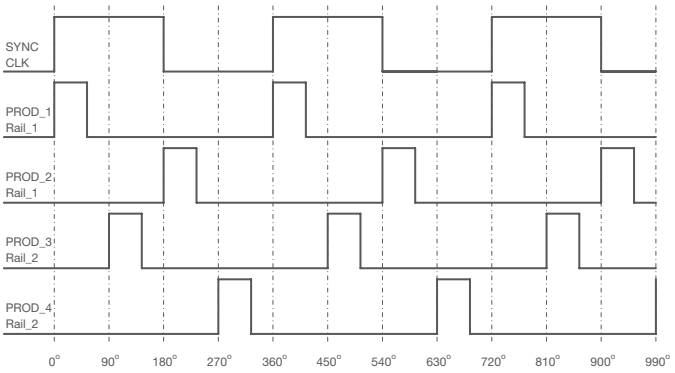


Figure 12. 2 x 2-phase current sharing groups now equally offset using the INTERLEAVE command.

Turn-On and Turn-Off

Turn-on and turn-off of a current sharing group may be controlled in two ways.

1 CTRL pin. The CTRL pin of all products in the current sharing group must be connected and be controlled from the same source.

2 PMBus enable. The products in the current sharing group must be configured for Broadcast Enable. Sending a PMBus Enable command to any of the products in the group will enable the whole group.

Ramp Synchronization

During turn-on and turn-off the voltage ramps of each phase are synchronized to start at the same time.
This ensures that inter-phase circulating currents are minimized. Each product contains a separate digital controller that executes firmware. The individual controller firmware requires synchronization prior to ramp events to minimize circulating currents. This is accomplished by forcing the Master phase to wait at least one additional firmware cycle during ramping events by configuring it to have additional TON_DELAY time and TOFF_DELAY relative to the other group Slaves.

When the sharing group receives a CTRL pin or PMBus enable, the Slaves initialize their registers and freeze the state of their firmware. Once the Master phase completes its extra timing delay it transmits a GCB Ramp Flag and all products of the group produce a sequenced PWM and begin their soft-start routine. Timing diagram shown in Figure 13.

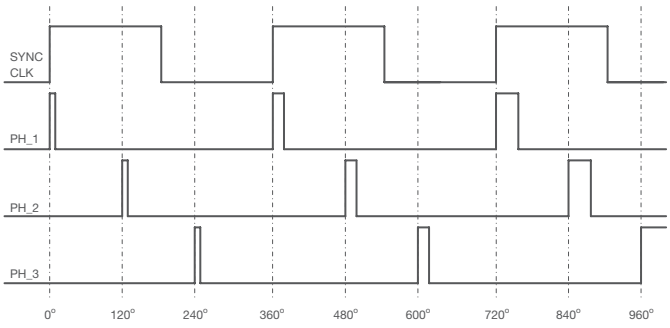


Figure 13. Start-up synchronization.

Minimum Duty Cycle

Current sharing groups can be comprised of 2 to 7 products. Each product contains its own digital PID controller. To ensure that each controller produces an identical pulse width at turn-on the products must be configured for minimum duty cycle in the USER_CONFIG register. This starts each product in the group with the same initial pulse width. The actual configured rise time is conserved as shown in Figure 14.

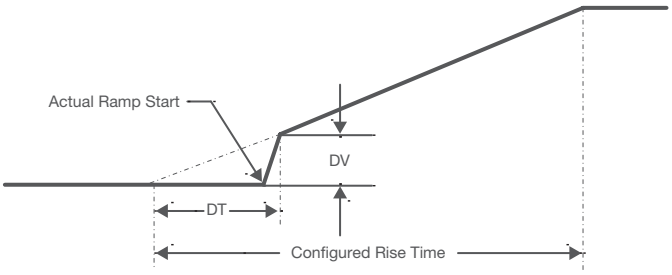


Figure 14. Turn-on rise time profile

The magnitude DV in the beginning of the ramp caused by the minimum duty cycle will increase with input voltage and switch frequency. The inrush current through the inductors may in some applications cause a small distortion in the beginning of the ramp as exemplified in Figure 15.

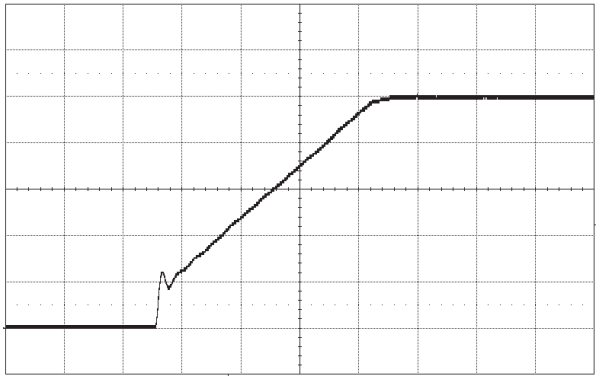


Figure 15. Effect of minimum duty cycle at ramp-up.

Ramp Behavior

The products use a unique ramping algorithm in current sharing configuration that results in near perfect current sharing while ramping. This is accomplished by deriving different compensator coefficients for ramping than those used for steady-state operation. The PID taps for ramps are not user configurable. The ramp compensation is derived from the configured rise/fall time, input voltage, output voltage and switching frequency. During ramp the loop bandwidth is intentionally set to a very low value so response to transients will be limited. The user should limit dynamic loading while ramping.

Once the ramp is completed the controllers of the products will switch to the configured compensator as defined in the used configuration. The switchover takes place at the moment when the PG (power good) signal is asserted. The user has control over the switchover by configuring the PG delay. While ramping down, the switch over takes place before the TOFF delay timer starts.

Ramp Time Accuracy

The unique ramping algorithm used in current sharing restricts the rise and fall times to a maximum value. The low bandwidth ramp technique limits the resolution of the rise and fall times. The ramp time accuracy and the maximum limit will depend on the configured switch frequency, input voltage and output voltage.

Broadcast Enable and Margining

PMBus enable and margining commands can be configured with current sharing groups just like single modules. All products must be connected to the same SMBus and GCB bus. The broadcast group can be comprised of current sharing products and single phase products. All products that should respond to the same broadcast command must be assigned the same Broadcast Group Number.

To use Broadcast Enable, send a PMBus Enable (OPERATION command) to any member of the broadcast group. The enable signal will broadcast on the GCB bus to all members of the same broadcast group as illustrated in Figure X. To use Broadcast Margining, activate margining (OPERATION command) for any member of the broadcast group. The margining signal will broadcast on the GCB bus to all members of the same broadcast group.

Note that Broadcast Enable works only when using enable via the PMBus. If using enable by the CTRL pin, the CTRL pin of each product in the group must be connected to the same enable signal.

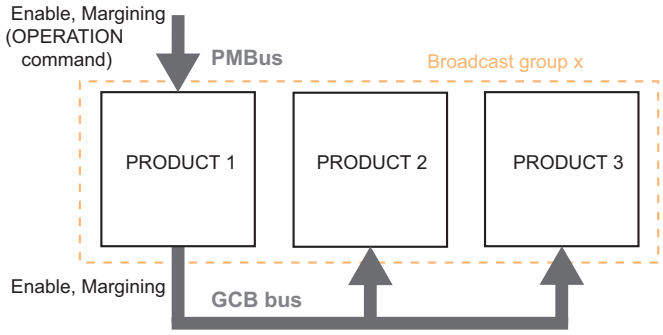


Figure 16. Enable or margining signal will broadcast on the GCB bus.

Broadcast Enable and Broadcast Margining are configured by the commands GCB_CONFIG and MISC_CONFIG according to the table below.

Function	Configuration	MISC_CONFIG	GCB_CONFIG
Broadcast Enable	Enabled	Bit 14 = 1	Bit 12:8 = Group Number 0-31
	Disabled	Bit 14 = 0	-
Broadcast Margining	Enabled	Bit 15 = 1	Bit 12:8 = Group Number 0-31
	Disabled	Bit 15 = 0	-

Table 2. Broadcast Enable and Broadcast Margining configuration.

Fault Response

If one or more products in a current sharing group fault, the remaining phases will continue to operate (the product with the next lowest position becomes the new Master). Automatically adding back faulted phases into the group, i.e. restarting of individual products in the group due to a fault, is not supported. If the products in the group have one or more fault responses configured for restart (which is the default setting for BMR46x), a synchronized restart of the whole group will occur only after all phases have shut down due to faults.

Voltage Tracking

For current sharing groups voltage tracking is emulated by configuring the output ramp to match the ramp of the VTRK voltage. The rise/fall times should be set to

$$T_{RISE/FALL} = 1.1 \times T_{RISE/FALL\_VTRK} \times \frac{V_{OUT}}{VTRK} \times \frac{1}{Tracking\_ratio}$$

Note that the formula allows configuring of any tracking ratio, simple by adjusting the rise/fall time (tracking ratio shall always be set to 100% in TRACK_CONFIG). Example: To configure a 1.2 V current sharing rail to track a 3.3 V voltage with ramp time 5 ms, by tracking ratio 75%, the ramp time of the products in the current sharing group should be set to

1.1 x 5 x 1.2 / 3.3 / 0.75 = 2.7 ms.

The ramp time can be adjusted upwards to improve the current sharing balance during the ramp, or downwards to improve the accuracy of the tracking ratio. Voltage tracking with a pre-bias voltage at the output is not recommended since there is risk of phase currents to drift apart.

Layout Considerations

As much as possible, the PWB layout and placement of output capacitances shall be made symmetrical between the products in a current sharing group, as illustrated in Figure 17. This is to minimize loadline differences, improve ripple cancelling and even up the control loop response of each phase. For the same reason VOUT connections shall be as low impedance as possible.

Each product in a current sharing group must use the same point for voltage sense. It is recommended that the traces for the voltage sense lines are routed as a differential pair in order to minimize the sensitivity to disturbances. Adding a small decoupling capacitor between the voltage sense lines close to the products is a good design practice.

Output capacitances shall be placed close to the load while input capacitances shall be placed close to the product.

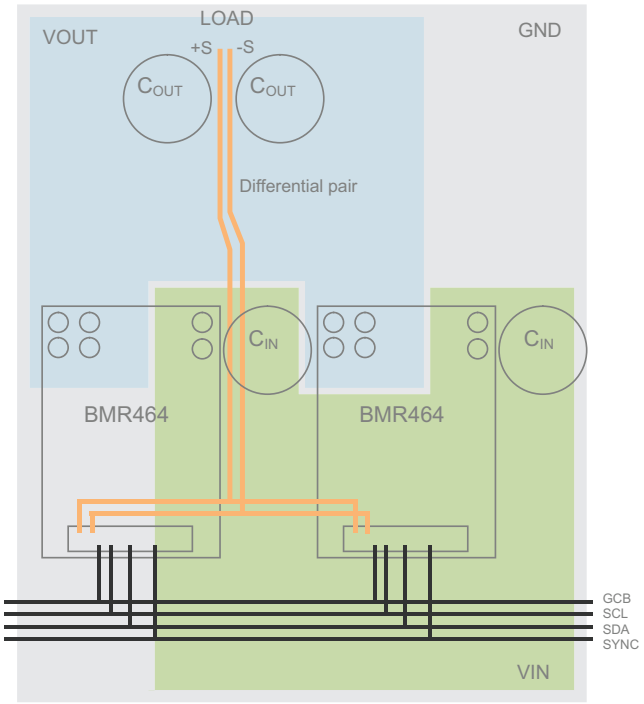


Figure 17. Layout example, two products.

Control Loop Design

Consider separate single products for the compensation analysis and divide the resulting total capacitance by the number of phases. The resultant filter consists of the phase output inductor and the equivalent phase capacitance. Consider the 3-phase example shown in Figure 18. This schematic is drawn symmetrically with identical phase filters; considering any one of the phases plus any common output capacitance divided by the number of phases. The resultant 3-phase compensation model reduces to the configuration shown in Figure 19. Refer to AN305 Control Loop Design for a detailed description on compensation.

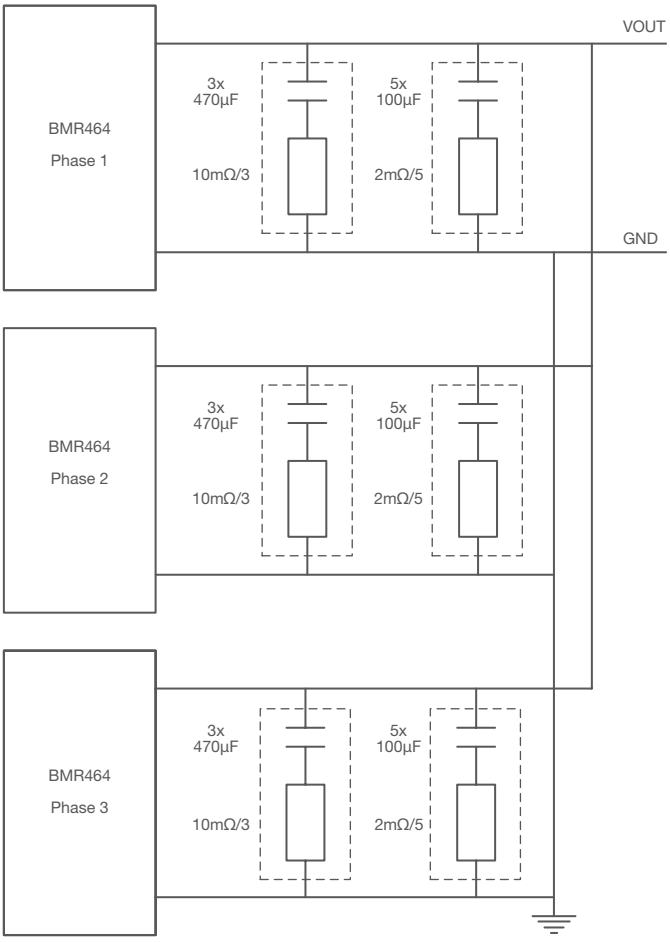


Figure 18. 3-phase current sharing example.

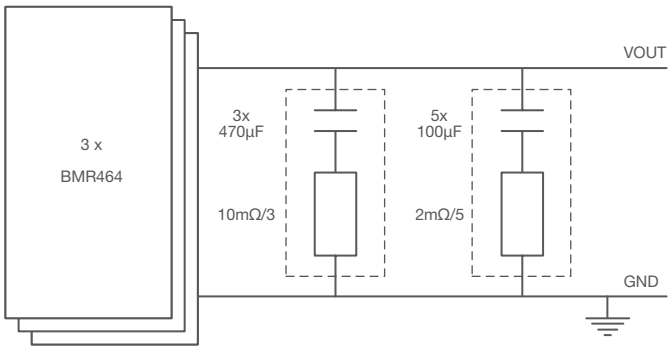


Figure 19. Current sharing compensation model..

Configuring Current Sharing

Products within a current sharing group must be of the same model. For example BMR463 can not be operated in parallel with BMR464. Each product in the group must be connected to the same GCB bus and SMBus. The product with the lowest position becomes the initial Master phase. The Master phase is used to provide the load current information to each Slave phase. If the Master phase is dropped or faults the product with the next lowest position becomes the new master.

Below sections give a detailed description of the configurations required by or related to the current sharing functionality. If making other general configurations, e.g. changing fault responses or PID taps, such configurations must be made equal for each product in the current sharing group. Refer to AN302 for a detailed specification of each command.

GCB_CONFIG

Bits	Purpose	Configuration
15:13	Reserved	These bits are not used and should be set to 0.
12:8	Broadcast Group	For a current sharing group that shall be enabled by the PMBus, the Broadcast Group value must be set the same of each product in the group. If there are other products connected to the same GCB bus, which shall be enabled separately, these products must have a unique Broadcast Group value. See section Broadcast Enable and Margining.
7:6	Reserved	These bits are not used and should be set to 0.
5	GCB TX Inhibit	Set this bit to 0 (default value) for each product in the group to enable GCB communication.
4:0	GCB ID	Sets the rail's GCB ID for sequencing and fault spreading. Assign the same rail GCB ID to each product in the current sharing group. If there are other non-current sharing products connected to the same GCB bus, make sure that those rails have a unique rail GCB ID. This ID value must be the same as the IShare GCB ID set in ISHARE_CONFIG.

Examples:
GCB_CONFIG = 0x0000 GCB_ID = 0, Broadcast Group = 0
GCB_CONFIG = 0x0407 GCB_ID = 7, Broadcast Group = 4

ISHARE_CONFIG

Bits	Purpose	Configuration
15:8	IShare GCB ID	Set to the same GCB ID as in GCB_CONFIG for each product in the current sharing group.
7:5	Number of Member	For each product in the current sharing group, set to the number of products in the group - 1. Example: 3 products in the group use 3 – 1 = 2.
4:2	Member position	Defines position of product in the group. The master with position 1 is assigned value 0 and the slaves are assigned values 1, 2, 3, …
1	Reserved	This bit is not used and should be set to 0.
0	IShare control	Set this bit to 1 for each product in the current sharing group. This enables current sharing.

Examples:
ISHARE_CONFIG = 0x0721 GCB_ID = 7, Position 1 in a group of 2 products
ISHARE_CONFIG = 0x0725 GCB_ID = 7, Position 2 in a group of 2 products

USER_CONFIG

Bits	Purpose	Configuration
15:13	Minimum Duty Cycle	The minimum allowable duty cycle must be enabled to ensure that each phase starts the turn-on ramp with the same pulse width. For each product in the group, enable a minimum duty cycle of FSW / 256, i.e. bits 15:13 = 001.
12	Alternate Ramp Down	Set according to system design requirements. Normally set to 0 for each product in the current group (default value).
11	SYNC Time-out Enable	
10	Reserved	
9	PID Feed-forward Control	
8	Fault spreading mode	If fault spreading shall be used for the current sharing rail, set this bit to 1 for each product in the current sharing group.
7	Reserved	This bit is not used and should be set to 0.
6	Sync Utilization Control	For each product in the current sharing group, except the one that possibly will be used to generate sync clock, this bit shall be set to 1 (force the SYNC pin to be input). For a product that shall be used to output sync clock this bit shall be set to 0.

5	Sync Output Control	Set to 1 for products in the current sharing group that shall be used to output sync clock from the SYNC pin. Make sure the SYNC Output Mode bit in MFR_CONFIG is set according to the system design requirements for these products. For each product in the group that uses the SYNC pin as an input the Sync Output Control bit shall be set to 0 (default).
4:3	Reserved	Set to 0 for each products in the current group (default value).
2	OFF low-side control	
1:0	Standby Mode	Monitoring must be enabled for all products in the current sharing group (bits 1:0 = 01 = default value). This ensures that the firmware is initialized prior to enabling the output voltage.

Examples:
USER_CONFIG = 0x2031 SYNC pin as clock output, fault spreading disabled
USER_CONFIG = 0x2051 SYNC pin as clock input, fault spreading disabled
USER_CONFIG = 0x2151 SYNC pin as clock input, fault spreading enabled

MFR_CONFIG

Bits	Purpose	Configuration
15:11	Current Sense Blanking Delay	This delay parameter controls the blanking time (ns) after switching the top or bottom FET, preventing switch noise from disturbing the current measurement circuit. Normally the default value used for each product will be enough but in some applications an increased value might be needed.
10:8	Current Sense Fault Count	Set according to system design requirements. Normally the default values shall be used for each product in the current sharing group.
7:6	Reserved	
5:4	Current Sense Control	
3	NLR During Ramp	Shall be set to 0 (default) for each product in the current group.
2	Alternate Ramp Control	Shall be set to 1 (alternate ramp enabled) for each product in the current sharing group.
1	Reserved	This bit is not used and should be set to 0.
0	SYNC Pin Output Control	Set according to system requirements (open drain or push-pull output) for products in the group that is configured to output sync clock. For products using the SYNC pin as input this bit can be set to either 0 or 1.

Examples:
MFR_CONFIG = 0x8F14 SYNC pin output as open-drain
MFR_CONFIG = 0x8F15 SYNC pin output as push-pull

If the Current Sense Blanking Delay is increased the read READ_IOUT value will be affected by a small offset. To compensate for this the existing IOUT_CAL_OFFSET value can be changed according to the approximate formula below (it is assumed that bits 5:4 Current Sense Control is unchanged = down slope sense).

$$IOUT\_CAL\_OFFSET_{NEW} = IOUT\_CAL\_OFFSET_{OLD} - \frac{V_{OUT} \times (BlankDelay_{NEW} - BlankDelay_{OLD})}{2 \times L}$$

Where *L* = Output inductor value of the product (model dependent).

MISC_CONFIG

Bits	Purpose	Configuration
15	Broadcast Margin	If broadcast margining or enable shall be used (see GCB_CONFIG) for the current sharing group these bits must be set accordingly. The same setting must be used for each product in the group. Note that Broadcast Enable can be used only when PMBus on/off control is used. If using on/off control by the CTRL pin, the CTRL pin of each product in the group must be connected to the enable signal.
14	Broadcast Enable	
13	Adaptive Compensation	Use default values for each product in the current sharing group.
12	Reserved	
11:10	Current Sense Gain Factor	
9:8	Reserved	
7	Precise Ramp-Up Delay	Shall be set to 1 (=Precise Ramp-up Delay disabled) for each product in the current sharing group.
6	Diode Emulation	Set according to system design requirements. Normally the default values shall be used for each product in the current sharing group. Diode Emulation and Adaptive Frequency is not supported with current sharing and shall be disabled.
5:3	Reserved	
2	Minimum GL Pulse	
1	Snapshot	
0	Adaptive Frequency	

Examples:
MISC_CONFIG = 0x2082 No broadcast functions
MISC_CONFIG = 0x6082 Broadcast Enable activated
MISC_CONFIG = 0xA082 Broadcast Margining activated

VOUT_COMMAND

Each current sharing phase must be set to the same output voltage. Since the droop/current sharing algorithm will need headroom to adjust the output voltage, it is recommended to keep VOUT_COMMAND below 0.96 x VOUT_MAX.

The user might want to increase the nominal output voltage by an offset in order to compensate for the load-line droop. Typically an offset magnitude of $0.5 \times I_{MAX} \times R_{DROOP}$ would be used.

VOUT_TRIM

Writing this command will have no effect for products in a current sharing group since the command is used by the current sharing algorithm. The Master phase will always retain a zero VOUT_TRIM value, while each Slave phase will adjust its VOUT_TRIM value until all phases carry equal load current

VOUT_CAL_OFFSET

The VOUT_CAL_OFFSET parameter contains a calibration value from production and should not be changed. If an offset voltage is desired to overcome the effects of droop, the value of VOUT_COMMAND should be adjusted.

VOUT_DROOP

Droop resistance is used as part of the current sharing algorithm. Each product in the group shall be assigned the same VOUT_DROOP value, which will be the effective droop (or loadline) of the whole group. Since the total current is shared between the products in the group, the droop of each individual phase will be set higher than the configured VOUT_DROOP value.

Example for a current sharing group with four products:

VOUT_DROOP value assigned to all four products	0.25 mV/A
Effective droop or loadline of the group output	0.25 mV/A
Effective droop or loadline for each individual phase with all phases active	0.25 x 4 = 1.0 mV/A

The assigned effective droop is maintained even when phases are added or dropped which means the individual droop of each phase is automatically adjusted.

It is recommended to assign a VOUT_DROOP value that gives an *individual* droop between 0.5 and 1.5 mV/A per phase. In general current sharing balance is improved with higher droop. A too high droop may cause instability at high loads. The highest possible droop for stable operation decreases as temperature and output load increases. The graphs in Figure 20 and Figure 21 show the recommended maximum individual droop per phase vs output voltage and maximum output current, assuming operation at a maximum temperature of +95ºC.

In order not to affect the configured over current protection (OCP) threshold; the maximum output current used when defining maximum droop should be equal to the configured OCP threshold.

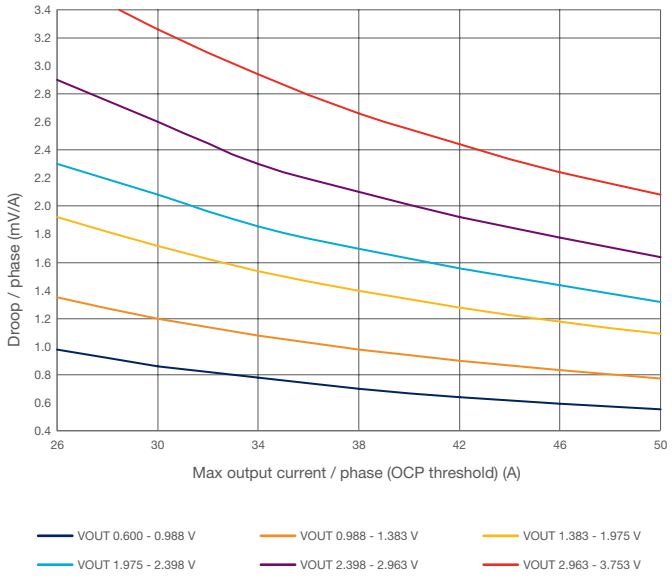


Figure 20. Recommended maximum individual droop per phase vs VOUT and max IOUT for BMR464.

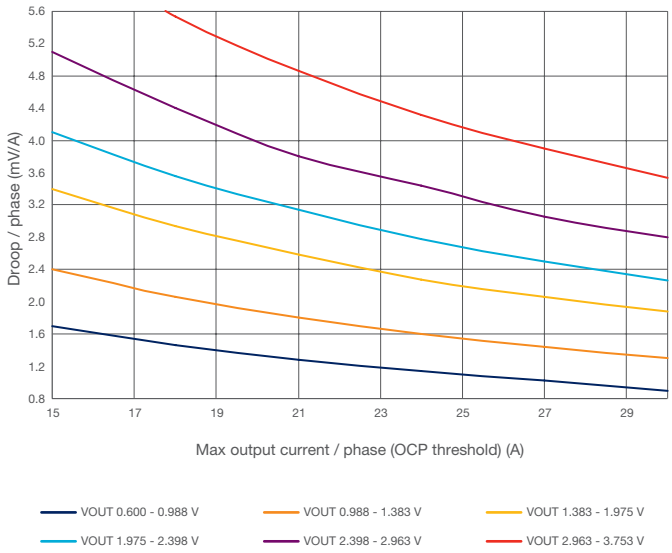


Figure 21. Recommended maximum individual droop per phase vs VOUT and max IOUT for BMR463.

TON_DELAY

For each Slave phase the TON_DELAY parameter shall be set equal and to 5 ms or higher. For the Master phase TON_DELAY shall be set at least 10 ms greater than the TON_DELAY value used for each Slave phase. The resulting delay times used for the common output will be the one set for the Master phase.

TOFF_DELAY

Same configurations rules as for TON_DELAY.

TON_RISE, TON_FALL

The TON_RISE and TON_FALL values must be equal for each phase in the group. For a current sharing group there is an upper limit to the ramp time that can be used. The limit will depend on the used switch frequency, input voltage and output voltage. Figure 22 shows the approximate maximum ramp time when considering the whole input voltage range 4.5-14 V. It is recommended to use ramp times in the range 5 to 10 ms.

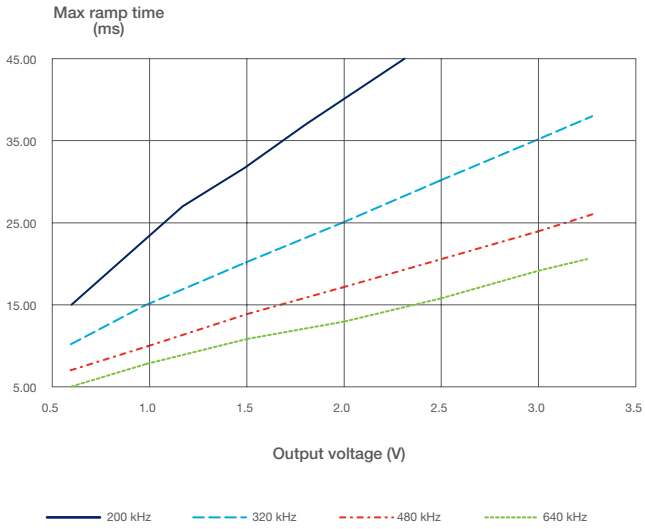


Figure 22. Max ramp time vs output voltage and switch frequency

FREQUENCY_SWITCH

If the current sharing group uses an external clock, the FREQUENCY_SWITCH value shall be set to the frequency value of the external clock. The FREQUENCY_SWITCH value shall be equal for each product in a current sharing group.

ON_OFF_CONFIG

The configuration of ON_OFF_CONFIG must be equal for each product in a current sharing group. Ramping down the output at turn-off is mandatory which means bit 0 in ON_OFF_CONFIG must be set to 0. Note that if enabling by the PMBus is used, Broadcast Enable must be activated in MISC_CONFIG and GCB_CONFIG

Examples:
ON_OFF_CONFIG = 0x16 Enable by CTRL pin, active high polarity
ON_OFF_CONFIG = 0x14 Enable by CTRL pin, active low polarity
ON_OFF_CONFIG = 0x1A Enable by PMBus command OPERATION

OVUV_CONFIG

For products in a current sharing group the crowbar function must be turned off, i.e. bit 7 in OVUV_CONFIG must be cleared.

Example:
OVUV_CONFIG = 0x0F

POWER_GOOD_DELAY

In order for the switching of compensator coefficients (see Ramp Behavior) to not occur before ramp-up has finished, the POWER_GOOD_DELAY value should fulfill the equation below.

The POWER_GOOD_DELAY value shall be equal for each product in the group.

$$POWER\_GOOD\_DELAY > 1.3 \times TON\_RISE \times \frac{(VOUT\_COMMAND - POWER\_GOOD\_ON)}{VOUT\_COMMAND}$$

Configuration Checklist

Use the following checklist as a guideline when creating configuration files for current sharing rails.

1 Perform a RESTORE_DEFAULT_ALL command in order to load default configuration of product.

2 Enable ramp-down at turn-off for all products in the group (clear bit 0 in ON_OFF_CONFIG).

3 Disable the crowbar function used at OV fault (OVUV_CONFIG).

4 Enable Alternate Ramp Control for all products in the group (MFR_CONFIG).

5 Enable a Minimum Duty Cycle of FSW / 256 for all products in the group (USER_CONFIG).

6 Designate and configure SYNC source for the group. Products not sourcing SYNC must be configured as SYNC inputs (all products in the group must used the same SYNC signal) (MFR_CONFIG, USER_CONFIG).

7 Disable Precise Ramp Up Delay for all products in the group (MISC_CONFIG).

8 Assign the same VOUT_DROOP value to all products in the group.

9 Assign the same GCB_ID to all products in the group (GCB_CONFIG).

10 Assign the same IShare GCB ID =GCB ID and enable Current Share Control for all products in the group (ISHARE_CONFIG).

11 Assign a unique phase position for each product in the group (ISHARE_CONFIG).

12 Ensure that the TON_DELAY and TOFF_DELAY times for the Master are at least 10 ms greater than the corresponding delay parameters of each Slave. Delay parameters must be greater than 5 ms.

13 If using PMBus enable/disable of group, configure PMBus enable (ON_OFF_CONFIG), activate broadcast enable (MISC_CONFIG) and configure broadcast group (GCB_CONFIG).

14 If changing the default configuration, ensure that all products in the group are assigned the same

15
a. TON_RISE and TOFF_FALL times.
b. power good threshold and delay time.
c. fault thresholds and fault responses.
d. INTERLEAVE settings.
e. PID taps and NLR settings.
f. current sense blanking delay.
g. switch frequency.

Formed in the late seventies, Flex Power Modules is a division of Flex that primarily designs and manufactures isolated DC/DC converters and non-isolated voltage products such as point-of-load units ranging in output power from 1 W to 700 W. The products are aimed at (but not limited to) the new generation of ICT (information and communication technology) equipment where systems' architects are designing boards for optimized control and reduced power consumption.

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