



Non-Volatile Memory Reliability in 3E Products

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Introduction

Digitally controlled and managed power supplies represent a rapidly growing part of the power conversion industry. It is an exciting and dynamic part of the market because of the many advantages it offers relative to conventional analog-based control methodologies. Hardware and system impacts of digital power are being addressed in the many conference papers and trade journal articles that have recently been appearing. But this highly configurable new approach to power supplies has other impacts both to suppliers of power hardware and to their OEM customers. One of these impacts is the Quality Assurance process, which faces new challenges with the introduction of digital power supplies.

This paper will describe endurance and data retention figures for the Non-Volatile Memories (NVM) used in Ericsson Digital Power products.

This Technical Paper applies to:

BMR 450-451

BMR 453-458

BMR 461

BMR 462-467

PIM 4000 Series products

NVM Endurance

The Non-Volatile Memory (NVM) endurance is a measure of a product's NVM ability to retain data after repeated program/erase (P/E) cycles. For all Ericsson products, NVM endurance verification and approval are made according to standard procedures.

NVM test vehicles have been used to check the ability of the NVM to retain data after repeated program/erase (P/E) cycles at various temperatures. This is further described below.

BMR 450-451, BMR 462-467

Three qualification lots have been tested where the NVMs were cycled for 20K P/E cycles at -40°C, 0°C, 25°C, 125°C with no NVM related failures.

BMR 453-458, BMR 461

One qualification lot has been tested where the NVMs were cycled for 20K P/E cycles at 125°C with no NVM related failures.

PIM 4000 Series

The PIM 4000 Series products have been qualified for minimum 10K P/E cycles.

NVM Data Retention

The Non-Volatile Memory (NVM) data retention (DR) is a measure of how long time a product's NVM will keep or "remember" the data. This time is adversely affected by the product's PWM controller (junction) temperature.

NVM test vehicles have been used to check the ability of the NVM to retain data after prolonged storage at high temperature as described below.

BMR 450-451, BMR 462-467

The test devices were pre-cycled for 20k P/E cycles at 25°C and then baked at 150°C for 5000 hours.

Based on the test vehicle and the Arrhenius equation (see below) the estimated NVM data retention times for BMR 450-451 and 462-467 in Table 1 have been calculated.

Ea [eV] Activation Energy	Temperature [°C]	AF [Years] Acceleration Factor	DR [Years] Lite time
0.8	25	9 970	5 691
0.8	85	53.8	30.7
0.8	100	19.0	10.8
0.8	125	4.0	2.3
0.8	150	1	0.57

Table 1. NVM data retention (DR) times for BMR 450-451 and 462-467.

From Table 1, it can be seen that the NVM data retention time of, for example, a BMR 465 is estimated to be about 0.57 year (i.e. 5000 hours) at 150°C, and 2.3 years at 125°C.

BMR 453-458, BMR 461

In Table 2, the estimated NVM data retention times in BMR 461 and 453-458 are presented. One wafers lot were pre-cycled for 20k P/E cycles at 25°C and then baked at 150°C for 1000 hours.

It can be seen that the NVM data retention time, of for example, a BMR 456 is estimated to be about 0.11 year (i.e. 1000 hours) at 150°C, and 0.45 years at 125°C.

Ea [eV] Activation Energy	Temperature [°C]	AF [Years] Acceleration Factor	DR [Years] Lite time
0.8	25	9 970	1 138
0.8	85	53.8	6.1
0.8	100	19.0	2.2
0.8	125	4.0	0.45
0.8	150	1	0.11

Table 2. NVM data retention (DR) times for BMR 461 and 453-458.

PIM 4000 Series

In Table 3, the estimated NVM data retention times of PIM 4000 Series products are presented.

The NVM test vehicle was tested at 170°C for 420 hours. Based on the test vehicle and the Arrhenius equation (see below) Table 3 was created.

It can be seen that the NVM data retention time, of for example, a PIM 4328 PD is estimated to be about 0.13 year at 150°C, and 0.51 years at 125°C.

Ea [eV] Activation Energy	Temperature [°C]	AF [Years] Acceleration Factor	DR [Years] Lite time
0.8	25	26 860	1 287
0.8	50	2 408	115
0.8	85	145	6.9
0.8	125	10.7	0.51
0.8	150	2.7	0.13
0.8	170	1	0.05

Table 3. Non-Volatile Memory (NVM) data retention (DR) times for PIM 4000 Series products.

Arrhenius equation - Acceleration factor calculations

The Arrhenius equation can be used to estimate the data retention time of floating gate NVM technologies. It is used to find the acceleration factor between a stress

temperature and a use condition, which in turn can be used to derate results from NVM data retention test.

The acceleration factor, AF, between any two temperatures, T_1 and T_2 , may be calculated as in Equation (1):

In Table 4, the variable definitions used in the Arrhenius equation is described.

Note: The activation energy, E_a , used for test 0.8 eV is a

$$AF = AF(T_1 - T_2) = e^{\frac{E_a}{k}(\frac{1}{T_1} - \frac{1}{T_2})} \quad (1)$$

conservative estimate based on Industry standard data for Non-Volatile Memory failure mechanism.

AF calculations for six T_1/T_2 examples are found in Table 4 as well. In the calculation examples, it is assumed that the NVM qualification test was made at 150°C. Therefore, 150°C is regarded as the qualification temperature, T_1 , and therefore $AF = 1$ for 150°C.

Application Examples

Example 1 - 10 years NVM DR time for BMR 463
10 years NVM DR time is requested for a BMR 463.

From Table 1, it can be found that the NVM DR time is 10.8 years at 100°C. But if you really would like to estimate which temperature that allows exactly 10 years, then a reformulation of the Arrhenius equation, Equation (1), can be used, see Equation (2).

First determine the AF parameter for BMR 463.
 $AF = 10/0.57 = 17.52$ since the qualification was made for 5 000 hours = 0.57 years, which can be read from Table 1, and since 10 years is the requested NVM data retention time.

Secondly, we conclude that T_2 is $150 + 273 \text{ K} = 423 \text{ K}$ since the qualification was made at 150°C. From Table 1, it is understood that the qualification temperature is 150°C due to the fact that AF is equal to one for this temperature.

Now, by using Equation (2), T_1 can be calculated to be 101°C (374 K) as shown below:

$$T_1 = \frac{T_2}{1 + T_2 \frac{k}{E_a} \ln(AF(T_1 - T_2))} \quad (2)$$

$$T_1 = \frac{423}{1 + 423 \cdot \frac{8.616 \cdot 10^{-5}}{0.8} \cdot \ln(17.52)} \text{ K} \approx 374 \text{ K} = 101^\circ\text{C} \quad (3)$$

Example 2 - PIM 4328 PD DR time estimation

In an application operating at 50°C, 24 hours per day, 7 days per week, the NVM DR time in a PIM4328 PD is 115 years. This could be read from Table 3 directly.

Assuming the application is actually running 5 hours per day at 50°C and the rest of the day at 25°C, the NVM DR time can be re-calculated as follows:

5 hours/day at 50°C: The equivalent data aging at 25°C is 5 hours $\times AF(25^\circ\text{C})/AF(50^\circ\text{C}) =$
5 hours $\times 26\,860/2\,408 = 5 \text{ hours} \times 11.1 = 55.5 \text{ hours}.$

19 hours/day at 25°C: The equivalent data aging at 25°C is of course still 19 hours.

Total data aging per day is then 55.5 + 19 hours = 74.5 hours, which corresponds to 3.1 days at 25°C.

In this scenario, DR time is $12\,87/3.1 \text{ years} = 414 \text{ years}.$

Variable	Definition	Ex 1	Ex 2	Ex 3	Ex 4	Ex 5	Ex 6
e	Natural log	~2.718					
E_a	Activation energy	0.8 eV					
k	Boltzman's constant	$8.616 \times 10^{-5} \text{ eV}/^\circ\text{K}$					
T_1	Derated temperature	25°C (298 K)	50°C (323 K)	85°C (350 K)	100°C (373 K)	125°C (398 K)	150°C (423 K)
T_2	Stress temperature	150°C (423 K)	150°C (423 K)	150°C (423 K)	150°C (423 K)	150°C (423 K)	150°C (423 K)
AF	Calculated AF	9 970	53.8	53.8	19.0	4.0	1.0

Table 4. Calculations of Acceleration Factor, AF, using Arrhenius equation for some temperature differences.

Formed in the late seventies, Flex Power Modules is a division of Flex that primarily designs and manufactures isolated DC/DC converters and non-isolated voltage products such as point-of-load units ranging in output power from 1 W to 860 W. The products are aimed at (but not limited to) the new generation of ICT (information and communication technology) equipment where systems' architects are designing boards for optimized control and reduced power consumption.

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