Vertical SIP

Horizontal SMD

BMR473

40A digital PoL regulator

The BMR473 is a digital PoL regulator available in a horizontal surface mount or vertical SIP package for board space optimization.

The product is rated at 40A continuous and up to 4 modules can be paralleled for up to 160A output current.

The BMR473 is a single-phase converter with high power density and efficiency levels are up to 96.2% at full load.

Input is rated from 6 to 15V and the output is programmable from 0.6 to 5V.

The BMR473 is designed for telecom and datacom applications but can also be applied in other areas such as industrial and transportation.

Key features

- High efficiency up to 96.2% at 12 Vin, 5 Vout full load.
- Paralleling up to 4 units (160A)
- Remote control
- Power Good
- Synchronization and phase spreading
- Excellent thermal performance
- Configuration and monitoring via PMBus

Soldering methods

- Wave soldering (SIP)
- Reflow (SIP and SMD)

Key electrical information

Parameter	Values
Input voltage range	6 - 15 V
Output voltage range	0.6 - 5 V
Max output current	40 A

Mechanical

26.3 x 8.8 x 15.6 mm / 1.035 x 0.346 x 0.614 in (Vertical SIP)

19.0 x 13.0 x 7.5 mm / 0.748 x 0.512 x 0.296 in (Horizontal SMD)

Application areas

- Telecom
- Datacom

Product options

The table below describes the different product options.

For more information, please refer to Part 2 Mechanical information.

Example:	BMR473	2	0	01	/001	B	Definitions
Product family	BMR473						
Mounting options		2					1 = Surface mount 2 = Single in line package (SIP)
Pin length options			0				0 = standard (4.57 mm, SIP) 1 = short pin option (3.69 mm, SIP) 2 = long pin option (5.33 mm) 0 = solder bump (SMD)
Other hardware variants				01			01 = standard
Configuration code					/001		/001 = standard config. (positive remote control)
Packaging options						B	B = tray (one full package with 240 pieces) C = Tape and reel (one full package with 200 pieces)

If you do not find the variant you are looking for, please contact us at Flex Power Modules .

Order number examples

Part number	V_{in}	outputs	configuration
BMR4732001/001	6 –15 V	0.6 – 5 V, 40 A/100W	SIP 4.57 mm pins / positive logic / dry pack, tray
BMR4731001/001	6 –15 V	0.6 – 5 V, 40 A/100W	SMD soder bump/ positive logic / dry pack, tape & reel

Part 1: Electrical specifications

Absolute maximum ratings

Stress in excess of our defined *absolute maximum ratings* may cause permanent damage to the converter. Absolute maximum ratings, also referred to as *non-destructive limits,* are normally tested with one parameter at a time exceeding the limits in the electrical specification.

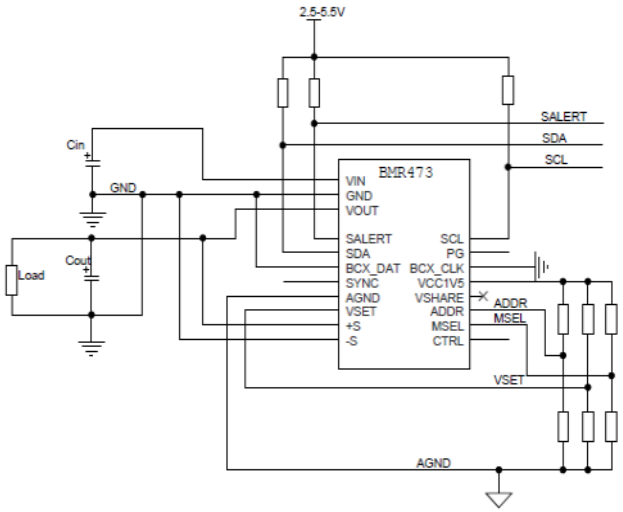
Characteristics		min	typ	max	Unit
Operating temperature (T_{P1})		-40		125	°C
Storage temperature		-40		125	°C
Input voltage (V_{in})		-0.3		16	V
Signal I/O voltage	SCL, SDA, SALERT, SYNC, BCX_DAT, BCX_CLK, CTRL, PG	-0.3		5.5	V
Ground voltage differential	-S, AGND, GND	-0.3		0.3	V
Analog pin voltage	V_{out}, +S	-0.3		5.5	V
	ADDR, VSET, MSEL	-0.3		1.65	V

Reliability

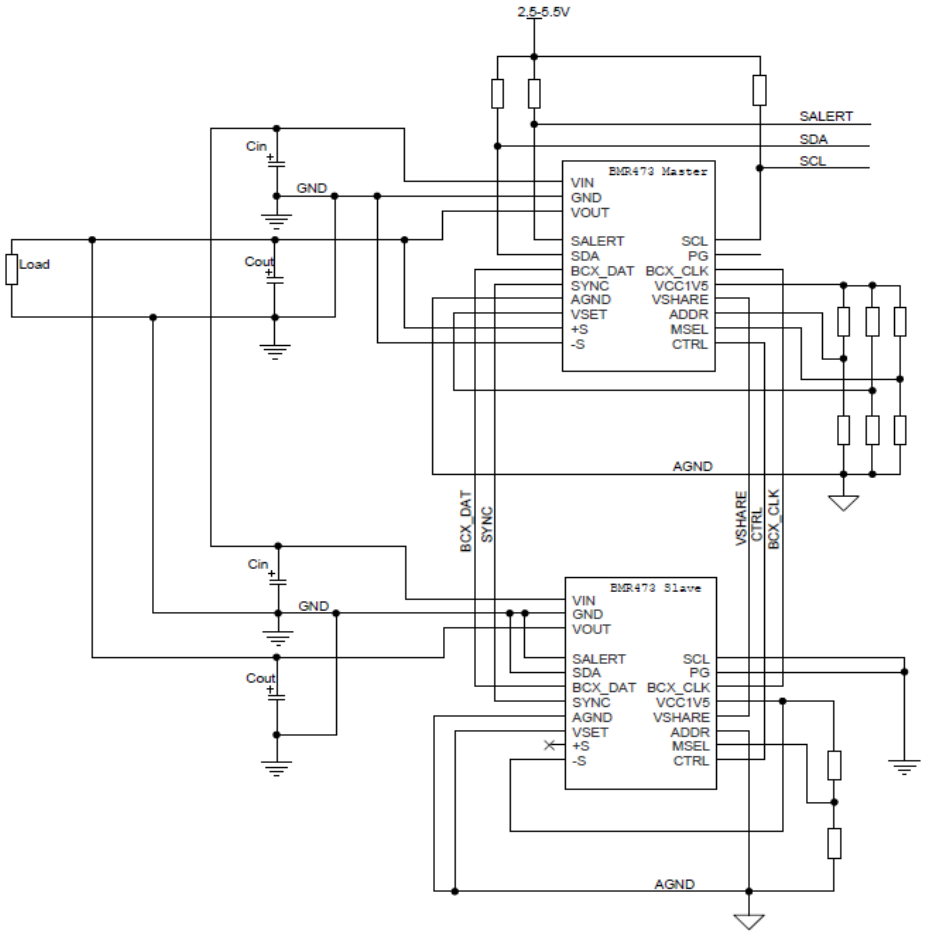
Failure rate (λ) and mean time (50%) between failures (MTBF= 1/ λ) are calculated based on *Telcordia SR-332 Issue 4: Method 1, Case 3, (80% of I_{out}, T_{P1}=40°C, Airflow=200 LFM).*

	Mean	90% confidence level	Unit
Steady-state failure rate (λ)	26	32	nfailures/h
Standard deviation (σ)	4.9		nfailures/h
MTBF	38.39	30.97	MHr

Typical application diagram (Stand Alone)



Typical application diagram (2 modules paralleling)



Electrical specifications for BMR4732001 (Vertical SIP)

Min and Max values are valid for: T_{P1} = -40 to + 85°C, V_{in}= 6 to 15 V, unless otherwise specified under conditions. Typical values given at: T_{P1} = +25°C, V_{in}= 12 V, max I_{out}, unless otherwise specified under conditions.

Additional external C_{in} = 5 x 22 µF ceramic + 470 µF OSCON (ESR 14 mΩ), C_{out}= 5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ).

Characteristic	descriptions	conditions	min	typical	max	unit
Input characteristics						
Input voltage range (V_{in})		0.6 V≤V_{out}≤ 3.3 V	6	12	15	V
		3.3 V<V_{out}≤ 5.0 V	7	12	15	V
Input idling power	I_{out} = 0 A	V_{out} = 0.6 V		0.7		W
		V_{out} = 1.0 V		0.7		W
		V_{out} = 1.8 V		1.0		W
		V_{out} = 2.5 V		1.4		W
		V_{out} = 3.3 V		1.7		W
		V_{out} = 5.0 V		2.5		W
Input standby power	Turned off with CTRL pin			0.2		W
Internal input capacitance				110		µF
Recommended external input ceramic capacitance, note 1			110			µF
Recommended external input bulk capacitance, note 1			470			µF
Output characteristics						
Output voltage	Default value			1.0		V
Output voltage adjust range			0.6		5.0	V
Output voltage adjust range including margining, note 8			0.57		5.25	V
Output voltage set-point resolution		0.6 V≤V_{out}≤ 1.2 V		10		mV
		1.2 V≤V_{out}≤ 2.4 V		20		mV
		2.4 V≤V_{out}≤ 5.0 V		40		mV
Output voltage accuracy	Including line, load and temperature		-1		1	% V_o

Electrical specifications for BMR4732001 (Vertical SIP)

Characteristic	descriptions	conditions	min	typical	max	unit
Output line regulation	I_{out} = max I_{out}	V_{out} = 0.6 V		1		mV
		V_{out} = 1.0 V		2		
		V_{out} = 1.8 V		2		
		V_{out} = 2.5 V		2		
		V_{out} = 3.3 V		2		
		V_{out} = 5.0 V		4		
Output load regulation	I_{out} = 0-100%	V_{out} = 0.6 V		1		mV
		V_{out} = 1.0 V		1		
		V_{out} = 1.8 V		1		
		V_{out} = 2.5 V		1		
		V_{out} = 3.3 V		1		
		V_{out} = 5.0 V		2		
Output ripple & noise, note 2	Up to 20 MHz bandwidth	V_{out} = 0.6 V		6		mVp-p
		V_{out} = 1.0 V		8		
		V_{out} = 1.8 V		11		
		V_{out} = 2.5 V		12		
		V_{out} = 3.3 V		12		
		V_{out} = 5.0 V		10		
Load transient voltage deviation, Load step 25-75-25% of max Io, note 3	di/dt=2 A/µs, C_{out} = 5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ)	V_{out} = 0.6 V		110		mV
		V_{out} = 1.0 V		110		
		V_{out} = 1.8 V		210		
		V_{out} = 2.5 V		270		
		V_{out} = 3.3 V		270		
		V_{out} = 5.0 V		180		
Load transient recovery time, Load step 25-75-25% of max Io, note 3	di/dt=2 A/µs, C_{out} = 5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ)	V_{out} = 0.6 V		400		µs
		V_{out} = 1.0 V		400		
		V_{out} = 1.8 V		400		
		V_{out} = 2.5 V		400		
		V_{out} = 3.3 V		400		
		V_{out} = 5.0 V		400		

Electrical specifications for BMR4732001 (Vertical SIP)

Characteristic	descriptions	conditions	min	typical	max	unit
Output current		0.6 V≤V_{out}≤ 1.8 V	0		40	A
		1.8 V<V_{out}≤ 3.3 V	0		30	A
		3.3 V<V_{out}≤ 5.0 V	0		20	A
Output current limit		0.6 V≤V_{out}≤ 1.8 V		52		A
		1.8 V<V_{out}≤ 3.3 V		39		A
		3.3 V<V_{out}≤ 5.0 V		26		A
Short circuit current	Hiccup mode, RMS value	V_{out} = 0.6 V		9.3		A
		V_{out} = 1.0 V		7.4		A
		V_{out} = 1.8 V		6.4		A
		V_{out} = 2.5 V		3.3		A
		V_{out} = 3.3 V		3.2		A
		V_{out} = 5.0 V		1.6		A
Efficiency (η)	50% of max I_{out}	V_{out} = 0.6 V		85.4		%
		V_{out} = 1.0 V		89.9		%
		V_{out} = 1.8 V		93.0		%
		V_{out} = 2.5 V		94.0		%
		V_{out} = 3.3 V		94.7		%
		V_{out} = 5.0 V		94.6		%
	100% of max I_{out}	V_{out} = 0.6 V		81.0		%
		V_{out} = 1.0 V		86.6		%
		V_{out} = 1.8 V		90.7		%
		V_{out} = 2.5 V		93.4		%
		V_{out} = 3.3 V		94.2		%
		V_{out} = 5.0 V		95.6		%
Power dissipation	at max I_{out}	V_{out} = 0.6 V		5.7	8.5	W
		V_{out} = 1.0 V		6.2	9	W
		V_{out} = 1.8 V		7.4	10	W
		V_{out} = 2.5 V		5.3	8	W
		V_{out} = 3.3 V		6.1	8	W
		V_{out} = 5.0 V		4.6	7	W
Internal output capacitance				350		µF
Recommended external output ceramic capacitance, note 4		0.6 V≤V_{out} ≤ 5.0 V	200	500		µF
Recommended external output bulk capacitance, note 4		0.6 V≤V_{out} ≤ 5.0 V	470	1880	10000	µF

Electrical specifications for BMR4731001 (Horizontal SMD)

Min and Max values are valid for: T_{P1} = -40 to + 85°C, V_{in}= 6 to 15 V, unless otherwise specified under conditions. Typical values given at: T_{P1} = +25°C, V_{in}= 12 V, max I_{out}, unless otherwise specified under conditions.

Additional external C_{in} = 8 x 22 µF ceramic + 470 µF OSCON (ESR 14 mΩ), C_{out}= 8 x 100 µF ceramic + 4 x 470 µF POSCAP (ERS 10 mΩ).

Characteristic	descriptions	conditions	min	typical	max	unit
Input characteristics						
Input voltage range (V_{in})		0.6 V≤V_{out}≤ 3.3 V	6	12	15	V
		3.3 V<V_{out}≤ 5.0 V	7	12	15	V
Input idling power	I_{out} = 0 A	V_{out} = 0.6 V		0.7		W
		V_{out} = 1.0 V		0.7		W
		V_{out} = 1.8 V		1.0		W
		V_{out} = 2.5 V		1.4		W
		V_{out} = 3.3 V		1.5		W
		V_{out} = 5.0 V		2.0		W
Input standby power	Turned off with CTRL pin			0.2		W
Internal input capacitance				68		µF
Recommended external input ceramic capacitance, note 1			176			µF
Recommended external input bulk capacitance, note 1			470			µF
Output characteristics						
Output voltage	Default value			1.0		V
Output voltage adjust range			0.6		5.0	V
Output voltage adjust range including margining, Note 8			0.57		5.25	V
Output voltage set-point resolution		0.6 V≤V_{out}≤ 1.2 V		10		mV
		1.2 V≤V_{out}≤ 2.4 V		20		mV
		2.4 V≤V_{out}≤ 5.0 V		40		mV
Output voltage accuracy	Including line, load and temperature		-1		1	% V_o

Electrical specifications for BMR4731001 (Horizontal SMD)

Characteristic	descriptions	conditions	min	typical	max	unit
Output line regulation	I_{out} = max I_{out}	V_{out} = 0.6 V		1		mV
		V_{out} = 1.0 V		1		
		V_{out} = 1.8 V		1		
		V_{out} = 2.5 V		1		
		V_{out} = 3.3 V		1		
		V_{out} = 5.0 V		1		
Output load regulation	I_{out} = 0-100%	V_{out} = 0.6 V		1		mV
		V_{out} = 1.0 V		1		
		V_{out} = 1.8 V		1		
		V_{out} = 2.5 V		1		
		V_{out} = 3.3 V		1		
		V_{out} = 5.0 V		1		
Output ripple & noise, note 2	Up to 20 MHz bandwidth	V_{out} = 0.6 V		4		mVp-p
		V_{out} = 1.0 V		5		
		V_{out} = 1.8 V		8		
		V_{out} = 2.5 V		10		
		V_{out} = 3.3 V		12		
		V_{out} = 5.0 V		15		
Load transient voltage deviation, Load step 25-75-25% of max Io, note 3	di/dt=2 A/µs, C_{out} = 8 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ)	V_{out} = 0.6 V		110		mV
		V_{out} = 1.0 V		110		
		V_{out} = 1.8 V		200		
		V_{out} = 2.5 V		260		
		V_{out} = 3.3 V		260		
		V_{out} = 5.0 V		180		
Load transient recovery time, Load step 25-75-25% of max Io, note 3	di/dt=2 A/µs, C_{out} = 8 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ)	V_{out} = 0.6 V		400		µs
		V_{out} = 1.0 V		400		
		V_{out} = 1.8 V		400		
		V_{out} = 2.5 V		400		
		V_{out} = 3.3 V		400		
		V_{out} = 5.0 V		400		

Electrical specifications for BMR4731001 (Horizontal SMD)

Characteristic	descriptions	conditions	min	typical	max	unit
Output current		0.6 V≤V_{out}≤ 1.8 V	0		40	A
		1.8 V<V_{out}≤ 3.3 V	0		30	A
		3.3 V<V_{out}≤ 5.0 V	0		20	A
Output current limit		0.6 V≤V_{out}≤ 1.8 V		52		A
		1.8 V<V_{out}≤ 3.3 V		39		A
		3.3 V<V_{out}≤ 5.0 V		26		A
Short circuit current	Hiccup mode, RMS value	V_{out} = 0.6 V		9.3		A
		V_{out} = 1.0 V		7.4		A
		V_{out} = 1.8 V		6.4		A
		V_{out} = 2.5 V		3.3		A
		V_{out} = 3.3 V		3.2		A
		V_{out} = 5.0 V		1.6		A
Efficiency (η)	50% of max I_{out}	V_{out} = 0.6 V		86.3		%
		V_{out} = 1.0 V		90.5		%
		V_{out} = 1.8 V		93.5		%
		V_{out} = 2.5 V		94.4		%
		V_{out} = 3.3 V		95.2		%
		V_{out} = 5.0 V		95.5		%
	100% of max I_{out}	V_{out} = 0.6 V		82.6		%
		V_{out} = 1.0 V		87.8		%
		V_{out} = 1.8 V		91.7		%
		V_{out} = 2.5 V		94.0		%
		V_{out} = 3.3 V		95.0		%
		V_{out} = 5.0 V		96.2		%
Power dissipation	at max I_{out}	V_{out} = 0.6 V		5.1	8.5	W
		V_{out} = 1.0 V		5.6	9	W
		V_{out} = 1.8 V		6.5	10	W
		V_{out} = 2.5 V		4.8	8	W
		V_{out} = 3.3 V		5.3	8	W
		V_{out} = 5.0 V		4.0	7	W
Internal output capacitance				72		µF
Recommended external output ceramic capacitance, note 4		0.6 V≤V_{out} ≤ 5.0 V	500	800		µF
Recommended external output bulk capacitance, note 4		0.6 V≤V_{out} ≤ 5.0 V	470	1880	10000	µF

Electrical specifications for BMR473

Characteristic	descriptions	conditions	min	typical	max	unit
Protection characteristics						
Input turn on voltage	Default value, Note 9	0.6 V≤V_{out}≤ 3.3 V		5.5		V
		3.3 V<V_{out}≤ 5.0 V		6.5		V
	PMBus configurable range		5.5		15	V
	Resolution			0.25		V
Input Under Voltage Lockout, UVLO	Default value, Note 10	0.6 V≤V_{out}≤ 3.3 V		4.5		V
		3.3 V<V_{out}≤ 5.0 V		5.5		V
	PMBus configurable range		4.5		15	V
	Resolution			0.25		V
Input Over Voltage Protection, IOVP	Default value			16		V
	PMBus configurable range		6		16	V
	Resolution			1		V
	Response delay			0		µs
	Fault response		Automatic restart, 70ms			
Output Over Voltage Protection, OVP	Default value			115		%
	PMBus configurable range		105		140	%
	Resolution			2.5		%
	Fault response		Automatic restart, 70ms			
Output Under Voltage Protection, UVP	Default value			85		%
	PMBus configurable range		60		95	%
	Resolution			2.5		%
	Response delay time			0		µs
	Fault response		Automatic restart, 70ms			
Over Current Protection, OCP	Default value, Note 11			52		A
	PMBus configurable range		8		52	A
	Resolution			2		A
	Response delay time		7 PWM cycles			
	Fault response		Automatic restart, 70ms			
Over Temperature Protection, OTP, note 5	Default value			135		°C
	PMBus configurable range		0		150	°C
	Resolution			1		°C
	Response delay time			0		µs
	Fault response		Automatic restart, 70ms			

Electrical specifications for BMR473

Characteristic	descriptions	conditions	min	typical	max	unit
Other characteristics						
Switching frequency (f_s)	Default value			450		kHz
	PMBus configurable range, note 6		450		900	kHz
	Set-point Accuracy		-10		10	%
Frequency synchronization, SYNC	SYNC output duty cycle			50		%
	SYNC input minimum pulse width				200	ns
	Allowable SYNC pin frequency difference from FREQUENCY_SWITCH frequency		-20		20	%
Initialization time				10		ms
Output voltage turn on delay time	Default value			10		ms
	PMBus configurable range (TON_DELAY)		0		127.5	ms
	Resolution			0.5		ms
	Accuracy		-10		15	%
Output voltage turn on ramp up time (0-100% of V_O)	Default value			10		ms
	PMBus configurable range (TON_RISE), note 7		0		31.75	ms
	Resolution			0.25		ms
	Accuracy		-10		15	%
Output voltage turn off delay time	Default value			0		ms
	PMBus configurable range (TOFF_DELAY), note 7		0		127.5	ms
	Resolution			0.5		ms
	Accuracy		-10		15	%
Output voltage turn off fall time (100-0% of Vo)	Default value		Disbaled, turn off immediately upon expiration of Turn off delay			
	PMBus configurable range (TOFF_FALL)		0		31.75	ms
	Resolution			0.25		ms
	Accuracy		-10		15	%
Power Good, PG	PG assertion threshold on V_O rising			95		% Vo
	PG de-assertion threshold on V_O falling			95		% Vo

Electrical specifications for BMR473

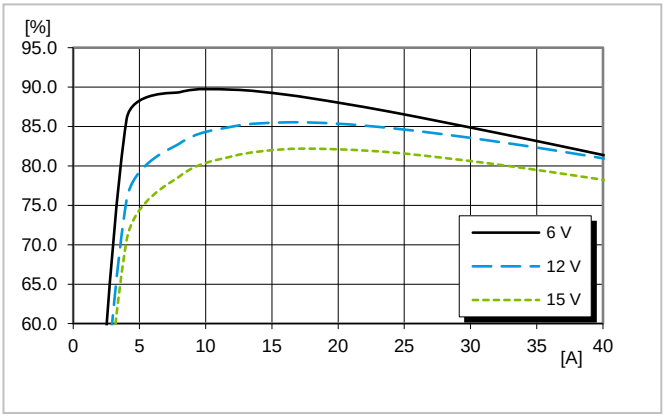
Characteristic	descriptions	conditions	min	typical	max	unit
Monitoring accuracy	Input voltage, READ_VIN		-3		3	%
	Output voltage, READ_VOUT		-2		2	%
	Output current, READ_IOUT		-5		5	A
	Temperature, READ_TEMPERATURE1		-3		3	°C
Logic output low level	SCL, SDA, SALERT, SYNC, PG, BCX_DAT, BCX_CLK				0.4	V
Logic output high level			2.25			V
Logic input low level	SCL, SDA, SYNC, CTRL				0.8	V
Logic input high level			1.35			V
Logic pin internal capacitance	PG			100		pF
Logic pin internal pull up resistance	PG to 5V, CTRL to 5V			10		kΩ
Supported PMBus operating frequency range			10		1000	kHz
SMBus Bus free time			0.5			µs
SMBus SDA setup time from SCL			0.26			µs
SMBus SDA hold time from SCL			0			µs
SMBus START/STOP condition setup/hold time			0.26			µs
SCL low period			0.5			µs
SCL high period			0.26			µs

Note 1: See section "Input capacitors" in "Design & Application Guide".
Note 2: See graph "Output ripple and noise".
Note 3: See graph "Transient response".
Note 4: See section "Output capacitors" in "Design & Application Guide".
Note 5: Temperature of Tp1, see section "Definition of product operating temperature".
Note 6: Effective switching frequency listed in section "Switching frequency" in "Design & Application Guide".
Note 7: Values less than 0.5 ms are supported as 0.5 ms.
Note 8: Should not exceed maximum output power 100 W.
Note 9: Change input turn on voltage to 6.5V when V_{out}>3.3 V.
Note 10: Change UVLO to 5.5 V when V_{out}>3.3 V.
Note 11: Decrease OCP when V_{out}>1.8 V.

Electrical graphs for **BMR4732001 (Vertical SIP)**

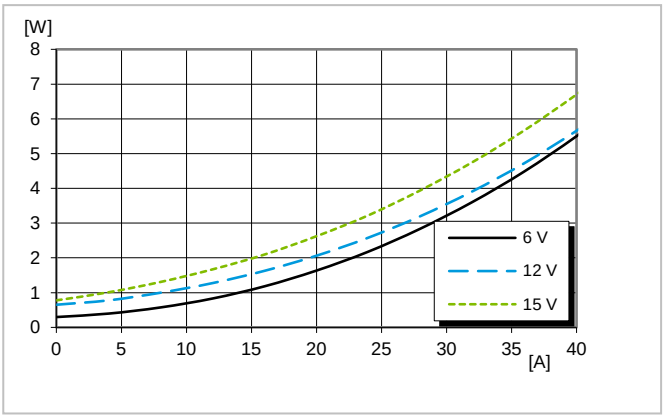
V_{out} = 0.6 V

Efficiency



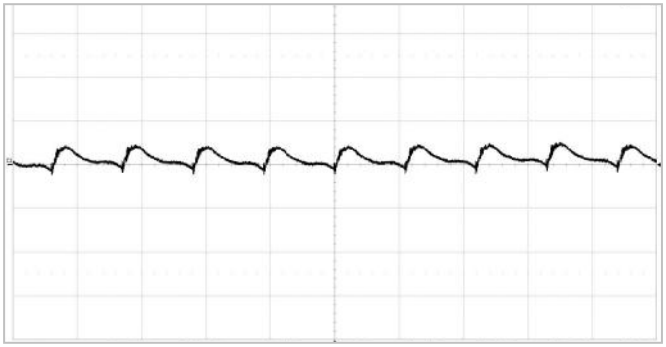
Efficiency vs. output current at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load current at T_{P1} = +25°C

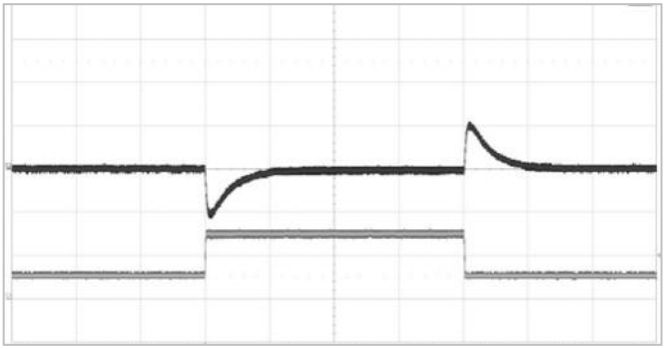
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



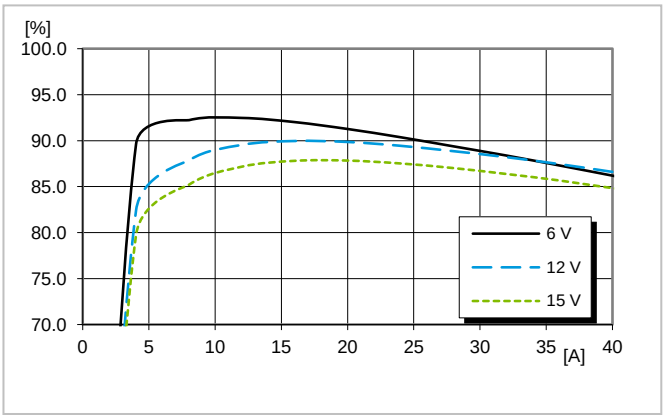
Output voltage response to output current change (10-30-10 A) at V_I=12V, C_O=5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4732001 (Vertical SIP)**

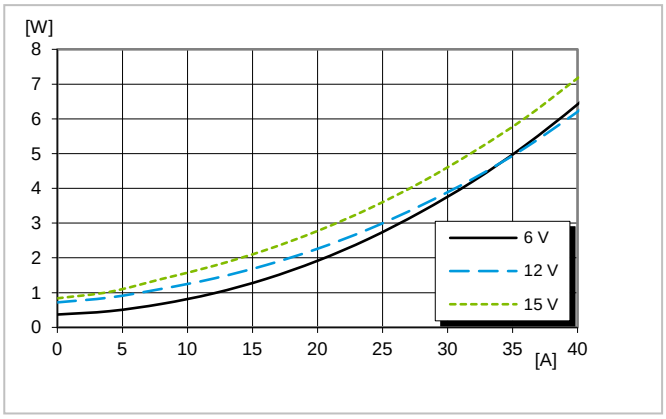
V_{out} = 1.0 V

Efficiency



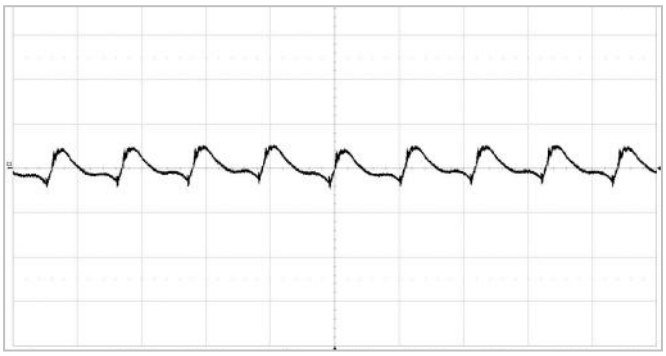
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

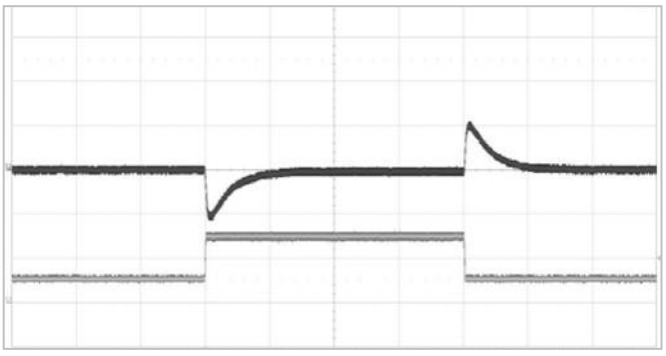
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



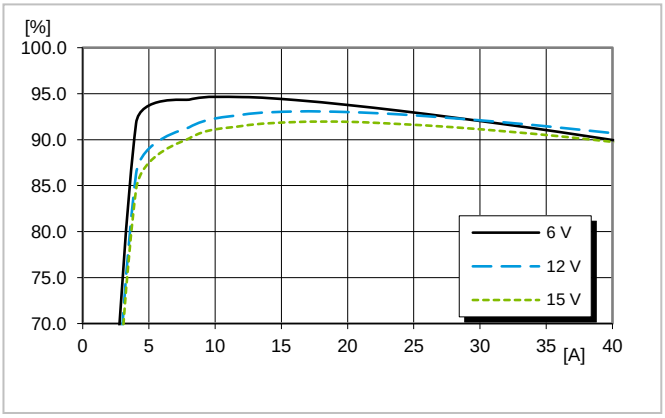
Output voltage response to output current change (10-30-10 A) at V_I=12V, C_O=5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4732001 (Vertical SIP)**

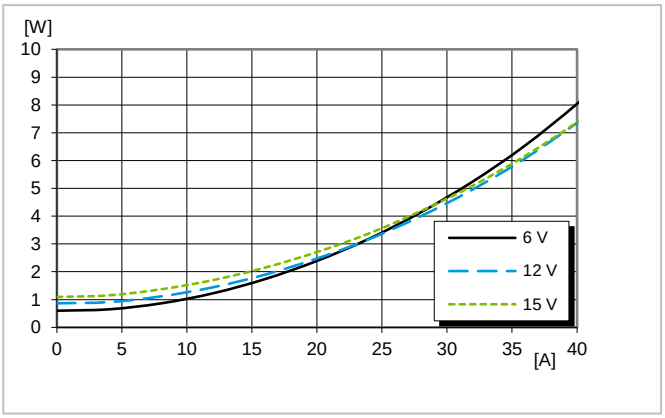
V_{out} = 1.8 V

Efficiency



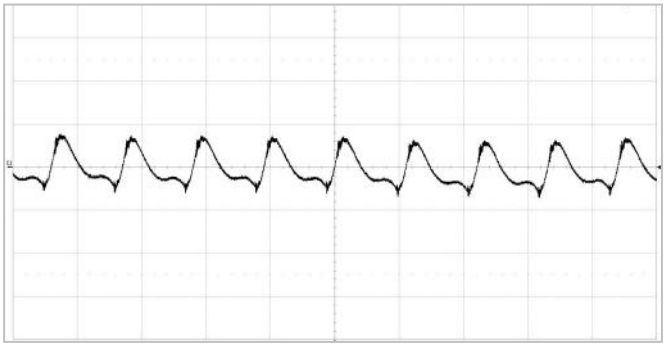
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

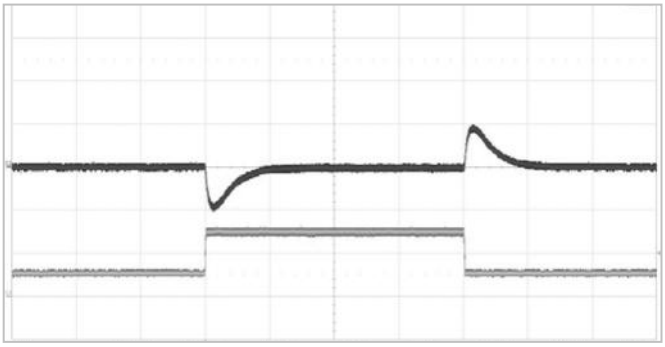
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



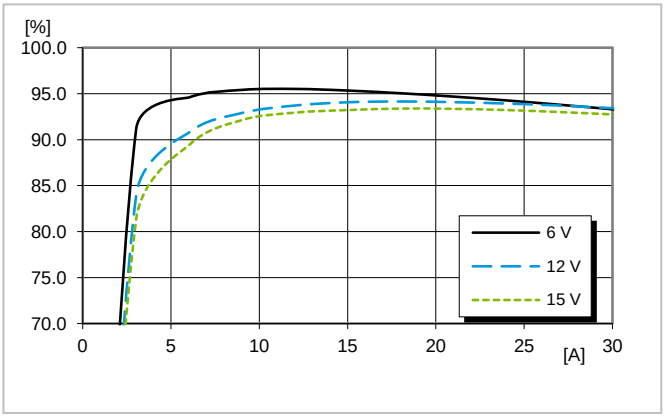
Output voltage response to output current change (10-30-10 A) at V_I=12V, C_O=5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4732001 (Vertical SIP)**

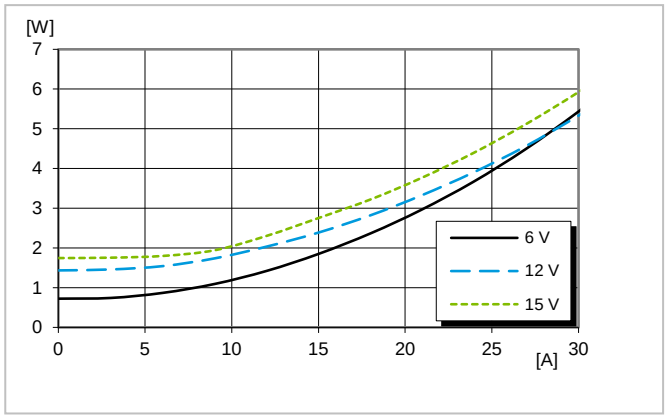
V_{out} = 2.5 V

Efficiency



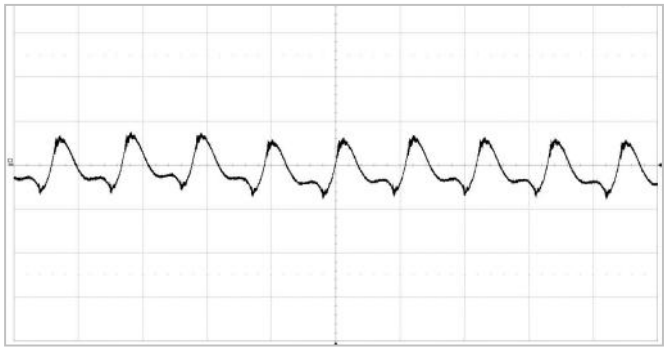
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

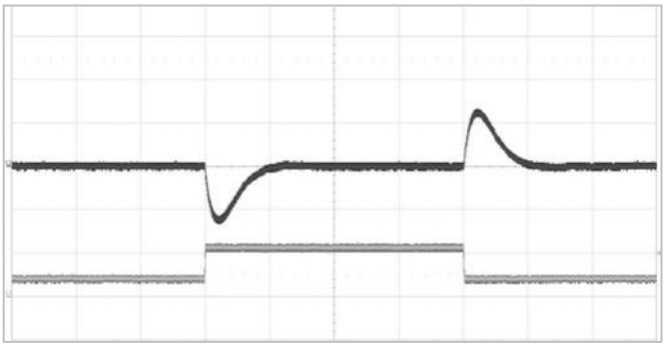
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



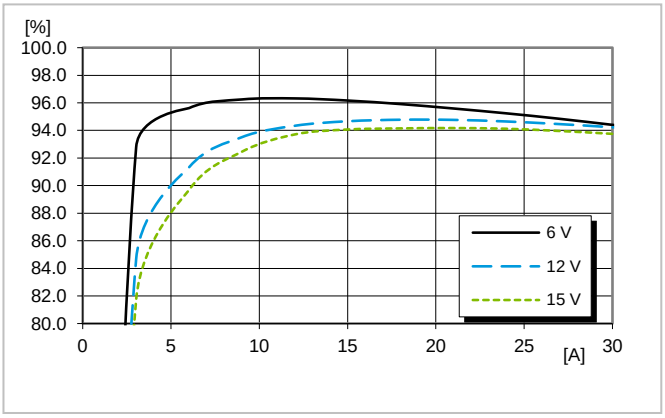
Output voltage response to output current change (7.5-22.5-7.5 A) at V_I=12V, C_O=5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4732001 (Vertical SIP)**

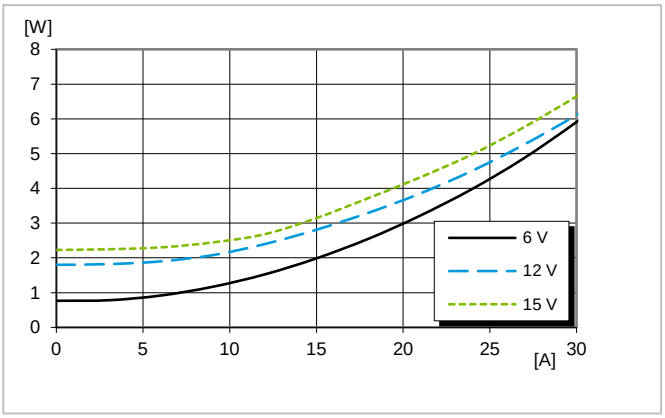
V_{out} = 3.3 V

Efficiency



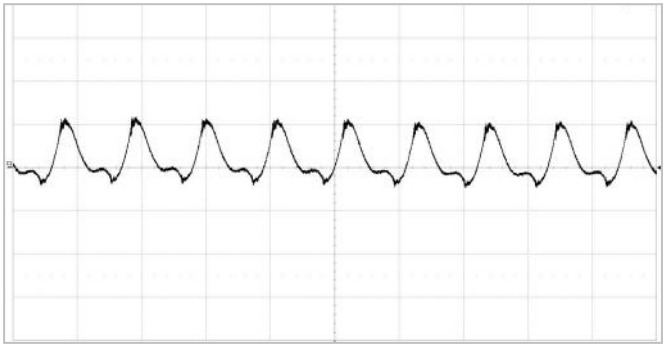
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

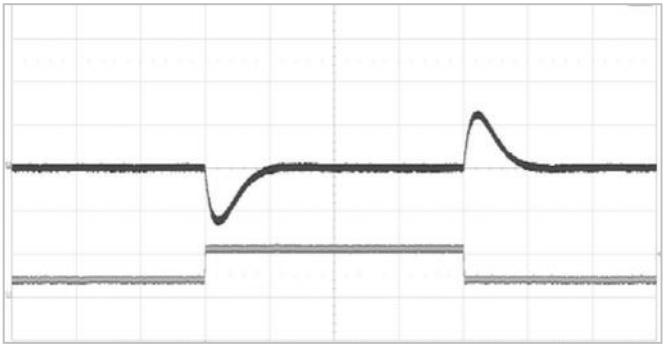
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



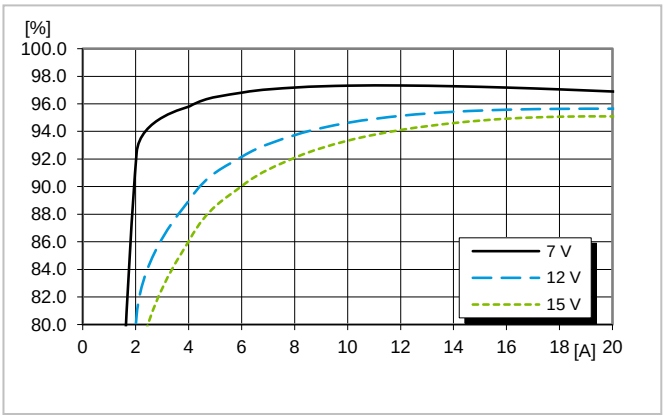
Output voltage response to output current change (7.5-22.5-7.5 A) at V_I=12V, C_O=5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4732001 (Vertical SIP)**

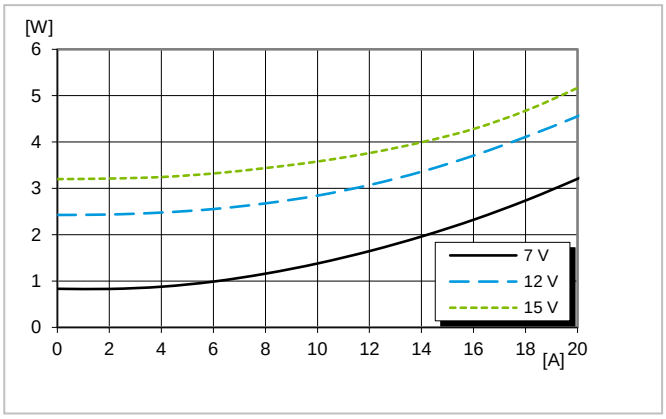
V_{out} = 5.0 V

Efficiency



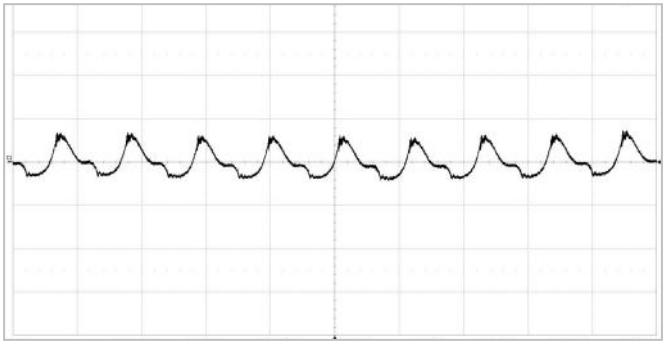
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

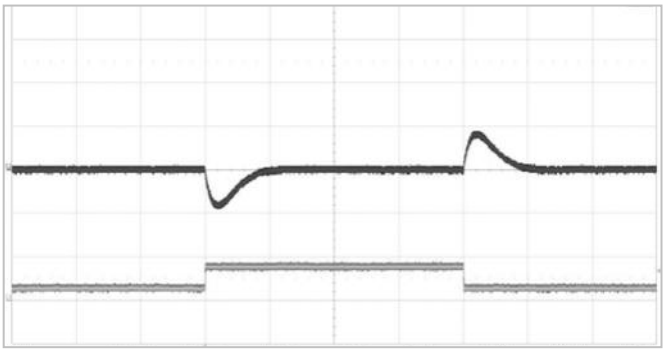
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



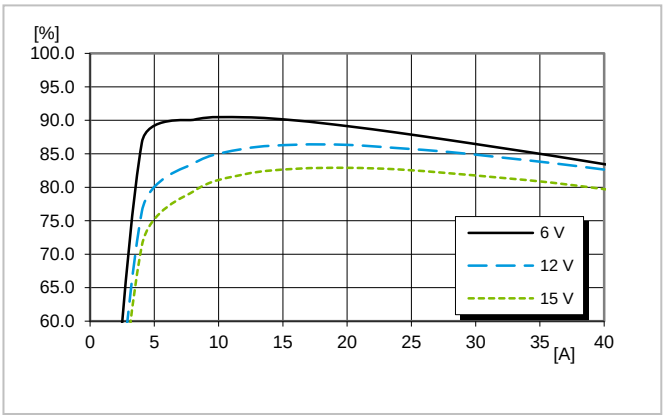
Output voltage response to output current change (5-15-5 A) at V_I=12V, C_O=5 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4731001 (Horizontal SMD)**

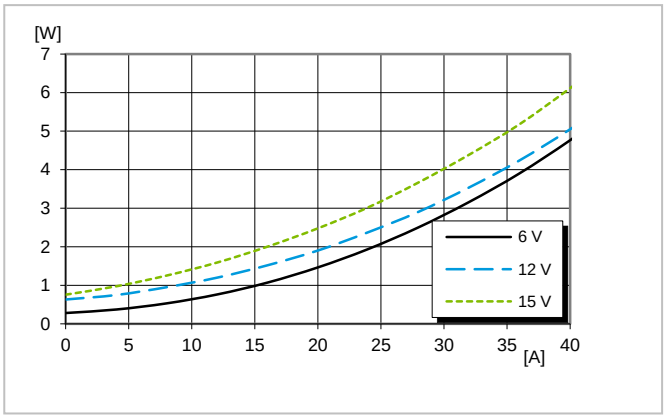
V_{out} = 0.6 V

Efficiency



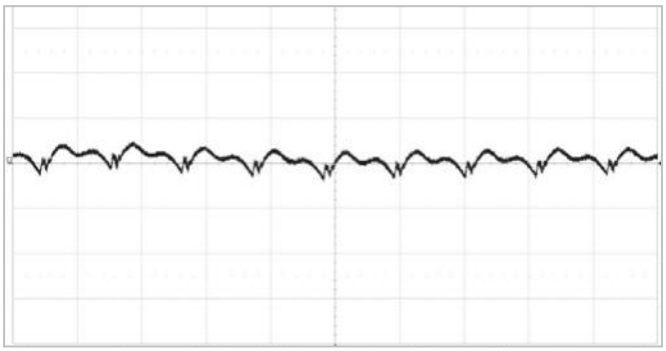
Efficiency vs. output current at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load current at T_{P1} = +25°C

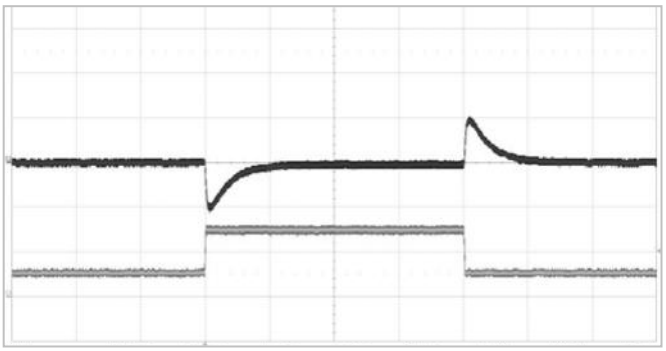
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



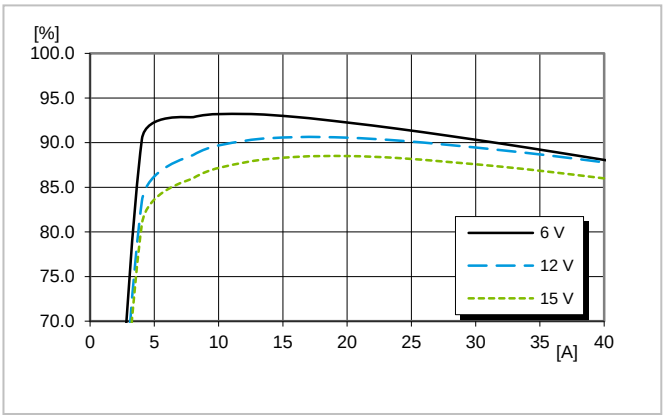
Output voltage response to output current change (10-30-10 A) at V_I=12V, C_O=8 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4731001 (Horizontal SMD)**

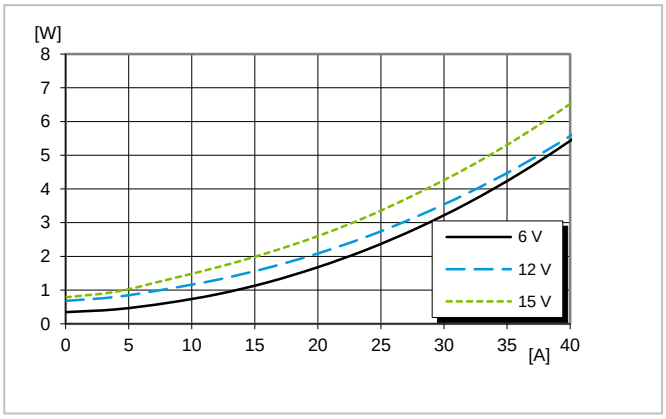
V_{out} = 1.0 V

Efficiency



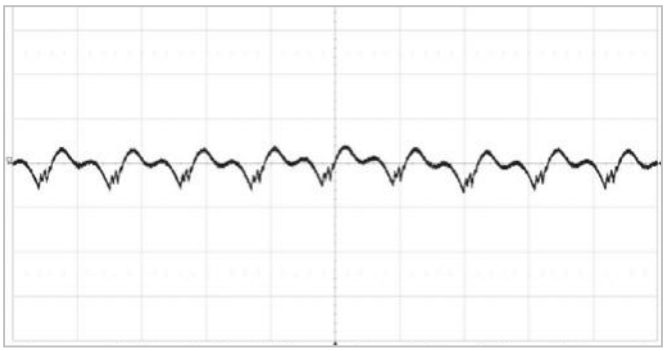
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

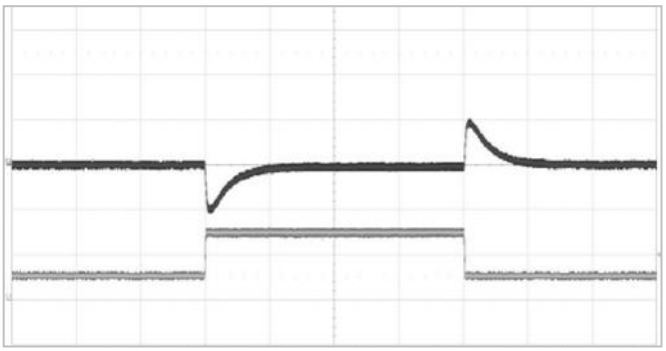
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



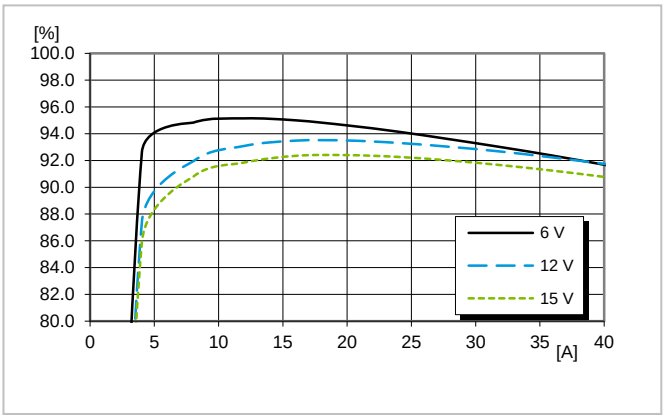
Output voltage response to output current change (10-30-10 A) at V_I=12V, C_O=8 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4731001 (Horizontal SMD)**

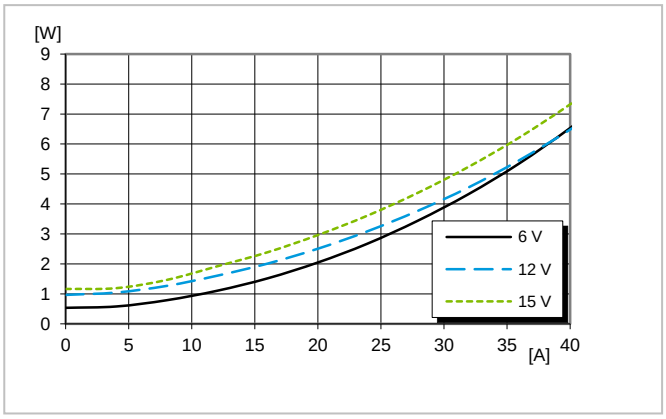
V_{out} = 1.8 V

Efficiency



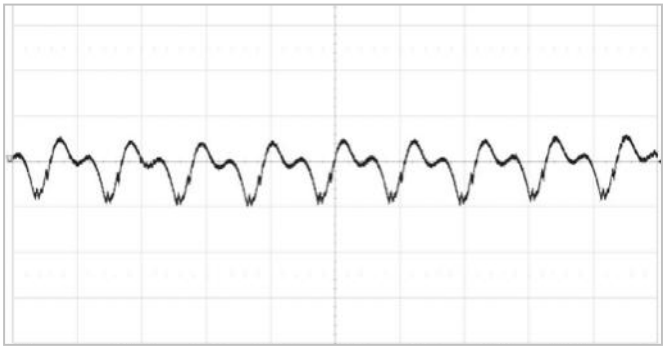
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

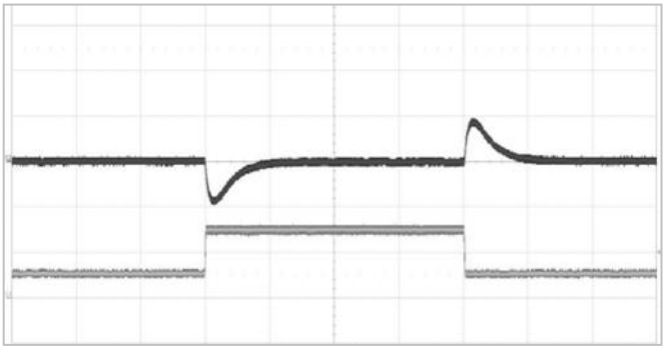
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



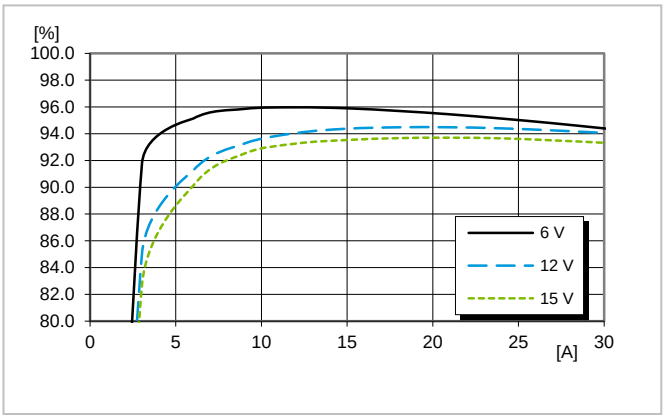
Output voltage response to output current change (10-30-10 A) at V_I=12V, C_O=8 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4731001 (Horizontal SMD)**

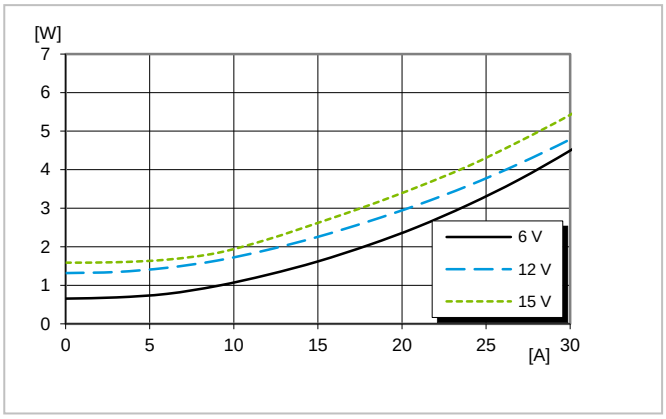
V_{out} = 2.5 V

Efficiency



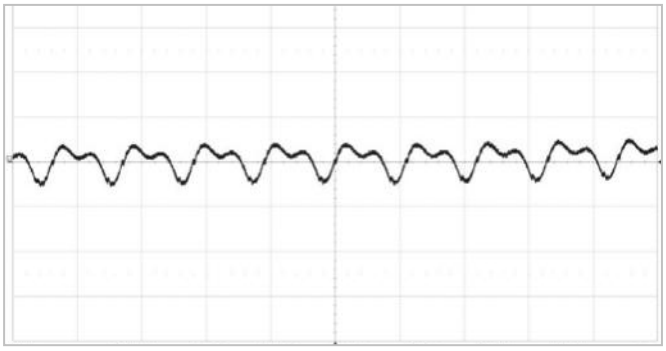
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

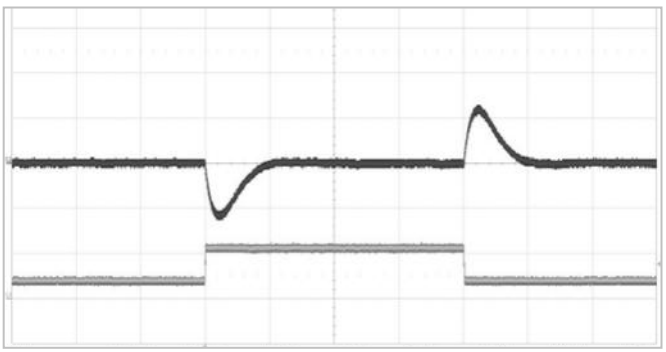
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 10 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



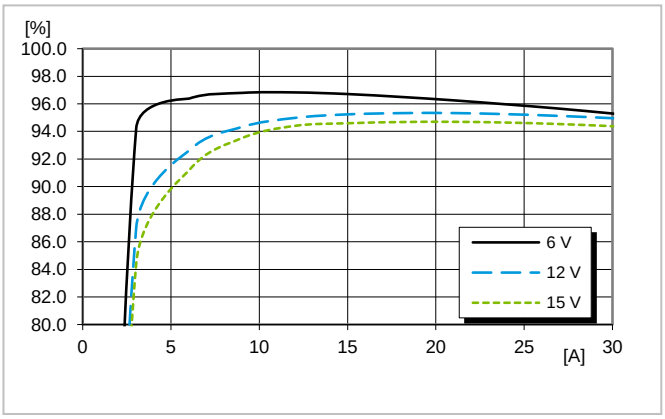
Output voltage response to output current change (7.5-22.5-7.5 A) at V_I=12V, C_O=8 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4731001 (Horizontal SMD)**

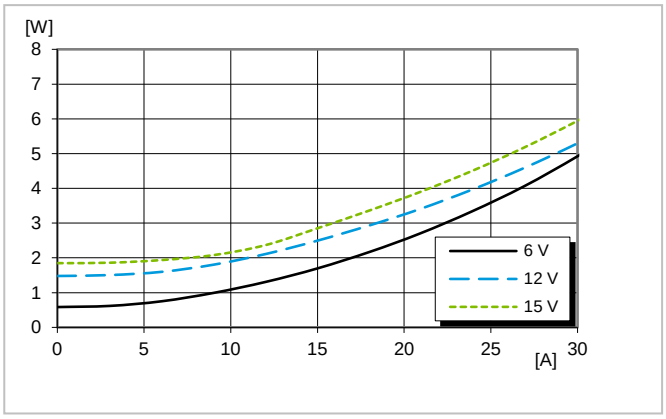
V_{out} = 3.3 V

Efficiency



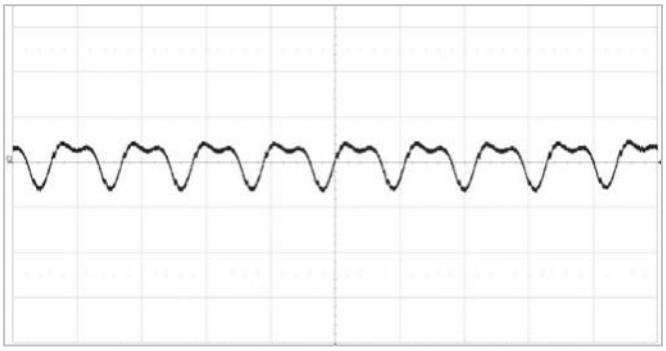
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

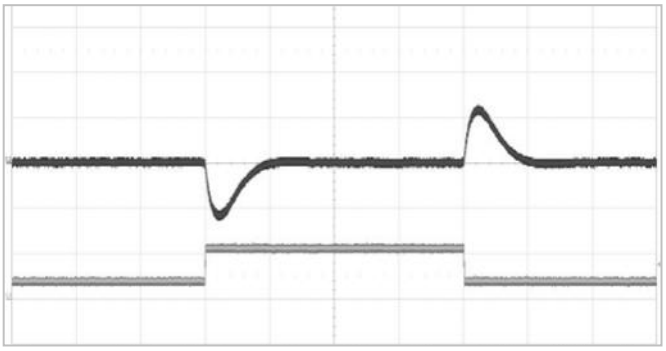
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 10 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response



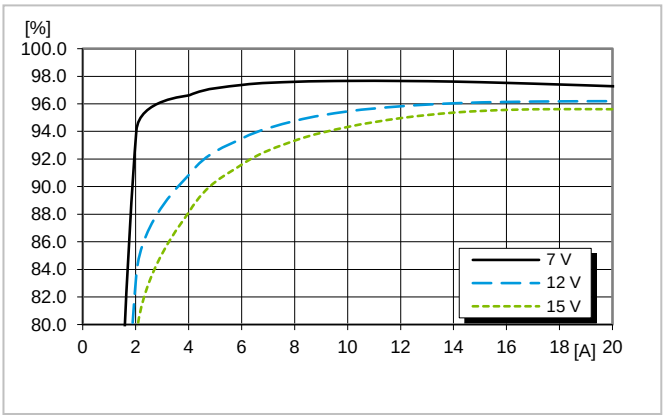
Output voltage response to output current change (7.5-22.5-7.5 A) at V_I=12V, C_O=8 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for **BMR4731001 (Horizontal SMD)**

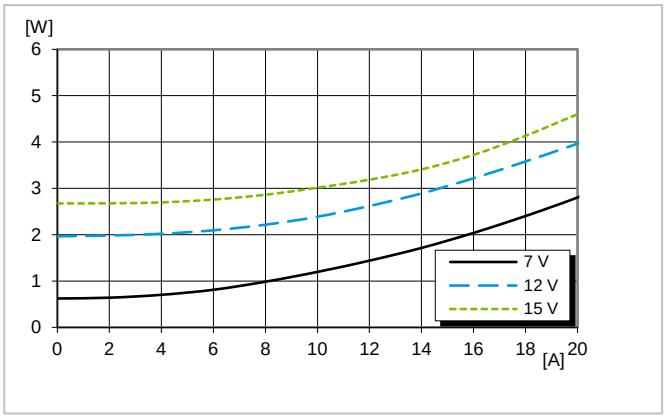
V_{out} = 5.0 V

Efficiency



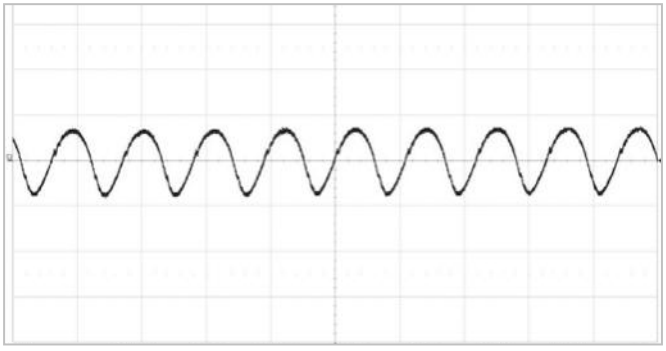
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

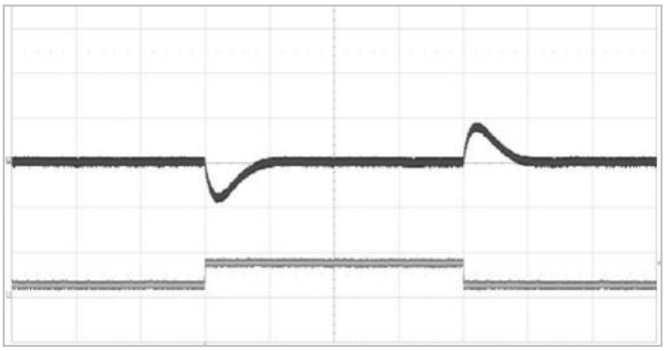
Output ripple and noise



Output voltage ripple at V_I=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 10 mV/div, 2 µs/div, 20 MHz bandwidth

Transient response

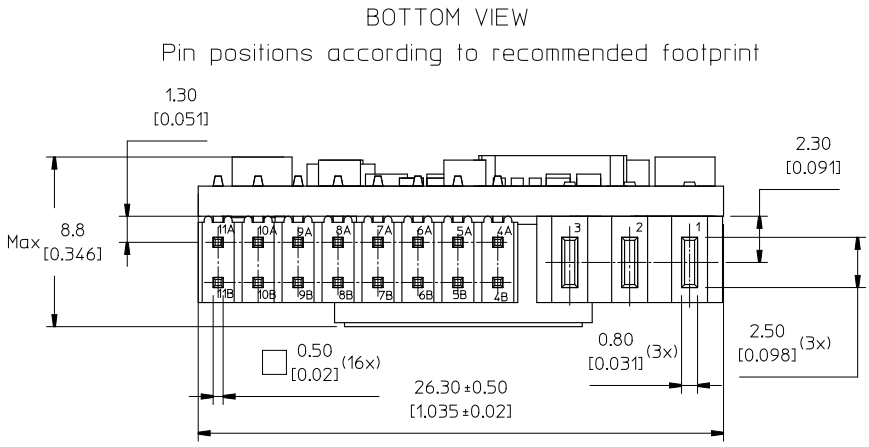


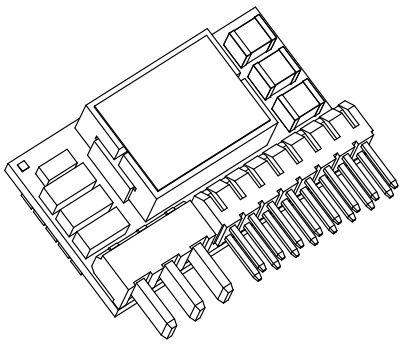
Output voltage response to output current change (5-15-5 A) at V_I=12V, C_O=8 x 100 µF ceramic + 4 x 470 µF POSCAP (ESR 10 mΩ), T_{P1} = +25°C, di/dt=2A/µs.

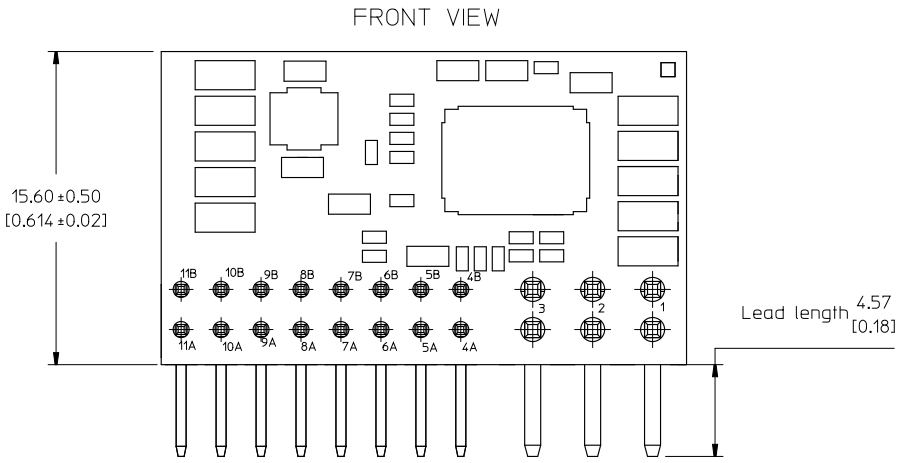
Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

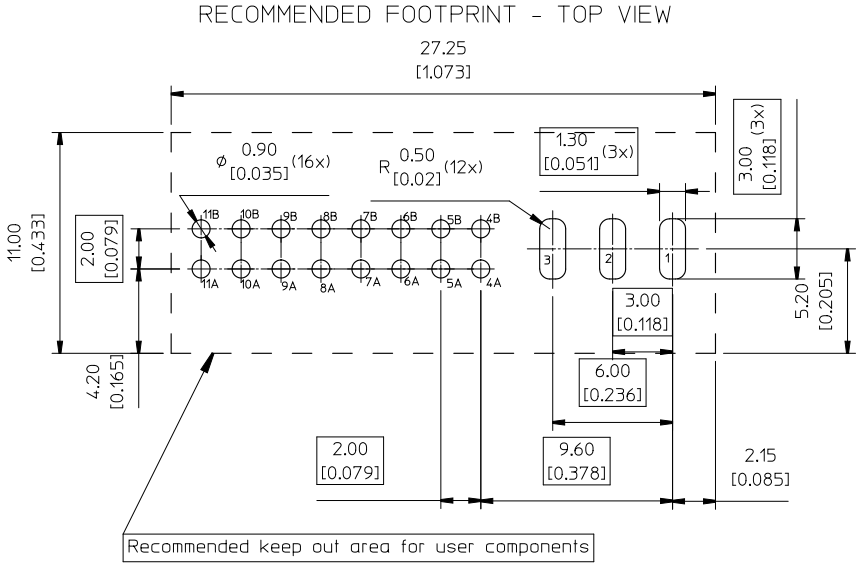
Part 2: Mechanical information

BMR473: hole mounted, Vertical SIP version







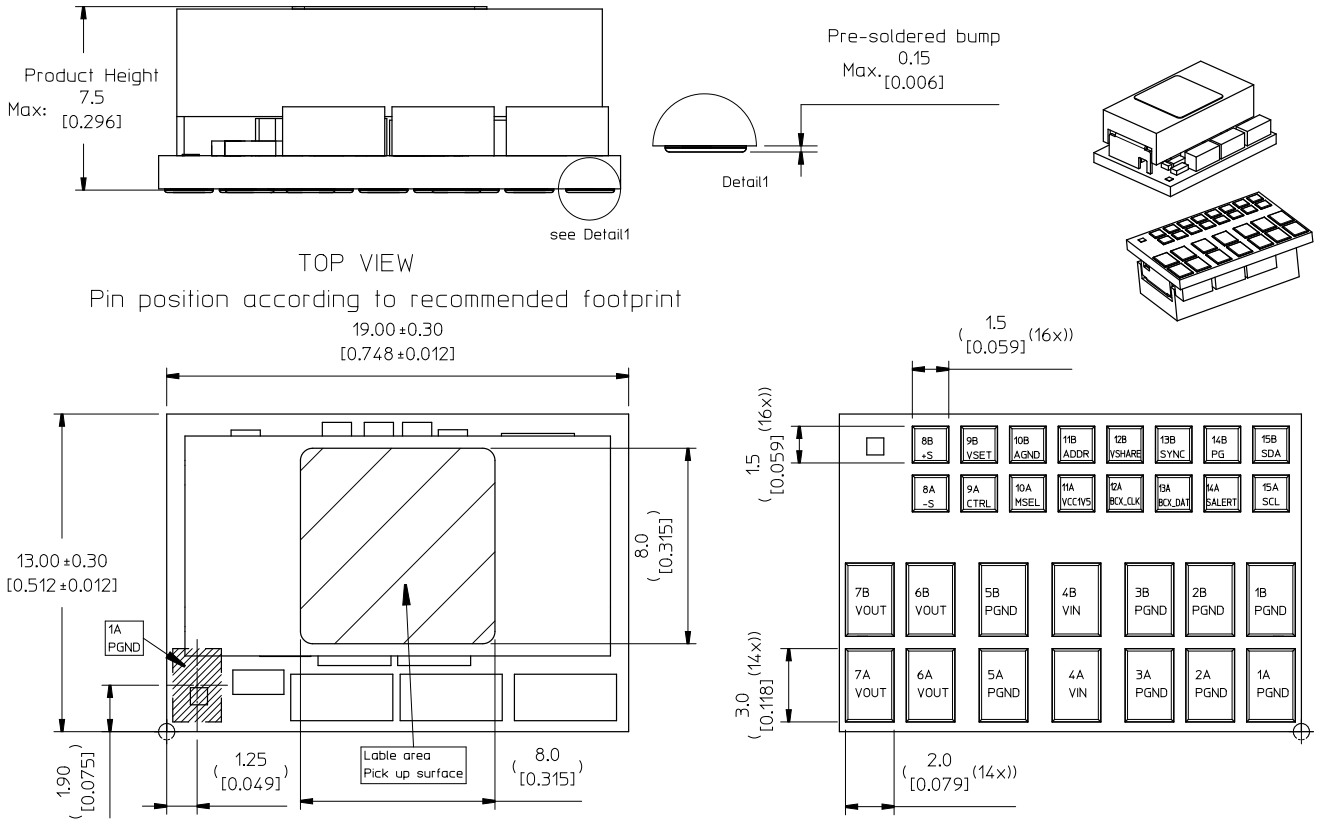


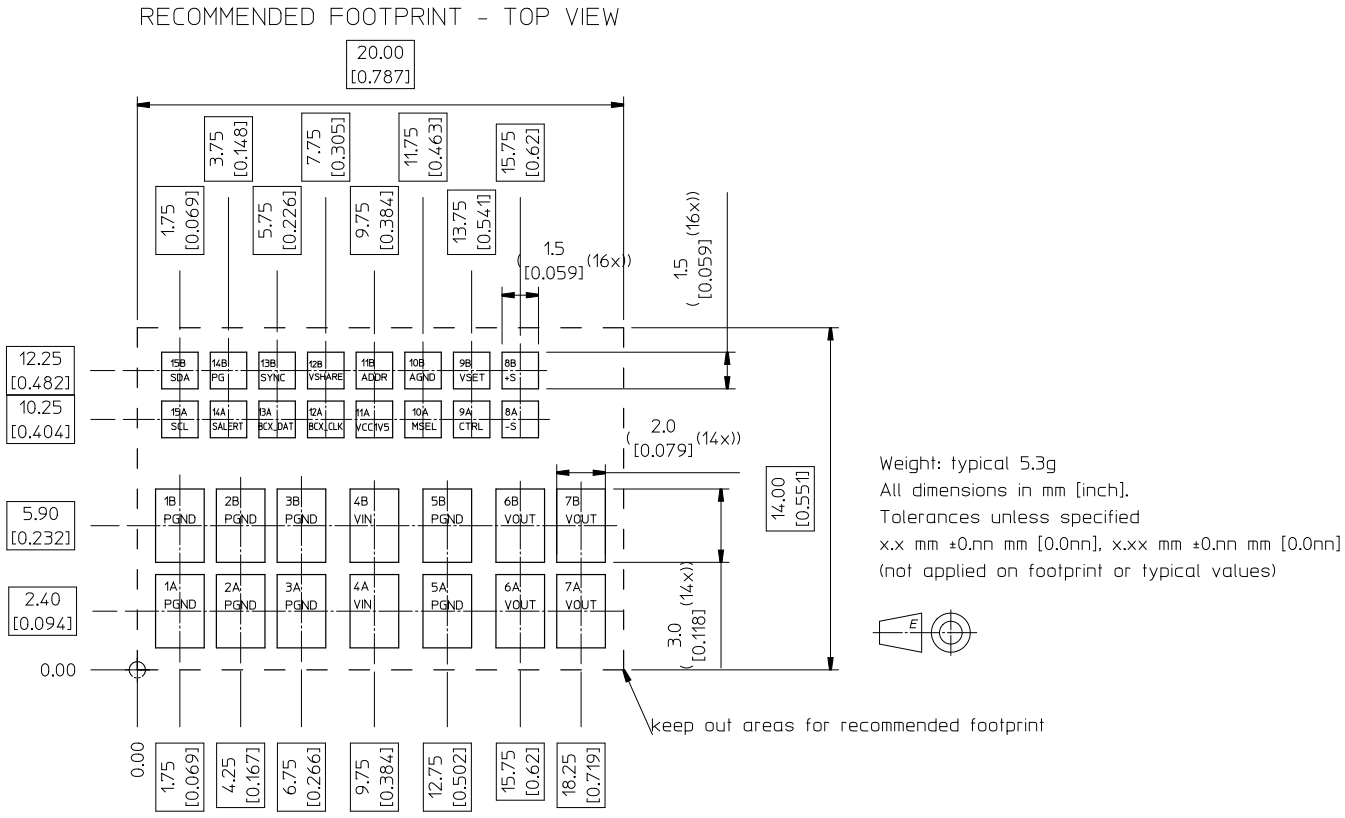
PIN SPECIFICATIONS
Pin 1-3 Material: Copper alloy (C11000)
Plating: Min Au 0.1 µm over 1-3 µm Ni.
Pin 4A-11B Material: Copper alloy
Plating: Min Au 0.1 µm over 1 µm Ni.

Weight: Typical 8.5 g
All dimensions in mm [inch]
Tolerances unless specified:
x.x ±0.50 [0.02]
x.xx±0.25 [0.01]
(not applied on footprint or typical values)

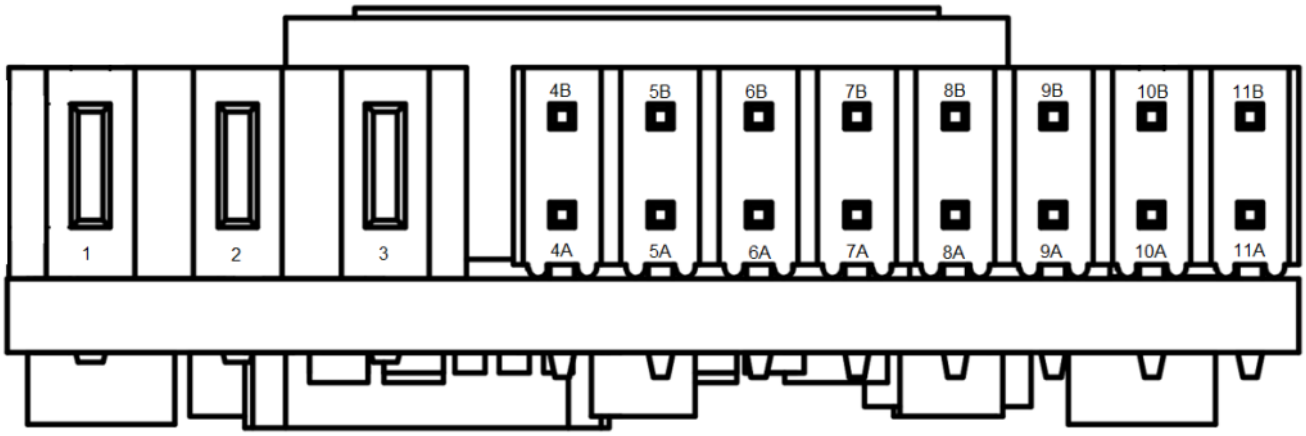
Part 2: Mechanical information

BMR473: Horizontal Surface Mount version





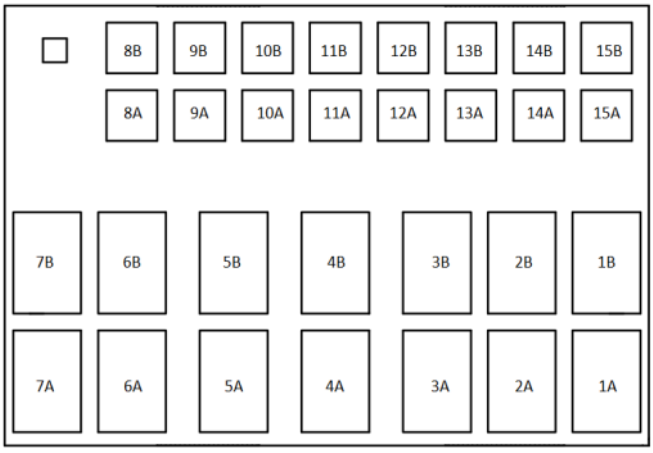
Connections for BMR4732001 (Vertical SIP)



Pin layout, bottom view, SIP

Pin	Designation	Type	Function
1	VIN	Power	Input voltage
2	GND	Power	Power ground
3	VOUT	Power	Output voltage
4A	SALERT	O, Open drain	PMBus Alert
4B	SCL	I/O	PMBus Clock
5A	SDA	I/O	PMBus Data
5B	PG	O, Open drain	PowerGood output
6A	BCX_DAT	I/O	Back-channel communications data
6B	BCX_CLK	I/O	Back-channel communications clock
7A	SYNC	I/O	Switching frequency synchronization
7B	VCC1V5	Power	Reference voltage for pin strapping
8A	AGND	Power	Ground reference for pin strapping
8B	VSHARE	I/O	Voltage sharing for paralleling
9A	VSET	I	Output voltage pin strap
9B	ADDR	I	PMBus address pin strap
10A	+S	I	Positive sense
10B	MSEL	I	Pin strap for soft-start time, over current fault limit and paralleling.
11A	-S	I	Negative sense
11B	CTRL	I	Remote Control

Connections for BMR4731001 (Horizontal SMD)



Pin layout, bottom view, horizontal mount SMD

Pin	Designation	Type	Function
1A,1B,2A,2B,3A,3B	GND	Power	Power ground
4A,4B	VIN	Power	Input voltage
5A,5B	GND	Power	Power ground
6A,6B,7A,7B	VOUT	Power	Output voltage
8A	-S	I	Negative sense
8B	+S	I	Positive sense
9A	CTRL	I	Remote Control
9B	VSET	I	Output voltage pin strap
10A	MSEL	I	Pin strap for soft-start time, over current fault limit and paralleling.
10B	AGND	Power	Ground reference for pin strapping
11A	VCC1V5	Power	Reference voltage for pin strapping
11B	ADDR	I	PMBus address pin strap
12A	BCX_CLK	I/O	Back-channel communications clock
12B	VSHARE	I/O	Voltage sharing for paralleling
13A	BCX_DAT	I/O	Back-channel communications data
13B	SYNC	I/O	Switching frequency synchronization
14A	SALERT	O, Open drain	PMBus Alert
14B	PG	O, Open drain	PowerGood output
15A	SCL	I/O	PMBus Clock
15B	SDA	I/O	PMBus Data

Part 3: Thermal considerations

Thermal considerations

The products are designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.

General

Cooling is mainly achieved by conduction from the pins to the host board and convection which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The products comes in a vertical SIP as well as horizontally mounted SMD version. For products mounted on a PWB without a heatsink attached, cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product. The wind speed and temperature are measured in a point upstream of the device. Distances between the tested device and the top space board and the side airflow guides are 6.35 mm ± 1 mm.

The product is tested on a 254 x 254 mm, 35 µm (1 oz), 8 layer test board mounted vertically in a wind tunnel with a cross section of 608 x 203 mm. .

The *output current derating graphs* found later in this section for each model provide the available output current vs. ambient air temperature and air velocity at V_{in} = 12 V.

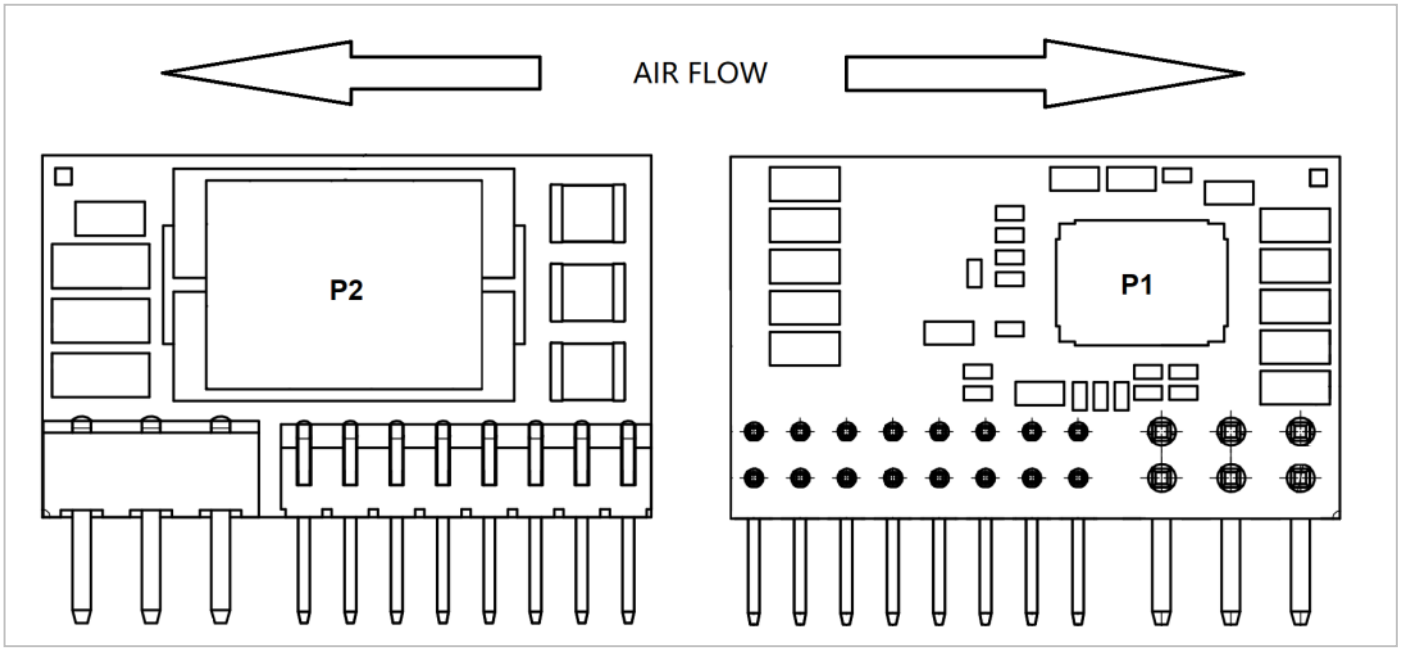
Definition of product operating temperature

Proper thermal conditions can be verified by measuring the temperature at position P1 as shown below. The temperature at this position (T_{P1}) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1}, measured at the reference point P1 are not allowed and may cause permanent damage.

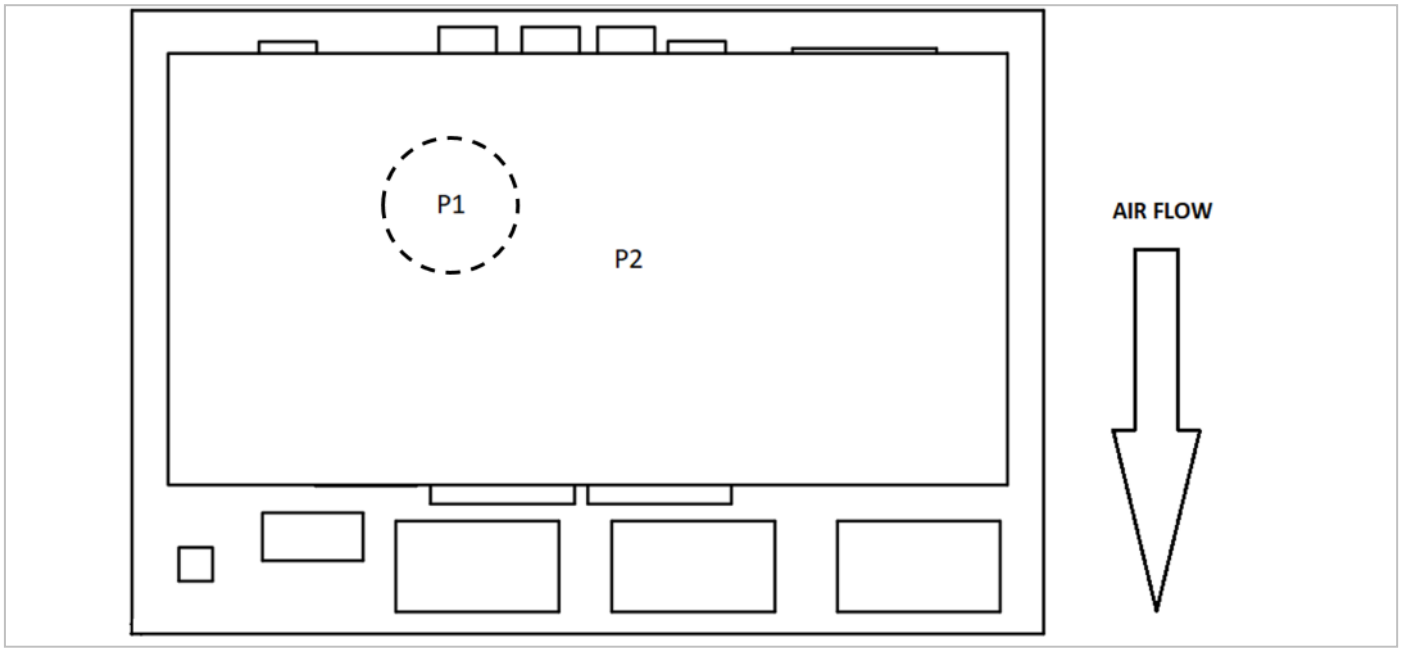
SIP Mounting		
Position	**Description**	**Max. Temp.**
P1	Controller	T_{P1}= 125 °C
P2	Inductor	T_{P2}= 125 °C

Horizontal Mounting		
Position	**Description**	**Max. Temp.**
P1	Controller	T_{P1}= 125 °C
P2	Inductor	T_{P2}= 125 °C

Temperature position and air flow direction



Temperature position and air flow direction, Vertical SIP

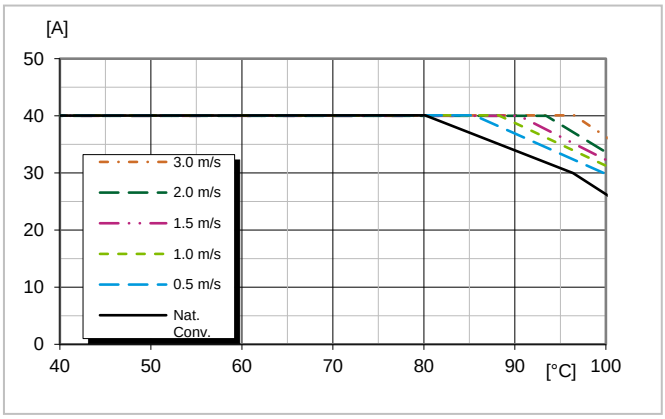


Temperature position and air flow direction, Horizontal mount SMD

Thermal graphs for BMR4732001 (Vertical SIP)

V_{out}= 0.6 V

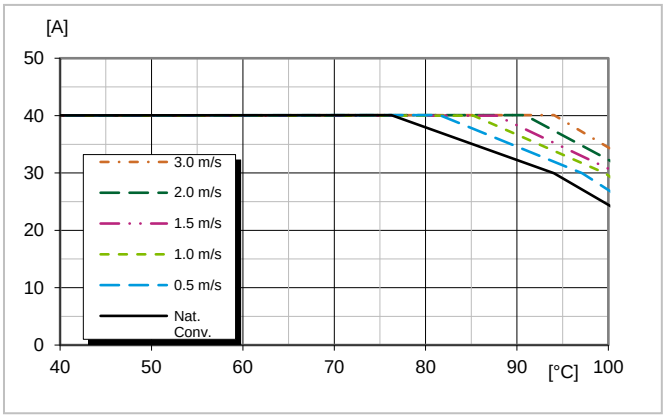
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=0.6V.

V_{out}= 1.0 V

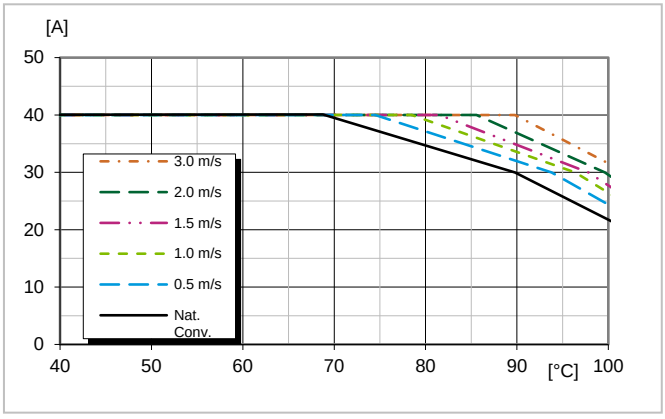
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=1.0V.

V_{out}= 1.8 V

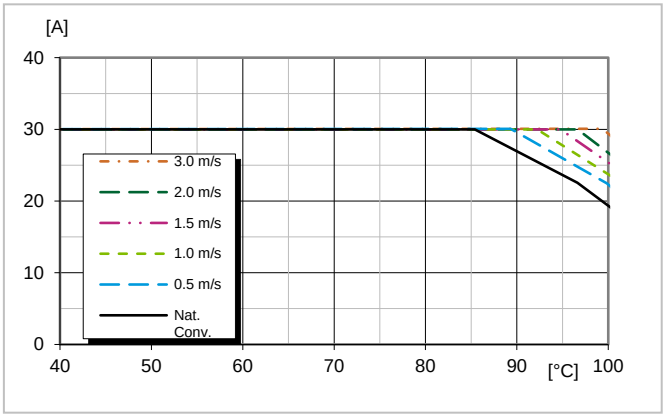
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=1.8V.

V_{out}= 2.5 V

Output current derating - open frame

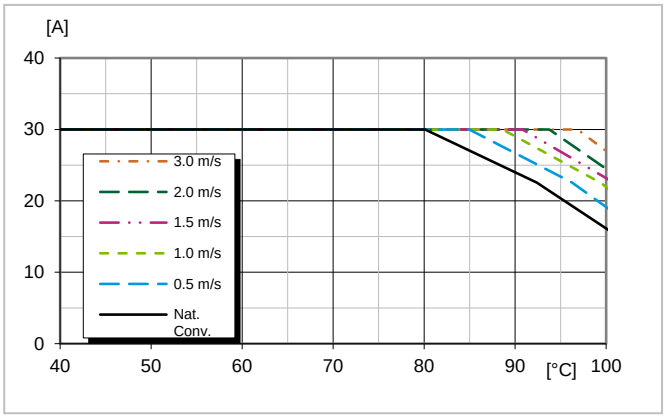


Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=2.5V.

Thermal graphs for BMR4732001 (Vertical SIP)

V_{out}= 3.3 V

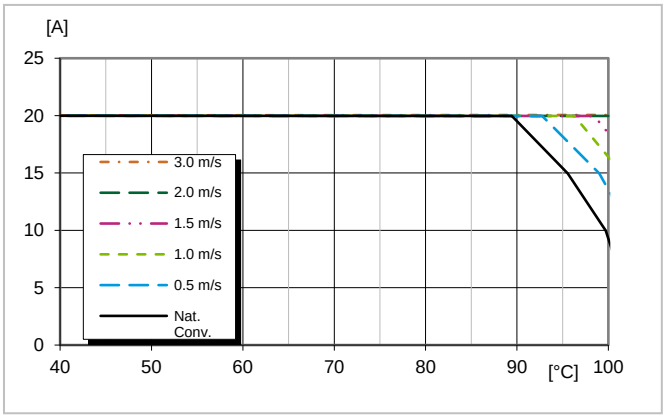
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=3.3V.

V_{out}= 5.0 V

Output current derating - open frame

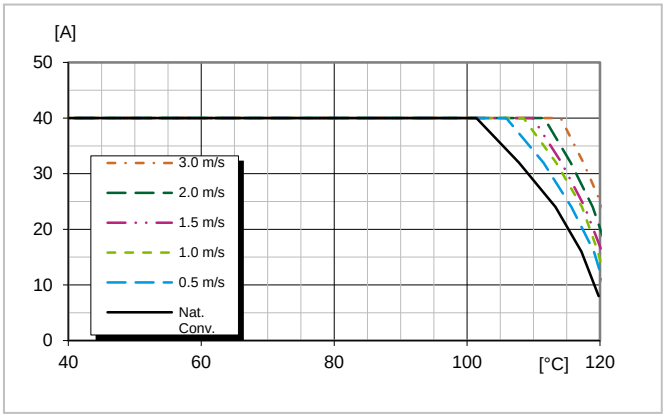


Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=5.0V.

Thermal graphs for BMR4731001 (Horizontal SMD)

V_{out}= 0.6 V

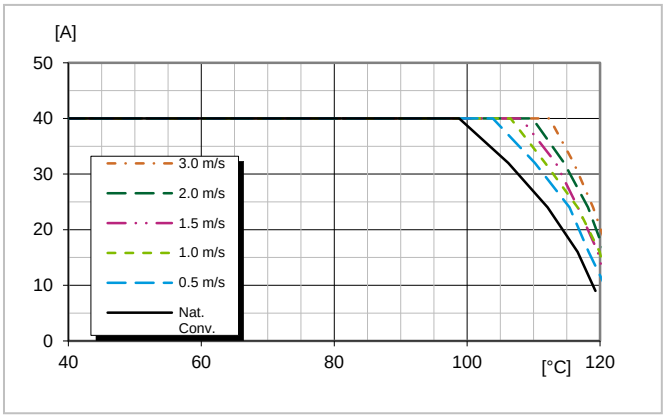
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=0.6V.

V_{out}= 1.0 V

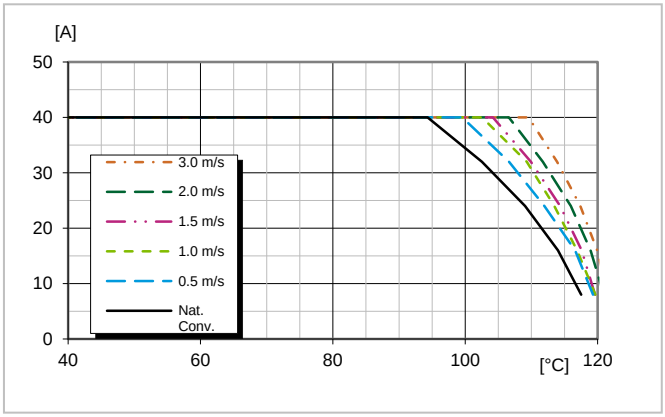
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=1.0V.

V_{out}= 1.8 V

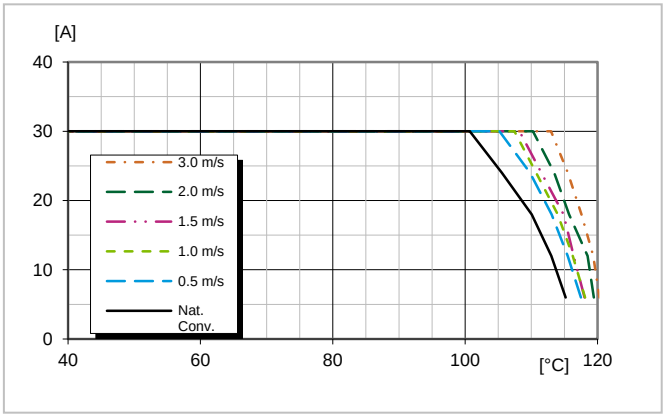
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=1.8V.

V_{out}= 2.5 V

Output current derating - open frame

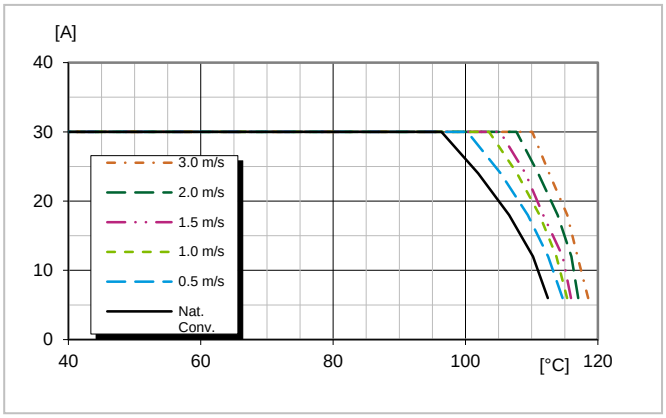


Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=2.5V.

Thermal graphs for BMR4731001 (Horizontal SMD)

V_{out}= 3.3 V

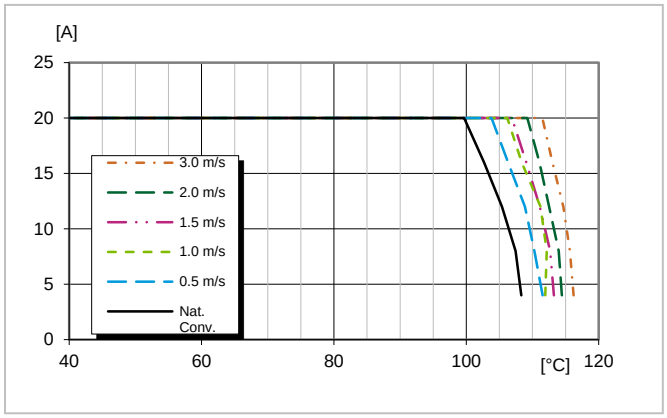
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=3.3V.

V_{out}= 5.0 V

Output current derating - open frame

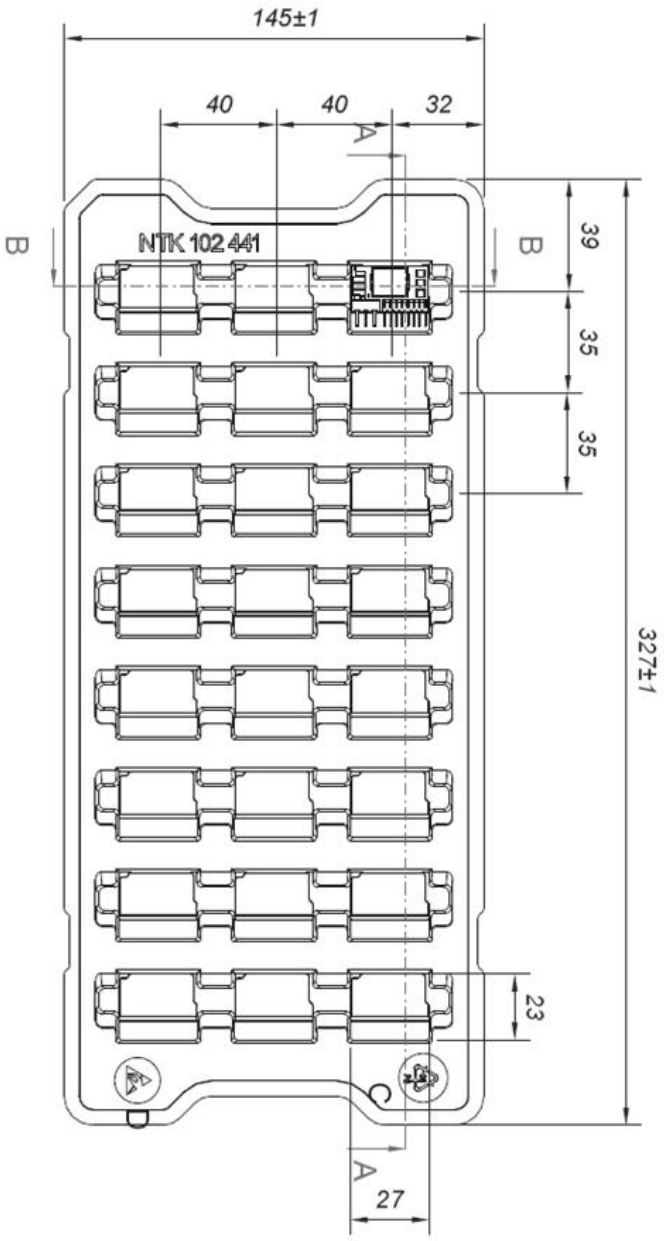


Available output current vs. ambient air temperature and airflow, V_I=12V, V_O=5.0V.

Part 4: Packaging

Packaging information— Vertical SIP

B option:	
Material	Antistatic Polystyrene (black)
Surface resistance	$10^5 <$ ohm/square $< 10^{11}$
Bakabilty	Trays are not bakeable
Tray thickness	20 mm (0.787 in) for SIP version
Box capacity	240 products (10 full trays/box)
Tray weight	47g empty tray, 255g full tray (SIP version)



All dimensions in mm [inch]

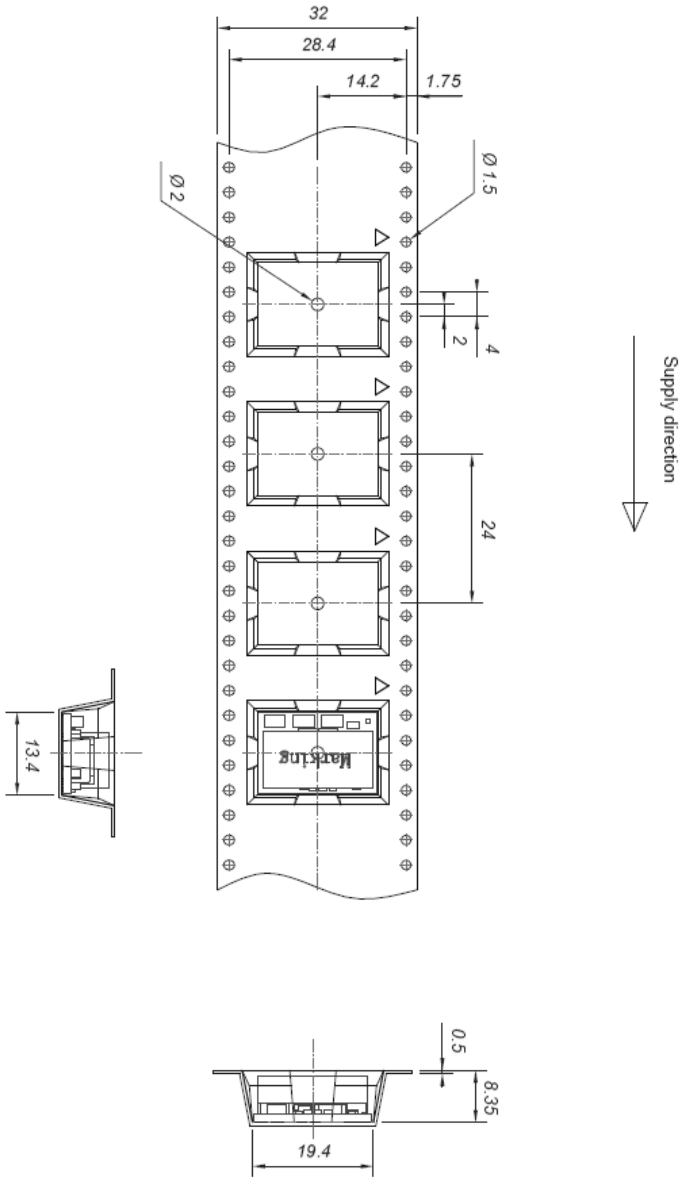
Tolerances: X.x ±0.26 [0.01], X.xx ±0.13 [0.005]

Note: The tray is not designed for machine pick up

Part 4: Packaging

Packaging information— Horizontal SMD

C option:	
Material	Antistatic Polystyrene (black)
Surface resistance	$10^5 <$ ohm/square $< 10^{11}$
Bakabilty	Trays are not bakeable
Tape width, W	32 mm [1.26 inch]
Pocket pitch, P_1	24 mm [0.94 inch]
Pocket depth, K_0	8.35 mm [0.33 inch]
Reel diameter	381 mm [15 inch]
Reel capacity	200 products /reel
Reel weight	1.5 kg/full reel



Part 5: Revision history

Revision table

Revision number	revision change	date	revisor
Rev. A	First release edition.	2022-06-30	JIDMWANG
Rev. B	Add variant of BMR4731001	2023-01-05	JIDMWANG
Rev. C	Minor changes	2024-01-26	KARWAER
Rev. D	Update pin description in	2025-02-04	JIDJLIAA