

BMR473

40A digital PoL regulator

The BMR473 is a digital PoL regulator available in a vertical SIP or horizontal mount package for board space optimization. The BMR473 is a single-phase converter with high power density. It is designed for telecom and datacom applications.



Key features

- High efficiency up to 95.6% at 12 Vin, 5 Vout full load.
- Paralleling up to 4 units (160A)
- Remote control
- Power Good
- Synchronization and phase spreading
- Excellent thermal performance
- Configuration and monitoring via PMBus

Soldering methods

- Wave soldering (SIP)
- Reflow (SIP and laydown)

Key electrical information

Parameter	Values
Input voltage range	6 - 15 V
Output voltage range	0.6 - 5 V
Max output current	40 A

Mechanical

26.3 x 8.8 x 15.6 mm / 1.035 x 0.346 x 0.614 in (SIP)

Application areas

- Telecom
- Datacom

Product options

The table below describes the different product options.

Example: BMR473 2 0 01 /001						B	Definitions
Product family	BMR473						
Mounting options		2					1 = Surface mount 2 = Single in line package (SIP)
Pin length options			0				0 = standard (4.57 mm) 1 = short pin option (3.69 mm) 2 = long pin option (5.33 mm)
Other hardware variants				01			01 = standard
Configuration code					/001		/001 = standard config. (positive remote control)
Packaging options						B	B = tray (one full package with 240 pieces)

For more information, please refer to Part 2 [Mechanical information](#).

If you do not find the variant you are looking for, please contact us at [Flex Power Modules](#).

Order number examples

Part number	V _{in}	outputs	configuration
BMR4732001/001	6 – 15 V	0.6 – 5 V, 40 A/100W	4.57 mm pins / positive logic / dry pack, tray

Part 1: Electrical specifications

Absolute maximum ratings

Stress in excess of our defined *absolute maximum ratings* may cause permanent damage to the converter. Absolute maximum ratings, also referred to as *non-destructive limits*, are normally tested with one parameter at a time exceeding the limits in the electrical specification.

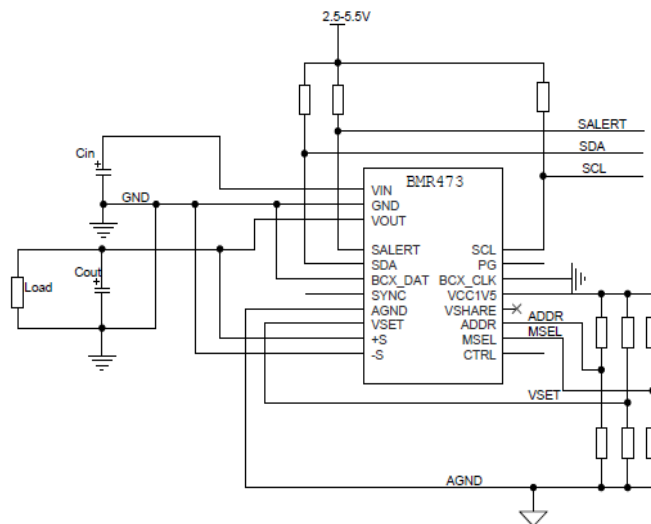
Characteristics		min	typ	max	Unit
Operating temperature (T _{P1})		-40		125	°C
Storage temperature		-40		125	°C
Input voltage (V _{in})		-0.3		16	V
Signal I/O voltage	SCL, SDA, SALERT, SYNC, BCX_DAT, BCX_CLK, CTRL, PG	-0.3		5.5	V
Ground voltage differential	-S, AGND, GND	-0.3		0.3	V
Analog pin voltage	V _{out} , +S	-0.3		5.5	V
	ADDR, VSET, MSEL	-0.3		1.65	V

Reliability

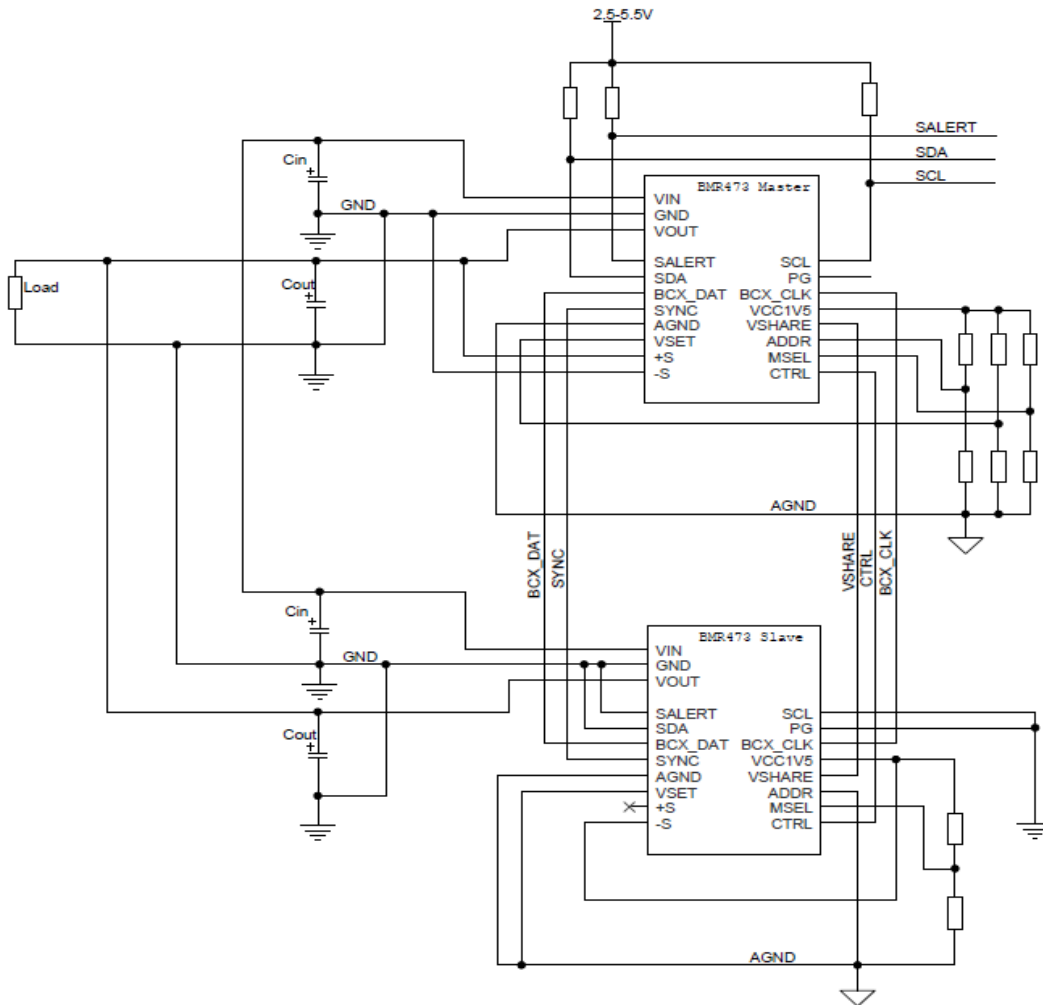
Failure rate (λ) and mean time (50%) between failures (MTBF= 1/ λ) are calculated based on *Telcordia SR-332 Issue 4: Method 1, Case 3, (80% of I_{out}, T_{P1}=40°C, Airflow=200 LFM)*.

	Mean	90% confidence level	Unit
Steady-state failure rate (λ)	26	32	nfailures/h
Standard deviation (σ)	4.9		nfailures/h
MTBF	38.39	30.97	MHr

Typical application diagram (Stand Alone)



Typical application diagram (2 modules paralleling)



Electrical specifications for BMR4732001

Min and Max values are valid for: $T_{P1} = -40$ to $+85^{\circ}\text{C}$, $V_{in} = 6$ to 15 V, unless otherwise specified under conditions. Typical values given at: $T_{P1} = +25^{\circ}\text{C}$, $V_{in} = 12$ V, max I_{out} , unless otherwise specified under conditions.

Additional external $C_{in} = 5 \times 22 \mu\text{F}$ ceramic + $470 \mu\text{F}$ OSCON, $C_{out} = 5 \times 100 \mu\text{F}$ ceramic + $4 \times 470 \mu\text{F}$ POSCAP.

Characteristic	descriptions	conditions	min	typical	max	unit
Input characteristics						
Input voltage range (V_{in})		$0.6 \text{ V} \leq V_{out} \leq 3.3 \text{ V}$	6	12	15	V
		$3.3 \text{ V} < V_{out} \leq 5.0 \text{ V}$	7	12	15	V
Input idling power	$I_{out} = 0 \text{ A}$	$V_{out} = 0.6 \text{ V}$		0.7		W
		$V_{out} = 1.0 \text{ V}$		0.7		W
		$V_{out} = 1.8 \text{ V}$		1.0		W
		$V_{out} = 2.5 \text{ V}$		1.4		W
		$V_{out} = 3.3 \text{ V}$		1.7		W
		$V_{out} = 5.0 \text{ V}$		2.5		W
Input standby power	Turned off with CTLR pin			0.2		W
Internal input capacitance				110		μF
Recommended external input ceramic capacitance			110			μF
Recommended external input bulk capacitance,			470			μF
Output characteristics						
Output voltage	Default value			1.0		V
Output voltage adjust range			0.6		5.0	V
Output voltage adjust range including margining			0.57		5.25	V
Output voltage set-point resolution		$0.6 \text{ V} \leq V_{out} \leq 1.2 \text{ V}$		10		mV
		$1.2 \text{ V} \leq V_{out} \leq 2.4 \text{ V}$		20		mV
		$2.4 \text{ V} \leq V_{out} \leq 5.0 \text{ V}$		40		mV
Output voltage accuracy	Including line, load and temperature		-1		1	% V_o

Electrical specifications for BMR4732001

Characteristic	descriptions	conditions	min	typical	max	unit
Output line regulation	$I_{out} = \max I_{out}$	$V_{out} = 0.6\text{ V}$		1		mV
		$V_{out} = 1.0\text{ V}$		2		
		$V_{out} = 1.8\text{ V}$		2		
		$V_{out} = 2.5\text{ V}$		2		
		$V_{out} = 3.3\text{ V}$		2		
		$V_{out} = 5.0\text{ V}$		4		
Output load regulation	$I_{out} = 0\text{-}100\%$	$V_{out} = 0.6\text{ V}$		1		mV
		$V_{out} = 1.0\text{ V}$		1		
		$V_{out} = 1.8\text{ V}$		1		
		$V_{out} = 2.5\text{ V}$		1		
		$V_{out} = 3.3\text{ V}$		1		
		$V_{out} = 5.0\text{ V}$		2		
Output ripple & noise, note 2	Up to 20 MHz bandwidth	$V_{out} = 0.6\text{ V}$		6		mVp-p
		$V_{out} = 1.0\text{ V}$		8		
		$V_{out} = 1.8\text{ V}$		11		
		$V_{out} = 2.5\text{ V}$		12		
		$V_{out} = 3.3\text{ V}$		12		
		$V_{out} = 5.0\text{ V}$		10		
Load transient voltage deviation, Load step 25-75-25% of max I_o , note 3	$di/dt=2\text{ A}/\mu\text{s}$, $C_{out} = 5 \times 100\text{ }\mu\text{F}$ ceramic + $4 \times 470\text{ }\mu\text{F}$ POSCAP	$V_{out} = 0.6\text{ V}$		110		mV
		$V_{out} = 1.0\text{ V}$		110		
		$V_{out} = 1.8\text{ V}$		210		
		$V_{out} = 2.5\text{ V}$		270		
		$V_{out} = 3.3\text{ V}$		270		
		$V_{out} = 5.0\text{ V}$		180		
Load transient recovery time, Load step 25-75-25% of max I_o , note 3	$di/dt=2\text{ A}/\mu\text{s}$, $C_{out} = 5 \times 100\text{ }\mu\text{F}$ ceramic + $4 \times 470\text{ }\mu\text{F}$ POSCAP	$V_{out} = 0.6\text{ V}$		400		μs
		$V_{out} = 1.0\text{ V}$		400		
		$V_{out} = 1.8\text{ V}$		400		
		$V_{out} = 2.5\text{ V}$		400		
		$V_{out} = 3.3\text{ V}$		400		
		$V_{out} = 5.0\text{ V}$		400		

Electrical specifications for BMR4732001

Characteristic	descriptions	conditions	min	typical	max	unit
Output current		$0.6\text{ V} \leq V_{\text{out}} \leq 1.8\text{ V}$	0		40	A
		$1.8\text{ V} < V_{\text{out}} \leq 3.3\text{ V}$	0		30	A
		$3.3\text{ V} < V_{\text{out}} \leq 5.0\text{ V}$	0		20	A
Output current limit		$0.6\text{ V} \leq V_{\text{out}} \leq 1.8\text{ V}$		52		A
		$1.8\text{ V} < V_{\text{out}} \leq 3.3\text{ V}$		39		A
		$3.3\text{ V} < V_{\text{out}} \leq 5.0\text{ V}$		26		A
Short circuit current	Hiccup mode, RMS value	$V_{\text{out}} = 0.6\text{ V}$		9.3		A
		$V_{\text{out}} = 1.0\text{ V}$		7.4		A
		$V_{\text{out}} = 1.8\text{ V}$		6.4		A
		$V_{\text{out}} = 2.5\text{ V}$		3.3		A
		$V_{\text{out}} = 3.3\text{ V}$		3.2		A
		$V_{\text{out}} = 5.0\text{ V}$		1.6		A
Efficiency (η)	50% of max I_{out}	$V_{\text{out}} = 0.6\text{ V}$		85.4		%
		$V_{\text{out}} = 1.0\text{ V}$		89.9		%
		$V_{\text{out}} = 1.8\text{ V}$		93.0		%
		$V_{\text{out}} = 2.5\text{ V}$		94.0		%
		$V_{\text{out}} = 3.3\text{ V}$		94.7		%
		$V_{\text{out}} = 5.0\text{ V}$		94.6		%
	100% of max I_{out}	$V_{\text{out}} = 0.6\text{ V}$		81.0		%
		$V_{\text{out}} = 1.0\text{ V}$		86.6		%
		$V_{\text{out}} = 1.8\text{ V}$		90.7		%
		$V_{\text{out}} = 2.5\text{ V}$		93.4		%
		$V_{\text{out}} = 3.3\text{ V}$		94.2		%
		$V_{\text{out}} = 5.0\text{ V}$		95.6		%
Power dissipation	at max I_{out}	$V_{\text{out}} = 0.6\text{ V}$		5.7	8.5	W
		$V_{\text{out}} = 1.0\text{ V}$		6.2	9	W
		$V_{\text{out}} = 1.8\text{ V}$		7.4	10	W
		$V_{\text{out}} = 2.5\text{ V}$		5.3	8	W
		$V_{\text{out}} = 3.3\text{ V}$		6.1	8	W
		$V_{\text{out}} = 5.0\text{ V}$		4.6	7	W
Internal output capacitance				350		μF
Recommended external output ceramic capacitance		$0.6\text{ V} \leq V_{\text{out}} \leq 5.0\text{ V}$	500			μF
Recommended external output bulk capacitance, note 4		$0.6\text{ V} \leq V_{\text{out}} \leq 5.0\text{ V}$	470	2380	10000	μF

Electrical specifications for BMR4732001

Characteristic	descriptions	conditions	min	typical	max	unit
Protection characteristics						
Input turn on voltage	Default value	$0.6\text{ V} \leq V_{out} \leq 3.3\text{ V}$		5.5		V
		$3.3\text{ V} < V_{out} \leq 5.0\text{ V}$		6.5		V
	PMBus configurable range		5.5		15	V
	Resolution			0.25		V
Input Under Voltage Lockout, UVLO	Default value	$0.6\text{ V} \leq V_{out} \leq 3.3\text{ V}$		4.5		V
		$3.3\text{ V} < V_{out} \leq 5.0\text{ V}$		5.5		V
	PMBus configurable range		4.5		15	V
	Resolution			0.25		V
Input Over Voltage Protection, IOVP	Default value			16		V
	PMBus configurable range		6		16	V
	Resolution			1		V
	Response delay			0		µs
	Fault response		Automatic restart, 70ms			
Output Over Voltage Protection, OVP	Default value			115		%
	PMBus configurable range		105		140	%
	Resolution			2.5		%
	Fault response		Automatic restart, 70ms			
Output Under Voltage Protection, UVP	Default value			85		%
	PMBus configurable range		60		95	%
	Resolution			2.5		%
	Response delay time			0		µs
	Fault response		Automatic restart, 70ms			
Over Current Protection, OCP	Default value			52		A
	PMBus configurable range		8		52	A
	Resolution			2		A
	Response delay time		7 PWM cycles			
	Fault response		Automatic restart, 70ms			
Over Temperature Protection, OTP, note 5	Default value			135		°C
	PMBus configurable range		0		150	°C
	Resolution			1		°C
	Response delay time			0		µs
	Fault response		Automatic restart, 70ms			

Electrical specifications for BMR4732001

Characteristic	descriptions	conditions	min	typical	max	unit
Other characteristics						
Switching frequency (f _s)	Default value			450		kHz
	PMBus configurable range, note 6		450		900	kHz
	Set-point Accuracy		-10		10	%
Frequency synchronization, SYNC	SYNC output duty cycle			50		%
	SYNC input minimum pulse width				200	ns
	Allowable SYNC pin frequency difference from FREQUENCY_SWITCH frequency		-20		20	%
Initialization time				10		ms
Output voltage turn on delay time	Default value			10		ms
	PMBus configurable range (TON_DELAY)		0		127.5	ms
	Resolution			0.5		ms
	Accuracy		-10		15	%
Output voltage turn on ramp up time (0-100% of V _o)	Default value			10		ms
	PMBus configurable range (TON_RISE), note 7		0		31.75	ms
	Resolution			0.25		ms
	Accuracy		-10		15	%
Output voltage turn off delay time	Default value			0		ms
	PMBus configurable range (TOFF_DELAY), note 7		0		127.5	ms
	Resolution			0.5		ms
	Accuracy		-10		15	%
Output voltage turn off fall time (100-0% of V _o)	Default value		Disabled, turn off immediately upon expiration of Turn off delay			
	PMBus configurable range (TOFF_FALL)		0		31.75	ms
	Resolution			0.25		ms
	Accuracy		-10		15	%
Power Good, PG	PG assertion threshold on V _o rising			95		% V _o
	PG de-assertion threshold on V _o falling			95		% V _o

Electrical specifications for BMR4732001

Characteristic	descriptions	conditions	min	typical	max	unit
Monitoring accuracy	Input voltage, READ_VIN		-3		3	%
	Output voltage, READ_VOUT		-2		2	%
	Output current, READ_IOUT		-5		5	A
	Temperature, READ_TEMPERATURE1		-3		3	°C
Logic output low level	SCL, SDA, SALERT, SYNC, PG, BCX_DAT, BCX_CLK			0.4	V	
Logic output high level		2.25		V		
Logic input low level	SCL, SDA, SYNC, CTRL			0.8	V	
Logic input high level		1.35		V		
Logic pin internal capacitance	PG			100	pF	
Logic pin internal pull up resistance	PG to 5V, CTRL to 5V			10	kΩ	
Supported PMBus operating frequency range			10		1000	kHz
SMBus Bus free time			0.5			μs
SMBus SDA setup time from SCL			0.26			μs
SMBus SDA hold time from SCL			0			μs
SMBus START/STOP condition setup/hold time			0.26			μs
SCL low period			0.5			μs
SCL high period			0.26			μs

Note 1: See section "Input capacitors" in "Design & Application Guide".

Note 2: See graph "Output ripple and noise".

Note 3: See graph "Transient response".

Note 4: See section "Output capacitors" in "Design & Application Guide".

Note 5: Temperature of T_{p1}, see section "Definition of product operating temperature".

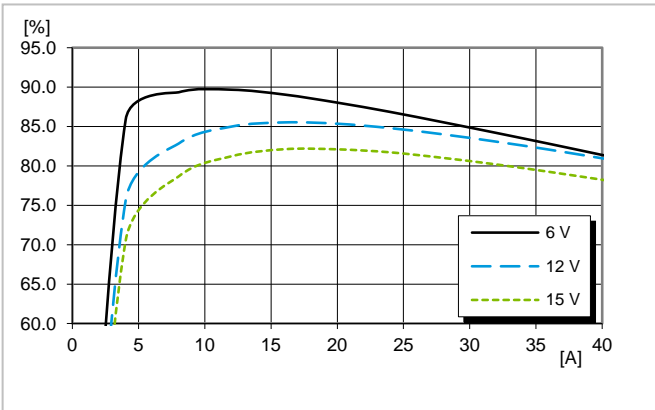
Note 6: Effective switching frequency listed in section "Switching frequency" in "Design & Application Guide".

Note 7: Values less than 0.5ms are supported as 0.5ms.

Electrical graphs for BMR4732001

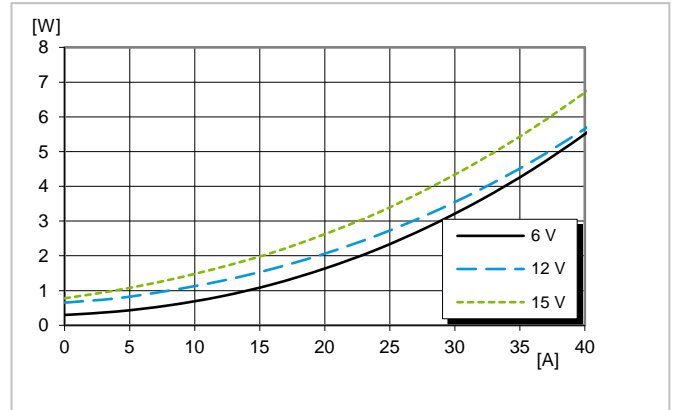
$V_{out} = 0.6 V$

Efficiency



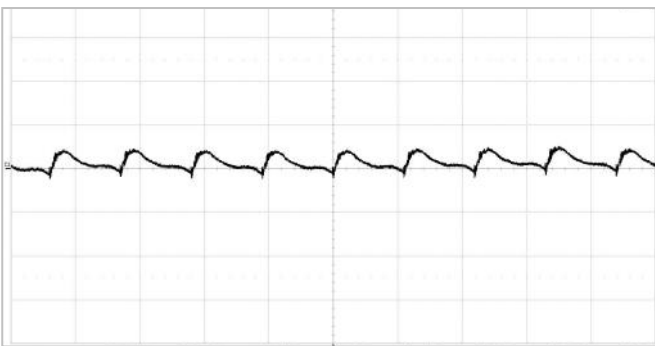
Efficiency vs. output current at $T_{PI} = +25^{\circ}C$

Power dissipation



Dissipated power vs. load current at $T_{PI} = +25^{\circ}C$

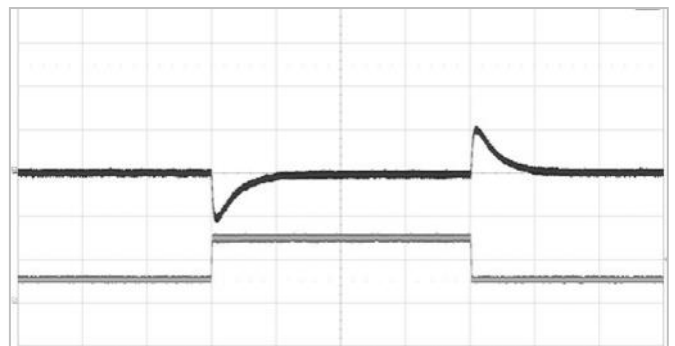
Output ripple and noise



Output voltage ripple at $V_I=12V, I_o=\max I_o, T_{PI} = +25^{\circ}C$

Scale: 5 mV/div, 2 μ s/div, 20MHz bandwidth

Transient response



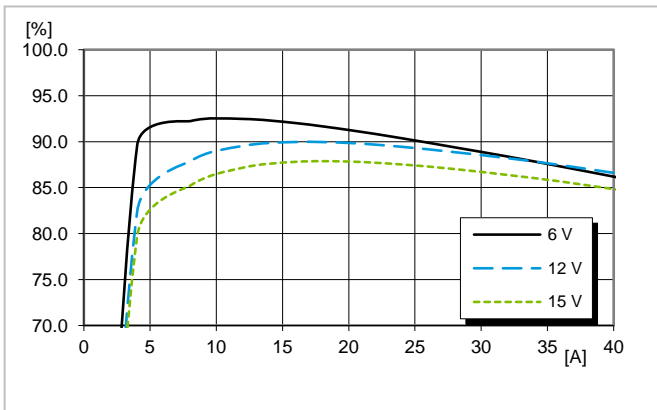
Output voltage response to output current change (10-30-10 A) at $V_I=12V, C_O=5 \times 100 \mu F$ ceramic + $4 \times 470 \mu F$ POSCAP, $T_{PI} = +25^{\circ}C, di/dt=2A/\mu s$.

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500 μ s/div

Electrical graphs for BMR4732001

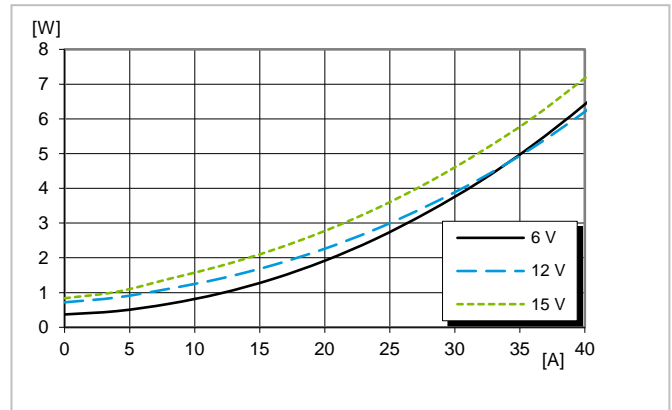
V_{out} = 1.0 V

Efficiency



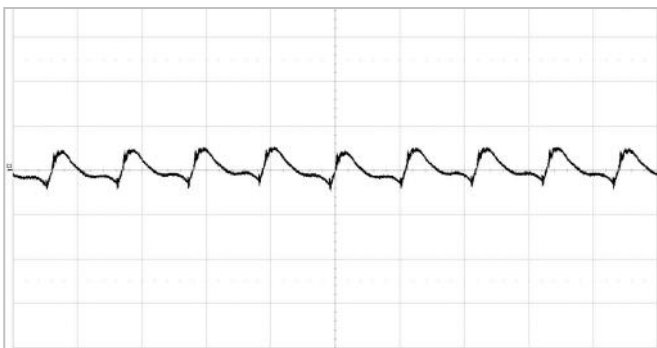
Efficiency vs. output power and input voltage at $T_{P1} = +25^{\circ}\text{C}$

Power dissipation



Dissipated power vs. load power at $T_{P1} = +25^{\circ}\text{C}$

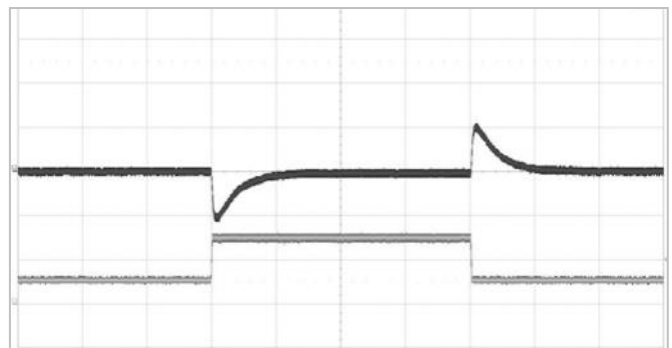
Output ripple and noise



Output voltage ripple at $V_I=12\text{V}$, $I_o=\text{max } I_o$, $T_{P1} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2 µs/div, 20MHz bandwidth

Transient response



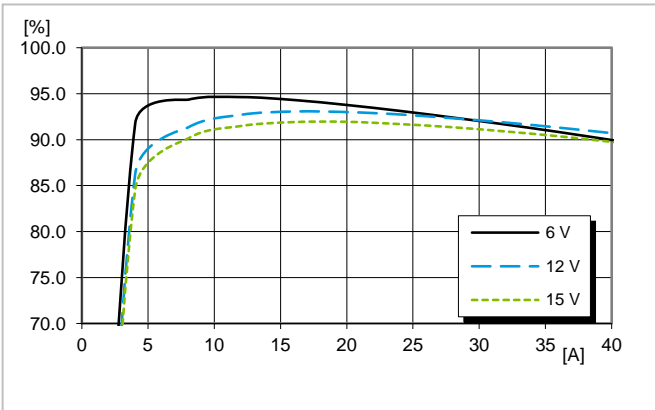
Output voltage response to output current change (10-30-10 A) at $V_I=12\text{V}$, $C_O=5 \times 100 \mu\text{F}$ ceramic + $4 \times 470 \mu\text{F}$ POSCAP, $T_{P1} = +25^{\circ}\text{C}$, $di/dt=2\text{A}/\mu\text{s}$.

Top trace: output voltage (100mV/div), bottom trace: load current (20A/div), time scale: 500 µs/div

Electrical graphs for BMR4732001

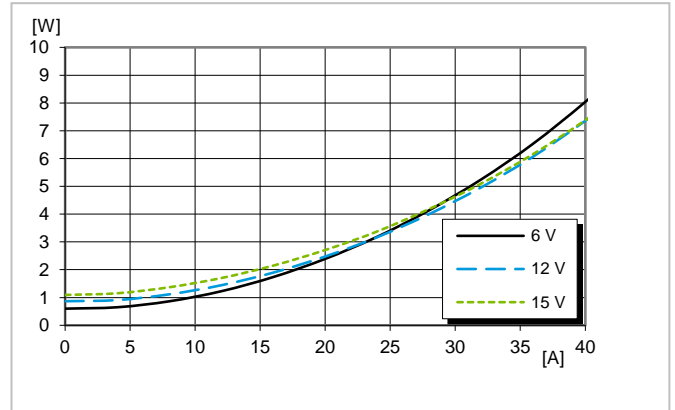
V_{out} = 1.8 V

Efficiency



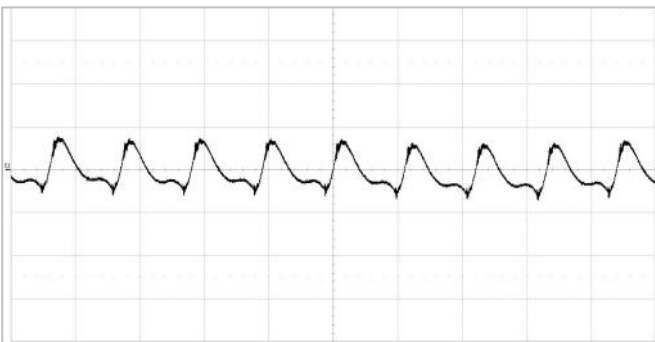
Efficiency vs. output power and input voltage at T_{P1} = +25°C

Power dissipation



Dissipated power vs. load power at T_{P1} = +25°C

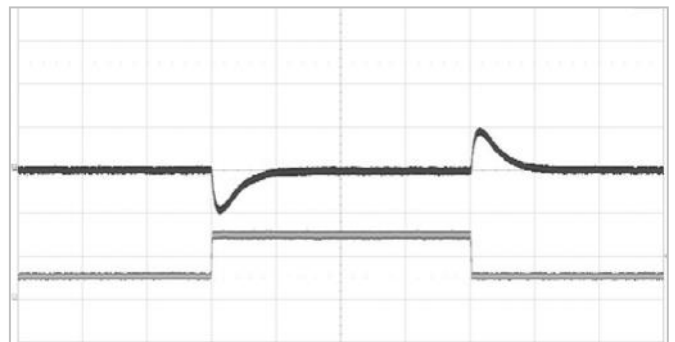
Output ripple and noise



Output voltage ripple at V_i=12V, I_o=max I_o, T_{P1} = +25°C

Scale: 5 mV/div, 2 μs/div, 20MHz bandwidth

Transient response



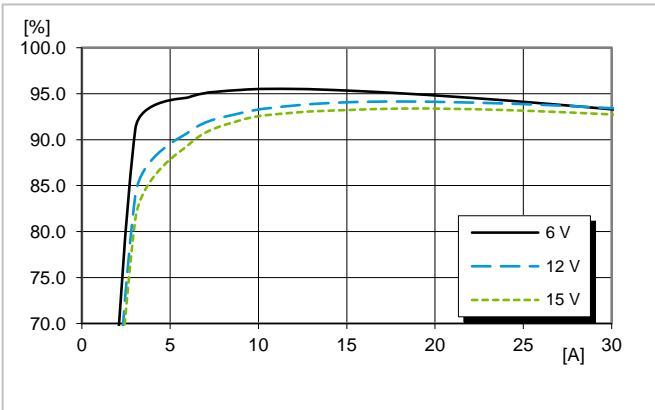
Output voltage response to output current change (10-30-10 A) at V_i=12V, C_O=5 x 100 μF ceramic + 4 x 470 μF POSCAP, T_{P1} = +25°C, di/dt=2A/μs.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 μs/div

Electrical graphs for BMR4732001

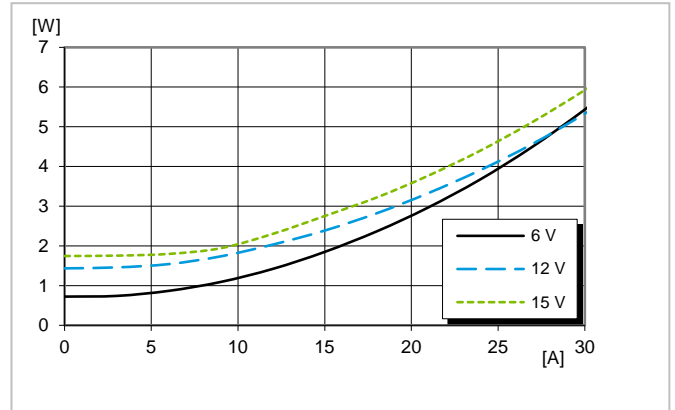
V_{out} = 2.5 V

Efficiency



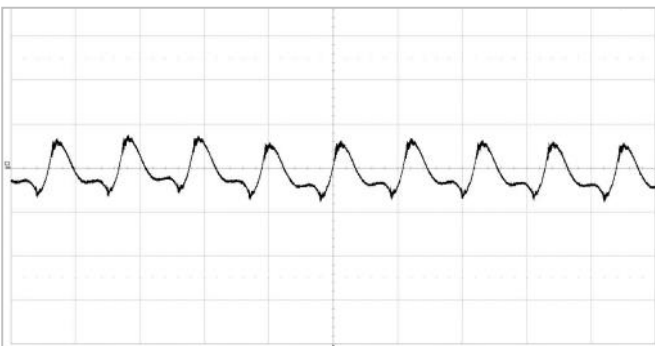
Efficiency vs. output power and input voltage at $T_{P1} = +25^{\circ}\text{C}$

Power dissipation



Dissipated power vs. load power at $T_{P1} = +25^{\circ}\text{C}$

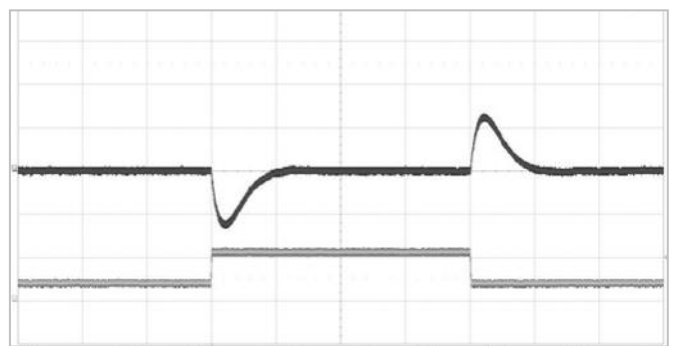
Output ripple and noise



Output voltage ripple at $V_I=12\text{V}$, $I_o=\text{max } I_o$, $T_{P1} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2 μs /div, 20MHz bandwidth

Transient response



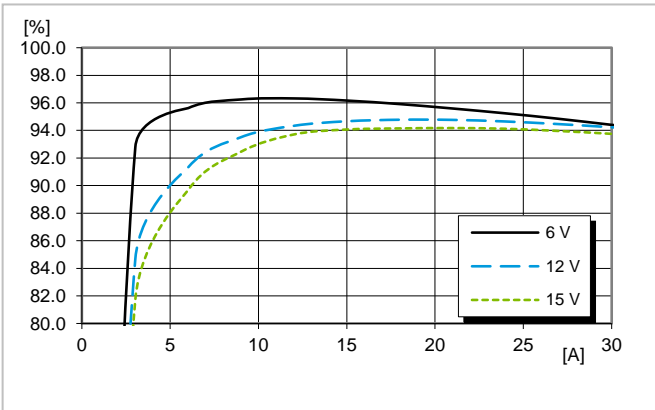
Output voltage response to output current change (7.5-22.5-7.5 A) at $V_I=12\text{V}$, $C_o=5 \times 100 \mu\text{F}$ ceramic + 4 \times 470 μF POSCAP, $T_{P1} = +25^{\circ}\text{C}$, $di/dt=2\text{A}/\mu\text{s}$.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 μs /div

Electrical graphs for BMR4732001

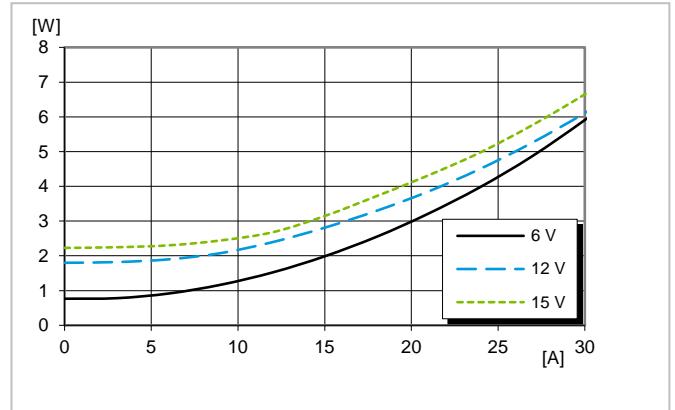
V_{out} = 3.3 V

Efficiency



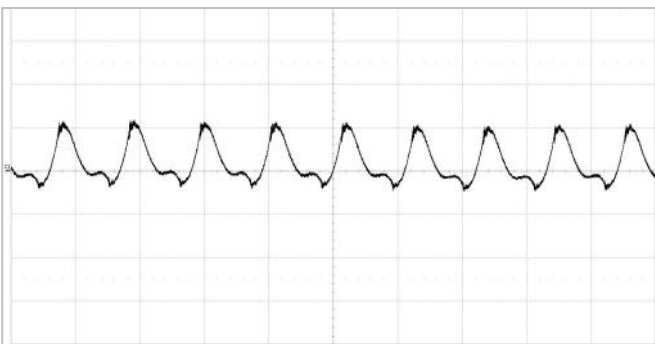
Efficiency vs. output power and input voltage at $T_{P1} = +25^{\circ}\text{C}$

Power dissipation



Dissipated power vs. load power at $T_{P1} = +25^{\circ}\text{C}$

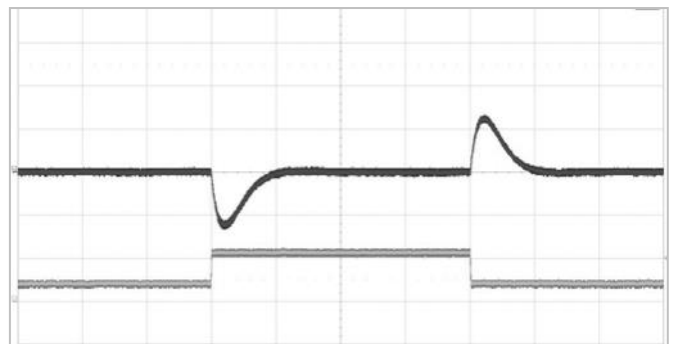
Output ripple and noise



Output voltage ripple at $V_i=12\text{V}$, $I_o=\text{max } I_o$, $T_{P1} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2 μs /div, 20MHz bandwidth

Transient response



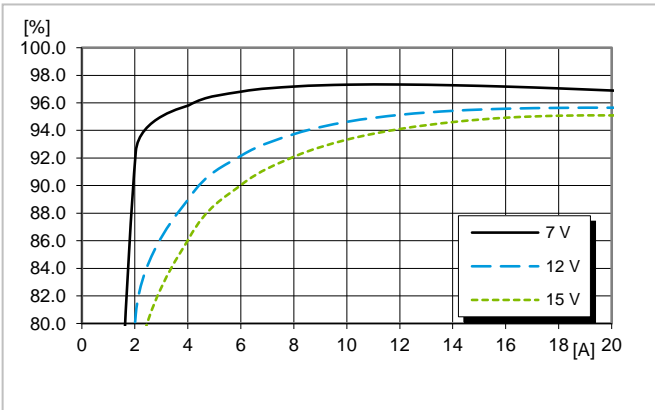
Output voltage response to output current change (7.5-22.5-7.5 A) at $V_i=12\text{V}$, $C_o=5 \times 100 \mu\text{F}$ ceramic + 4 x 470 μF POSCAP, $T_{P1} = +25^{\circ}\text{C}$, $di/dt=2\text{A}/\mu\text{s}$.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 μs /div

Electrical graphs for BMR4732001

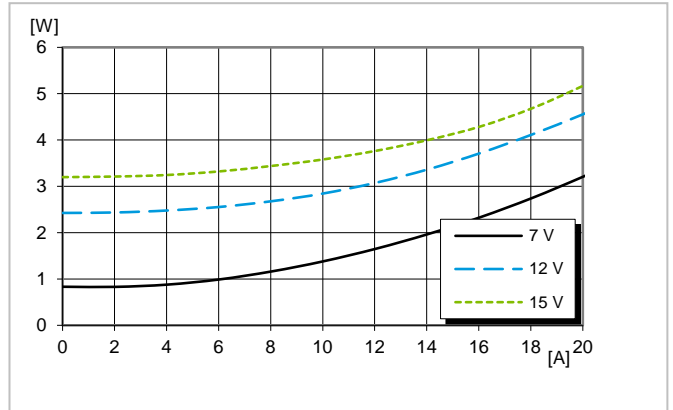
V_{out} = 5.0 V

Efficiency



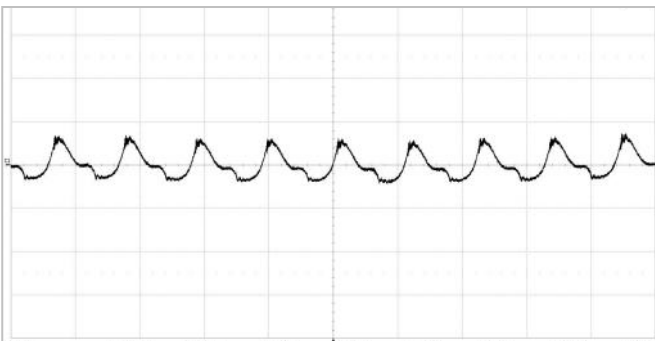
Efficiency vs. output power and input voltage at $T_{PI} = +25^{\circ}\text{C}$

Power dissipation



Dissipated power vs. load power at $T_{PI} = +25^{\circ}\text{C}$

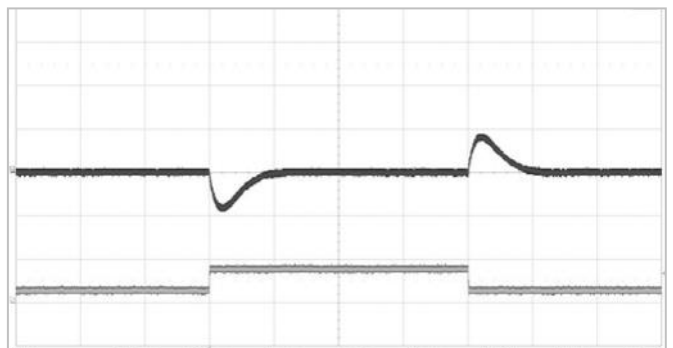
Output ripple and noise



Output voltage ripple at $V_I=12\text{V}$, $I_o=\text{max } I_o$, $T_{PI} = +25^{\circ}\text{C}$

Scale: 5 mV/div, 2 μs/div, 20MHz bandwidth

Transient response



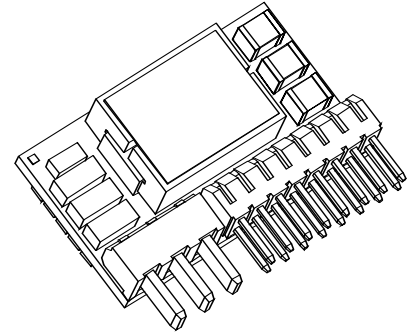
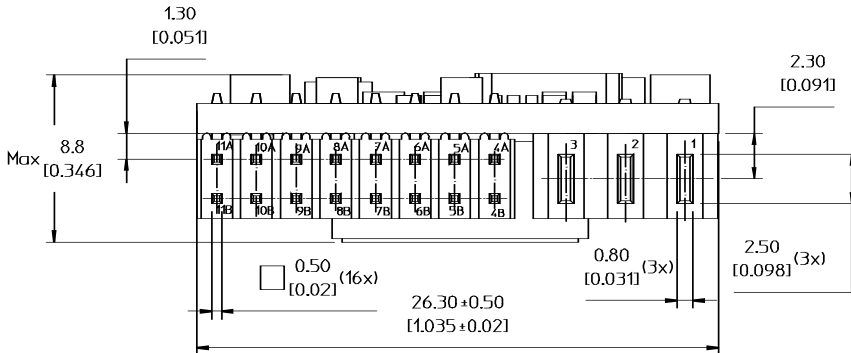
Output voltage response to output current change (5-15-5 A) at $V_I=12\text{V}$, $C_o=5 \times 100 \mu\text{F ceramic} + 4 \times 470 \mu\text{F POSCAP}$, $T_{PI} = +25^{\circ}\text{C}$, $di/dt=2\text{A}/\mu\text{s}$.

Top trace: output voltage (200mV/div), bottom trace: load current (20A/div), time scale: 500 μs/div

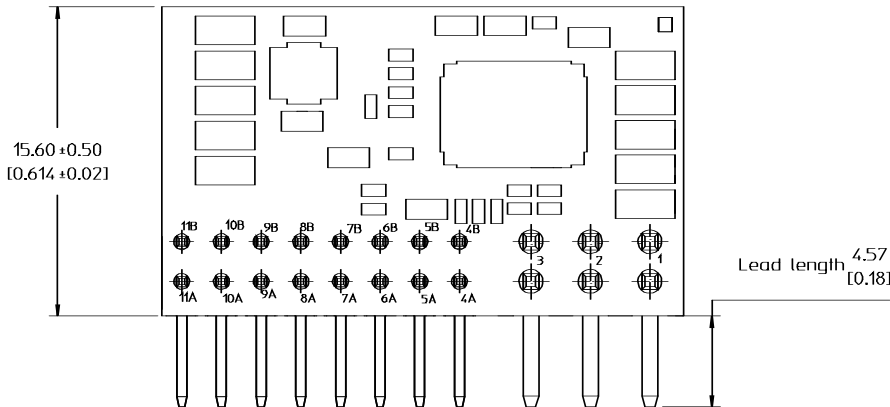
Part 2: Mechanical information
BMR473: hole mounted, SIP version

BOTTOM VIEW

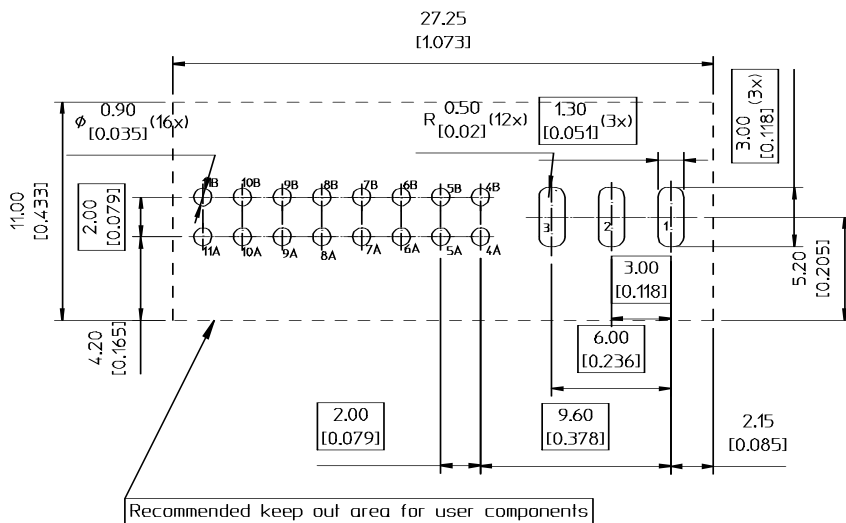
Pin positions according to recommended footprint



FRONT VIEW



RECOMMENDED FOOTPRINT - TOP VIEW



PIN SPECIFICATIONS

Pin 1-3 Material: Copper alloy (C11000)
Plating: Min Au 0.1 µm over 1-3 µm Ni.
Pin 4A-11B Material: Copper alloy
Plating: Min Au 0.1 µm over 1 µm Ni.

Weight: Typical 8.5 g

All dimensions in mm [inch]

Tolerances unless specified:

x.x ±0.50 [0.02]

x.xx ±0.25 [0.01]

(not applied on footprint or typical values)

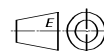
Weight: (insert max, typical or range) g

All dimensions in mm [inch].

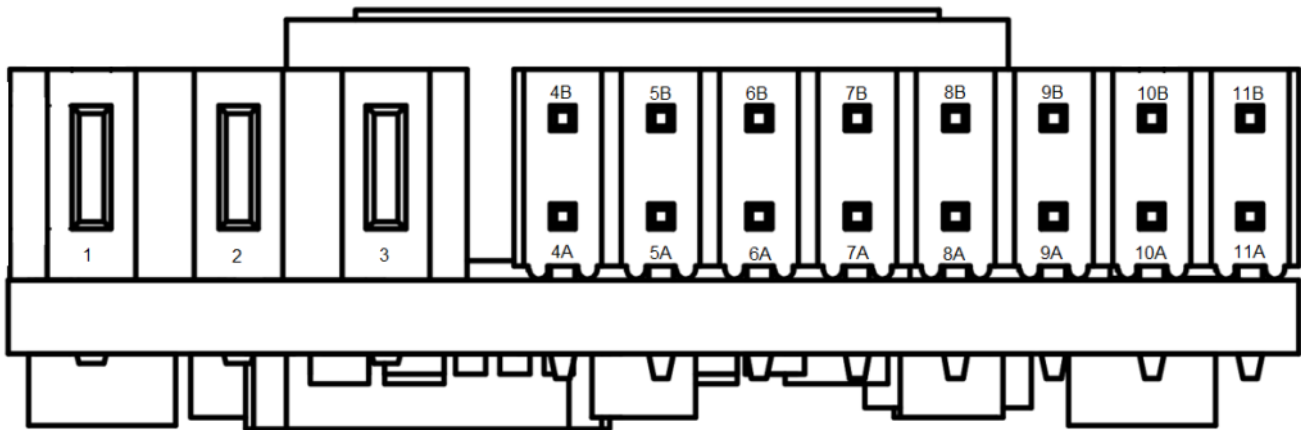
Tolerances unless specified

x.x mm ±0.50 mm [0.02], x.xx mm ±0.25 mm [0.01]

(not applied on footprint or typical values)



Connections



Pin layout, bottom view

Pin	Designation	Type	Function
1	VIN	Power	Input voltage
2	GND	Power	Power ground
3	VOUT	Power	Output voltage
4A	SALERT	O, Open drain	PMBus Alert
4B	SCL	I/O	PMBus Clock
5A	SDA	I/O	PMBus Data
5B	PG	O, Open drain	PowerGood output
6A	BCX_DAT	I/O	Back-channel communications data
6B	BCX_CLK	I/O	Back-channel communications clock
7A	SYNC	I/O	Switching frequency synchronization
7B	VCC1V5	Power	Reference voltage for pin strapping
8A	AGND	Power	Ground reference for pin strapping
8B	VSHARE	I/O	Voltage sharing for paralleling
9A	VSET	I	Output voltage pin strap
9B	ADDR	I	PMBus address pin strap
10A	+S	I	Positive sense
10B	MSEL	I	Pin strap for soft-start time, over current fault limit and paralleling.
11A	-S	I	Negative sense
11B	CTRL	I	Remote Control

Part 3: Thermal considerations

Thermal considerations

The products are designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.

General for SIP version

Cooling is mainly achieved by conduction from the pins to the host board and convection which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The products comes in a vertical SIP as well as horizontally mounted laydown version. For products mounted on a PWB without a heatsink attached, cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product. The wind speed and temperature are measured in a point upstream of the device. Distances between the tested device and the top space board and the side airflow guides are $6.35 \text{ mm} \pm 1 \text{ mm}$.

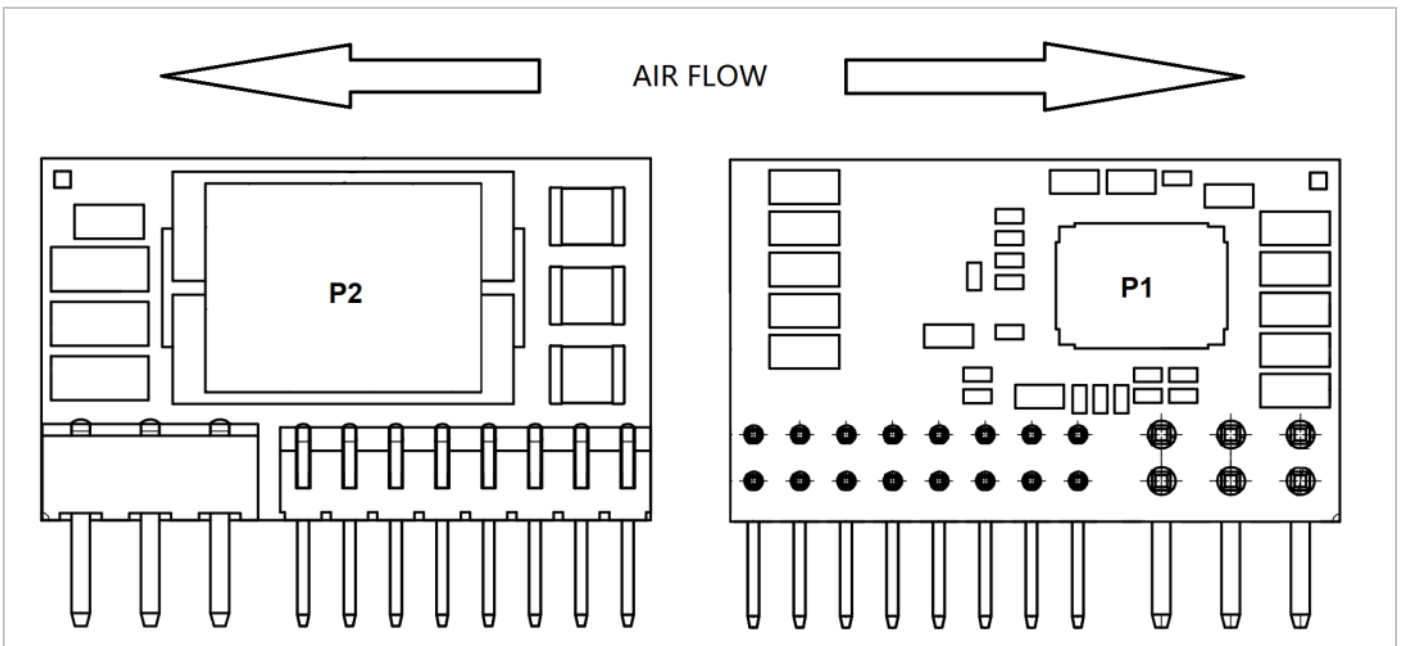
The product is tested on a $254 \times 254 \text{ mm}$, $35 \mu\text{m}$ (1 oz), 8 layer test board mounted vertically in a wind tunnel with a cross section of $608 \times 203 \text{ mm}$.

The [output current derating graphs](#) found later in this section for each model provide the available output current vs. ambient air temperature and air velocity at $V_{in} = 12 \text{ V}$.

Definition of product operating temperature

Proper thermal conditions can be verified by measuring the temperature at position P1 as shown below. The temperature at this position (T_{P1}) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum T_{P1} , measured at the reference point P1 are not allowed and may cause permanent damage.

SIP MOUNTING		
Position	Description	Max. Temp.
P1	Controller	$T_{P1} = 125 \text{ }^\circ\text{C}$
P2	Inductor	$T_{P2} = 120 \text{ }^\circ\text{C}$

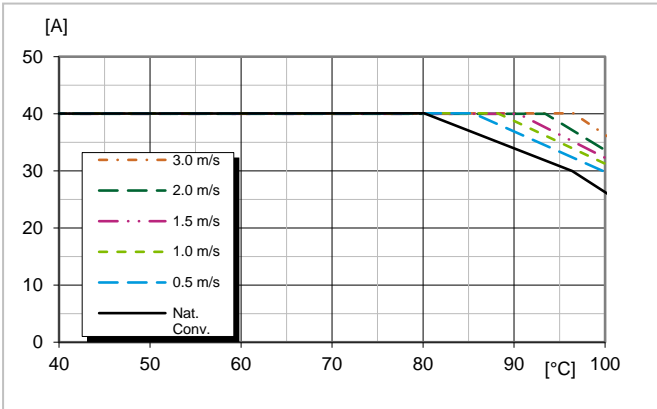
Temperature position and air flow direction

Temperature position and air flow direction, SIP

Thermal graphs

$V_{out} = 0.6\text{ V}$

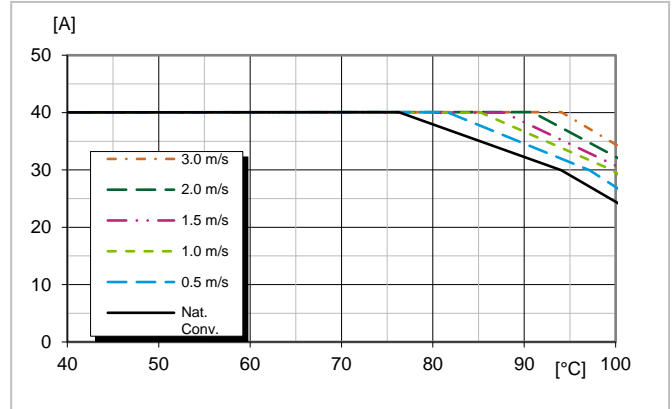
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, $V_i = 12\text{ V}$, $V_o = 0.6\text{ V}$.

$V_{out} = 1.0\text{ V}$

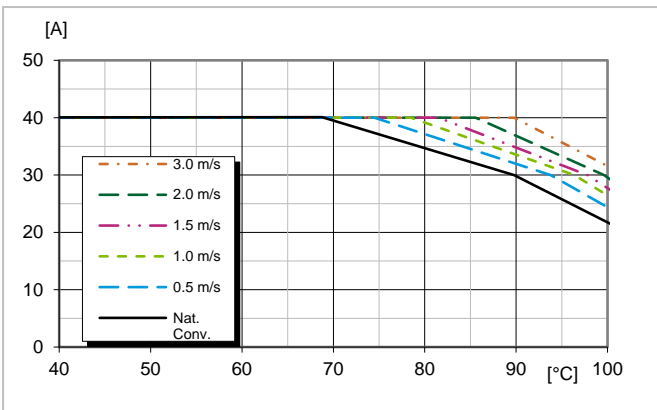
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, $V_i = 12\text{ V}$, $V_o = 1.0\text{ V}$.

$V_{out} = 1.8\text{ V}$

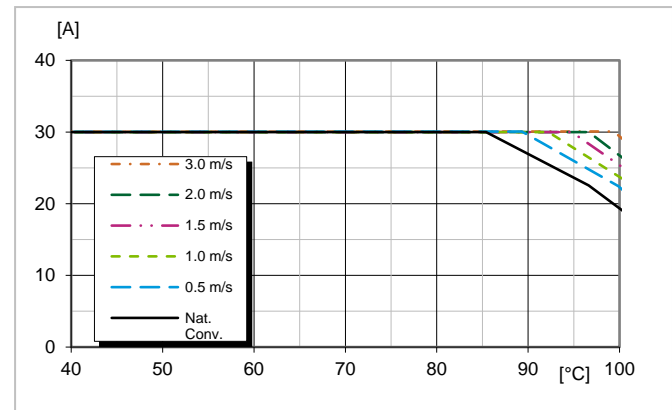
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, $V_i = 12\text{ V}$, $V_o = 1.8\text{ V}$.

$V_{out} = 2.5\text{ V}$

Output current derating - open frame

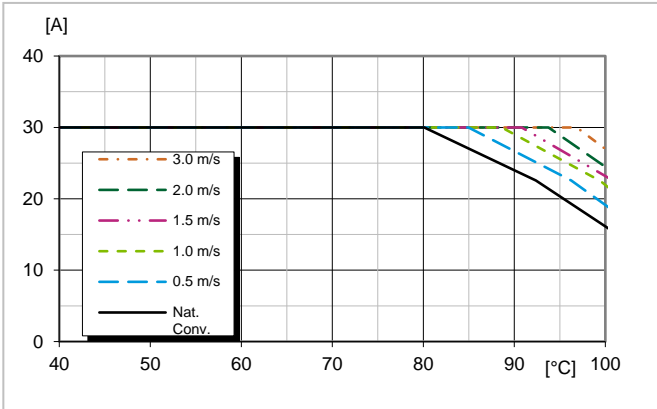


Available output current vs. ambient air temperature and airflow, $V_i = 12\text{ V}$, $V_o = 2.5\text{ V}$.

Thermal graphs

$V_{out} = 3.3\text{ V}$

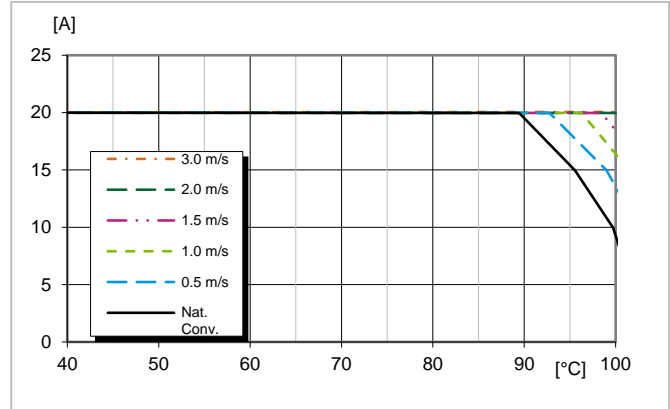
Output current derating - open frame



Available output current vs. ambient air temperature and airflow, $V_I = 12\text{V}$, $V_O = 3.32\text{V}$.

$V_{out} = 5.0\text{ V}$

Output current derating - open frame



Available output current vs. ambient air temperature and airflow, $V_I = 12\text{V}$, $V_O = 5.0\text{V}$.

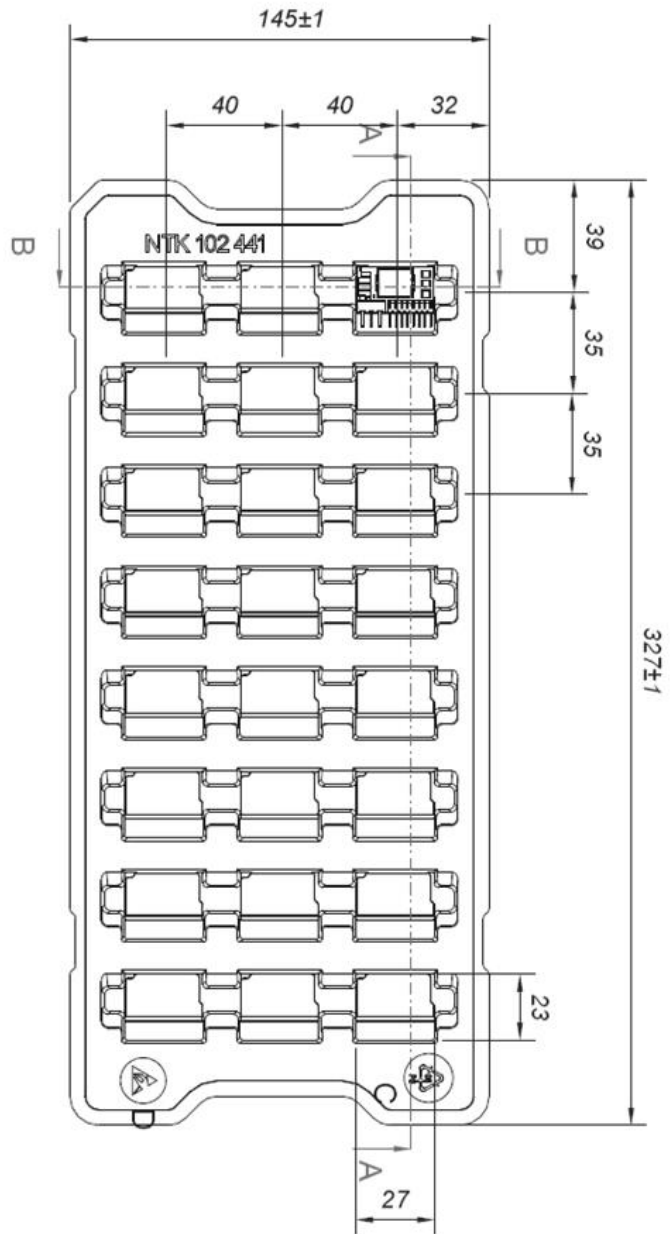
Part 4: Packaging
Packaging information

B option:	
Material	Antistatic Polystyrene (black)
Surface resistance	$10^5 < \text{ohm/square} < 10^{11}$
Bakability	Trays are not bakeable
Tray thickness	20 mm (0.787 in) for SIP version
Box capacity	240 products (10 full trays/box)
Tray weight	47g empty tray, 255g full tray (SIP version)

All dimensions in mm [inch]

Tolerances: X.x ±0.26 [0.01], X.xx ±0.13 [0.005]

Note: The tray is not designed for machine pick up



Part 5: Revision history

Revision table

Revision number	revision change	date	revisor
Rev. A	First release edition.	2022-07-04	JIDMWANG

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