TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

INPUT AND OUTPUT-RELATED GUIDELINES:

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors. If the input voltage source contains significant inductance, the addition a capacitor with low ESR at the input of the product will ensure stable operation.

Input capacitors

The input ripple RMS current in a buck converter is equal to

Eq.1 $I_{inputRMS} = I_{load} \sqrt{(D(1-D))}$

where I_{load} is the output load current and D is the duty cycle.

The maximum load ripple current becomes $I_{load}/2$. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor, and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors. A minimum capacitance of 470 µF with low ESR is recommended. The ripple current rating of the capacitors must follow Eq. 1. For high-performance/transient applications or wherever the input source performance is degraded, additional low ESR ceramic type capacitors at the input is recommended. The additional input low ESR capacitance above the minimum level insures an optimized performance.

Output capacitors

When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load. The most effective technique is to place low ESR ceramic and electrolytic capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. Ceramic capacitors will also reduce high frequency noise at the load. It is equally important to use low resistance and low inductance PWB layouts and cabling. External decoupling capacitors are a part of the control loop of the product and may affect the stability margins. Stable operation is guaranteed for the following total capacitance Co in the output decoupling capacitor bank where

Eq. 2. $C_o = [C_{min}, C_{max}] = [470, 10000]$ µF

The decoupling capacitor bank should consist of capacitors which has a capacitance value larger than $C \geq C_{min}$ and has an ESR range of

Eq. 3. ESR = [ESRmin, ESRmax] = [1,10] mΩ

The control loop stability margins are limited by the minimum time constant min τ_{min} of the capacitors. Hence, the time constant of the capacitors should follow

Eq. 4. $\tau \geq \tau_{min} = C_{min}\, ESR_{min} = 0.47$ µs

If the capacitors capacitance value is $C < C_{min}$ one must use at least N capacitors where

$N \geq \lceil C_{min}/C \rceil$ and $ESR \geq ESR_{min}(C_{min}/C)$

If the ESR value is $ESR > ESR_{max}$ one must use at least *N* capacitors of that type where

$N \geq \lceil ESR/ESR_{max} \rceil$ and $C \geq C_{min}/N$

If the ESR value is $ESR < ESR_{min}$ the capacitance value should be

$C \geq C_{min}(ESR_{min}/ESR)$

For a total capacitance outside the above stated range or capacitors that do not follow the stated above requirements above a re-design of the control loop parameters will be necessary for robust dynamic operation and stability. See technical paper TP022 for further information.

Control loop

The products use a average current-mode synchronous buck controller with a fixed frequency PWM scheme. Although the product uses a digital control loop, it operates much like a traditional analog PWM controller. The block diagram of the control loop is shown below.

The current error integrator adjusts the modulator control voltage to match the sensed inductor current, I_SNS, to the current voltage at the VSHARE pin. The integrator is tuned through the GMI, RVI, CZI, CPI, and CZI_MUL parameters. The bandwidth of the current control loop can be adjusted with the mid-band gain of the integrator, GMI × RVI. The low-frequency zero, RVI × CZI, compensates for the valley voltage of the modulator ramp and the nominal offset of the output voltage, and should be set below voltage loop cross -over frequency. The high-frequency pole, RVI × CPI, reduces high-frequency noise from VSHARE and minimizes pulse-width jitter, and should be set between half of the switching frequency (fsw/2) and the switching frequency (fsw).

The voltage error integrator regulates the output voltage by adjusting the current control voltage, VSHARE, similar to any current mode control architecture. The integrator is tuned through the GMV, RVV, CZV and CPV parameters. The bandwidth of the voltage control loop can be adjusted with the mid-band gain of the integrator, GMV × RVV. The output feedback divider ratio also contributes to the mid-band gain. The zero-frequency, RVV × CZV, should be set below the lowest cross-over frequency with largest output capacitor. The high-frequency pole, RVV × CPV, keeps switching noise out of the current loop and should be set between fsw/4 and fsw.

The characteristics of the control loop is configured by setting these compensation parameters. These settings can be reconfigured using the PMBus command USER_DATA_01 (COMPENSATION_CONFIG)(0xB1).

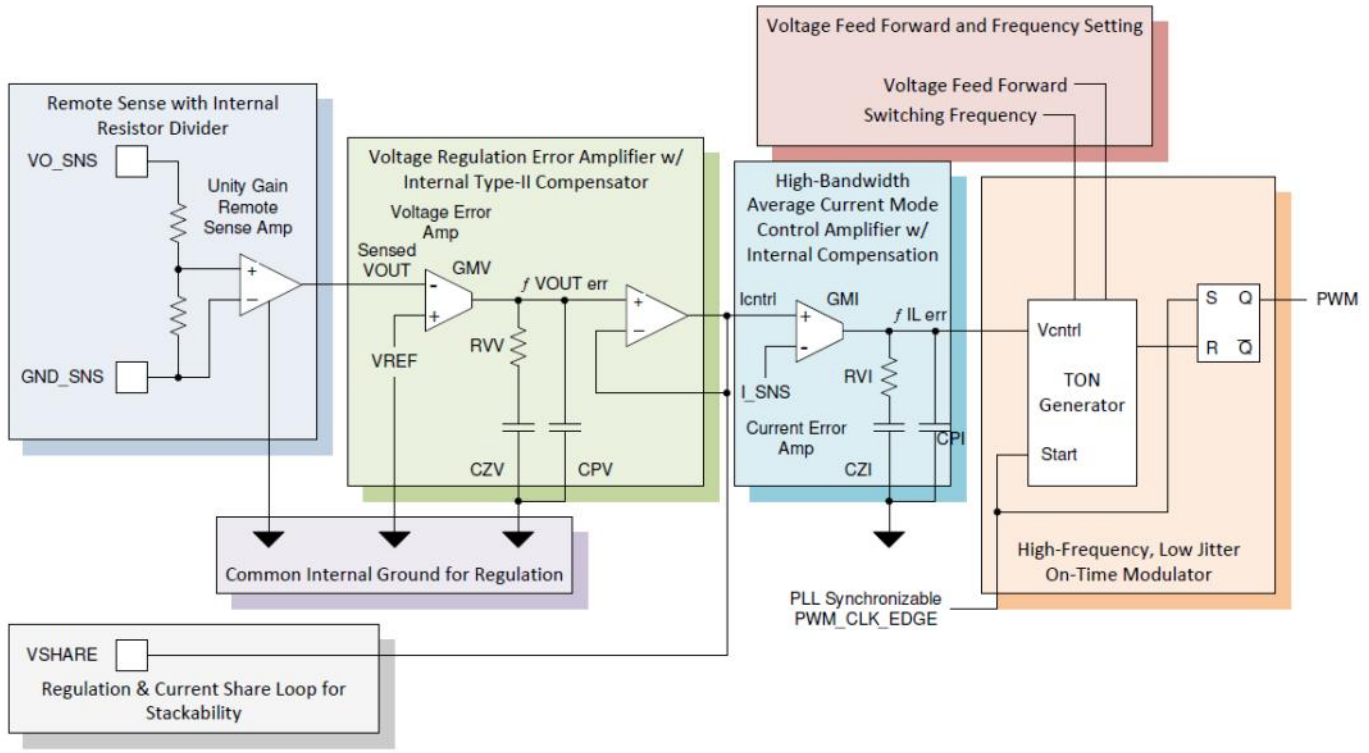


Figure 1: The block diagram of the control loop

PROTECTION FEATURES:

Input Under Voltage Lockout (UVLO)

The product monitors the input voltage and will turn-on and turn-off at configured levels. The default turn-on input voltage level setting is 5.5 V, whereas the corresponding turn-off input voltage level is 4.5V. Hence, the default hysteresis between turn-on and turn-off input voltage is 1 V. The default response from input-turn -off condition is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the product will be re-enabled. The turn-on and turn-off levels and response can be reconfigured using the PMBus interface.

Input Over Voltage Protection (IOVP)

The product includes input over voltage limiting circuitry. The default OVP limit is 16V. The default response from an input-over-voltage fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the product will be re-enabled. The OVP limit and response can be reconfigured using the PMBus interface.

Output over voltage protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. The default response from an output-over-voltage fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the product will be re-enabled. The OVP limit and response can be reconfigured using the PMBus interface.

Output under voltage protection (UVP)

The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. The default response from an output-under-voltage fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the product will be re-enabled. The UVP limit can be reconfigured using the PMBus interface.

Over Current Protection (OCP)

The product includes robust current limiting circuitry for protection at continuous overload. The default OCP limit is 52A. The default response from an over-current fault is a delayed shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled. The load distribution should be designed lower than the specified maximum output current. The OCP limit is programmed by pin-strapping of MSEL pin. The OCP limit and response can also be reconfigured using the PMBus interface.

Under Current Protection (UCP)

The product includes robust current limiting circuitry for protection at 20A continuous reversed current.

Over temperature protection (OTP)

The products are protected from thermal overload by an internal over temperature shutdown function in the controller, located at position P1 (see section Thermal Consideration). The default OTP limit is 135 °C. The default response from an over-temperature fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled. The OTP limit and response can be reconfigured using the PMBus interface.

OPERATIONAL GUIDELINES

Remote control

The product is equipped with a remote control function, i.e., the CTRL pin. The remote control can be connected to the ground or left open or to an external voltage (Vext), which is a 3 - 5 V positive supply voltage in accordance to the SMBus Specification version 2.0.

The CTRL function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. By default the product will turn on when the CTRL pin is left open and turn off when the CTRL pin is applied to GND. The CTRL pin has an internal pull-up resistor to VDD5. When the CTRL pin is left open, the voltage generated on the CTRL pin is max 5.5 V. If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the CTRL pin.

The product can also be configured using the PMBus interface to be "Always on", or turn on/off can be performed with PMBus commands.

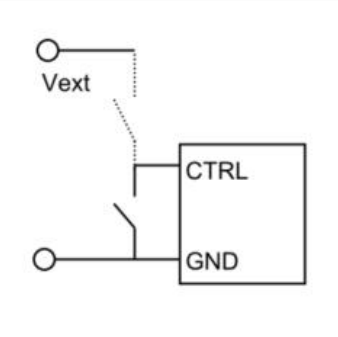


Figure 2: Remote Control

Output voltage adjust using pin-strap resistor (VSET pin)

Using an external voltage divider between VCC1V5 pin and AGND pin, Rtop and Rbot, the output voltage can be programmed according to the table in the next page. Maximum 1% tolerance resistors are required.
The resistor is sensed only during the initialization procedure after input voltage is applied. Changing the resistor value during normal operation will not change the output voltage.

The voltage divider also programs VOUT_SCALE_LOOP, VOUT_MIN and VOUT_MAX levels, see section "Output voltage range limitation".

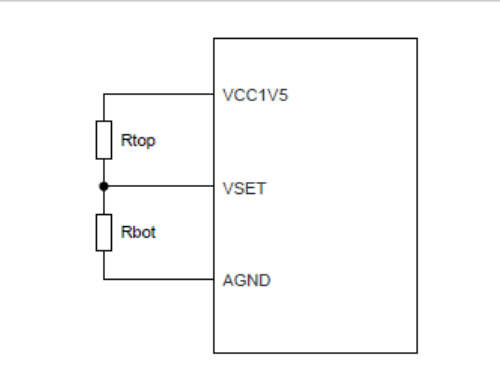


Figure 3: Pin-strap resistor for VSET pin

Output voltage adjust using pin-strap resistors—contd.

Rbot=4.64 kΩ		Rbot=5.62 kΩ		Rbot=6.81 kΩ		Rbot=8.25 kΩ		Rbot=10 kΩ		Rbot=12.1 kΩ		Rbot=14.7 kΩ		Rbot=17.8 kΩ	
Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)
				0.6	Open	0.65	Open	0.7	Open	0.75	Open	0.8	Open	0.85	Open
0.6	21.5	0.61	26.1	0.62	31.6	0.63	38.3	0.64	46.4	0.65	56.2	0.66	68.1	0.67	82.5
0.75	15.4	0.76	18.7	0.77	22.6	0.78	27.4	0.79	33.2	0.8	40.2	0.81	48.7	0.82	59
0.9	11.5	0.91	14	0.92	16.9	0.93	20.5	0.94	24.9	0.95	30.1	0.96	36.5	0.97	44.2
1.05	9.09	1.06	11	1.07	13.3	1.08	16.2	1.09	19.6	1.1	23.7	1.11	28.7	1.12	34.8
1.2	7.15	1.22	8.66	1.24	10.5	1.26	12.7	1.28	15.4	1.3	18.7	1.32	22.6	1.34	27.4
1.5	5.62	1.52	6.81	1.54	8.25	1.56	10	1.58	12.1	1.6	14.7	1.62	17.8	1.64	21.5
1.8	4.64	1.82	5.62	1.84	6.81	1.86	8.25	1.88	10	1.9	12.1	1.92	14.7	1.94	17.8
2.1	3.83	2.12	4.64	2.14	5.62	2.16	6.81	2.18	8.25	2.2	10	2.22	12.1	2.24	14.7
2.4	3.16	2.44	3.83	2.48	4.64	2.52	5.62	2.56	6.81	2.6	8.25	2.64	10	2.68	12.1
3	2.61	3.04	3.16	3.08	3.83	3.12	4.64	3.16	5.62	3.2	6.81	3.24	8.25	3.28	10
3.6	2.05	3.64	2.49	3.68	3.01	3.72	3.65	3.76	4.42	3.8	5.36	3.84	6.49	3.88	7.87
4.2	1.62	4.24	1.96	4.28	2.37	4.32	2.87	4.36	3.48	4.4	4.22	4.44	5.22	4.48	6.19
4.8	0.715	4.84	0.866	4.88	1.05	4.92	1.27	4.96	1.54	5	1.87				

Rbot=21.5 kΩ		Rbot=26.1 kΩ		Rbot=31.6 kΩ		Rbot=38.3 kΩ		Rbot=46.4 kΩ		Rbot=56.2 kΩ		Rbot=68.1 kΩ		Rbot=82.5 kΩ	
Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)	Vout (V)	Rtop (kΩ)
0.9	Open	0.95	Open	1	Open	1.05	Open	1.1	Open	1.15	Open	1.2	Open	1.25	Open
0.68	100	0.69	121	0.7	14.7	0.71	178	0.72	215	0.73	261	0.74	316	0.75	402
0.83	71.5	0.84	86.6	0.85	105	0.86	127	0.87	154	0.88	187	0.89	226	0.9	274
0.98	53.6	0.99	64.9	1	78.7	1.01	95.3	1.02	115	1.03	140	1.04	169	1.05	205
1.13	42.2	1.14	51.1	1.15	61.9	1.16	75	1.17	90.9	1.18	110	1.19	133	1.2	162
1.36	33.2	1.38	40.2	1.4	48.7	1.42	59	1.44	71.5	1.46	86.6	1.48	105	1.5	127
1.66	26.1	1.68	31.6	1.7	38.3	1.72	46.4	1.74	56.2	1.76	68.1	1.78	82.5	1.8	100
1.96	21.5	1.98	26.1	2	31.6	2.02	38.3	2.04	46.4	2.06	56.2	2.08	68.1	2.1	82.5
2.26	17.8	2.28	21.5	2.3	26.1	2.32	31.6	2.34	38.3	2.36	46.4	2.38	56.2	2.4	68.1
2.72	14.7	2.76	17.8	2.8	21.5	2.84	26.1	2.88	31.6	2.92	38.3	2.96	46.4	3	56.2
3.32	12.1	3.36	14.7	3.4	17.8	3.44	21.5	3.48	26.1	3.52	31.6	3.56	38.3	3.6	46.4
3.92	9.53	3.96	11.5	4	14	4.04	16.9	4.08	20.5	4.12	24.9	4.16	30.1	4.2	36.5
4.52	7.5	4.56	9.09	4.6	11	4.64	13.3	4.68	16.2	4.72	19.6	4.76	23.7	4.8	28.7

Table 1: VSET pin strap resistor dividers

Output voltage adjust using PMBus

The output voltage set by pin-strap can be overridden by configuration file or by using a PMBus command. See Electrical Specification for adjustment range.

Output voltage range limitation

The product includes a precision programmable feedback divider, with the feedback divider, output voltage up to 5V can be obtained. The feedback divider ratio can be set by VSET pin-strap or by the PMBus command VOUT_SCALE_LOOP.

When using pin-strap to set Vout, the feedback divider ratio and output voltage range is limited by the pin-strap resistor divider. The default feedback divider ratio and minimum/maximum output voltage is set to the value in below table. This protects the application circuit from an under voltage/over voltage in case accidental PMBus command. The output voltage limit can be reconfigured to by writing the PMBus command VOUT_MIN and VOUT_MAX.

V_{out} pin-strap value	VOUT_SCALE_LOOP	VOUT_MIN default value	VOUT_MAX default value
0.6 to 1.2 V	0.5	0.5 V	1.5 V
1.2 to 2.4 V	0.25	1 V	3 V
2.4 to 5 V	0.125	2 V	6 V

Table 2: VOUT_SCALE_LOOP, VOUT_MIN default and VOUT_MAX default when using pin-strap set V_{out}

When using PMBus command to set Vout, the recommended operating range of VOUT_COMMAND is dependent upon the feedback divider ratio. Setting VOUT_COMMAND lower than the recommended range can negatively affect VOUT regulation accuracy, while setting VOUT_COMMAND above the recommended range can limit the actual output voltage achieved.

V_{out} Range	VOUT_SCALE_LOOP
0.6 to 0.75 V	1
0.6 to 1.5 V	0.5
1 to 3 V	0.25
2 to 5 V	0.125

Table 3: Recommand V_{out} range when using VOUT_COMMAND to set V_{out}

Voltage margining up/down

Using the PMBus interface, The product can adjust its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating outside its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit outside its typical operating range. This functionality can also be used to test of supply voltage supervisors. Margin limits of the nominal output voltage ±5% are default, but the margin limits can be reconfigured using the PMBus interface.

Output Ripple and Noise

Output ripple and noise is measured according to figure below.

A 50 mm conductor works as a small inductor forming together with the two capacitors as a damped filter.

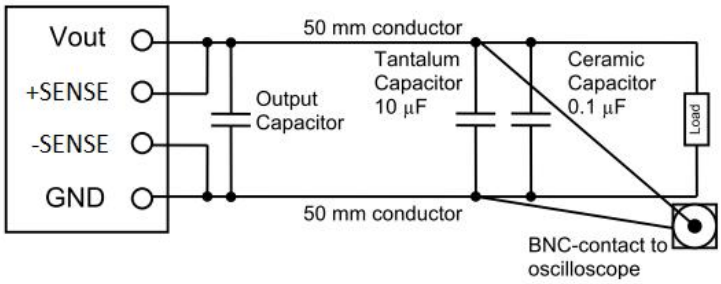


Figure 4: Output ripple and noise test set-up

Output over current limit adjust using pin-strap resistor (MSEL pin)

Using an external pin-strap resistor divider between VCC1V5 pin and AGND pin, Rtop and Rbot, the output over current limit can be programmed. For standalone device or the master device in parallel operation, refer to Table 4. For the slave devices in parallel operation, refer to Table 5. Maximum 1% tolerance resistors are required.

The resistor divider also programs value for Vout ramp-up time TON_RISE and paralleling configuration STACK_CONFIG (0xEC).

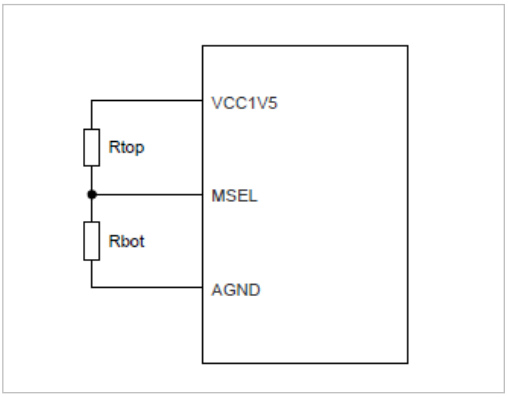


Figure 5: Pin-strap resistor for MSEL pin

Rbot=4.64 kΩ				Rbot=5.62 kΩ				Rbot=6.81 kΩ				Rbot=8.25 kΩ			
STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)
Standalone	40/52	0.5	21.5	2 phases	40/52	0.5	26.1	3 phases	40/52	0.5	31.6	4 phases	40/52	0.5	38.3
Standalone	40/52	1	15.4	2 phases	40/52	1	18.7	3 phases	40/52	1	22.6	4 phases	40/52	1	27.4
Standalone	40/52	3	11.5	2 phases	40/52	3	14	3 phases	40/52	3	16.9	4 phases	40/52	3	20.5
Standalone	40/52	5	9.09	2 phases	40/52	5	11	3 phases	40/52	5	13.3	4 phases	40/52	5	16.2
Standalone	40/52	7	7.15	2 phases	40/52	7	8.66	3 phases	40/52	7	10.5	4 phases	40/52	7	12.7
Standalone	40/52	10	5.62	2 phases	40/52	10	6.81	3 phases	40/52	10	8.25	4 phases	40/52	10	10
Standalone	40/52	20	4.64	2 phases	40/52	20	5.62	3 phases	40/52	20	6.81	4 phases	40/52	20	8.25
Standalone	40/52	31.75	3.83	2 phases	40/52	31.75	4.64	3 phases	40/52	31.75	5.62	4 phases	40/52	31.75	6.81

Rbot=10 kΩ				Rbot=12.1 kΩ				Rbot=14.7 kΩ				Rbot=17.8 kΩ			
STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)
Standalone	30/39	0.5	46.4	2 phases	30/39	0.5	56.2	3 phases	30/39	0.5	68.1	4 phases	30/39	0.5	82.5
Standalone	30/39	1	33.2	2 phases	30/39	1	40.2	3 phases	30/39	1	48.7	4 phases	30/39	1	59
Standalone	30/39	3	24.9	2 phases	30/39	3	30.1	3 phases	30/39	3	36.5	4 phases	30/39	3	44.2
Standalone	30/39	5	19.6	2 phases	30/39	5	23.7	3 phases	30/39	5	28.7	4 phases	30/39	5	34.8
Standalone	30/39	7	15.4	2 phases	30/39	7	18.7	3 phases	30/39	7	22.6	4 phases	30/39	7	27.4
Standalone	30/39	10	12.1	2 phases	30/39	10	14.7	3 phases	30/39	10	17.8	4 phases	30/39	10	21.5
Standalone	30/39	20	10	2 phases	30/39	20	12.1	3 phases	30/39	20	14.7	4 phases	30/39	20	17.8
Standalone	30/39	31.75	8.25	2 phases	30/39	31.75	10	3 phases	30/39	31.75	12.1	4 phases	30/39	31.75	14.7

Rbot=21.5 kΩ				Rbot=26.1 kΩ				Rbot=31.6 kΩ				Rbot=38.3 kΩ			
STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)	STACK_CONFIG	OC_WARN/OC_FAULT (A)	TON_RISE (ms)	Rtop (kΩ)
Standalone	20/26	0.5	100	2 phases	20/26	0.5	121	3 phases	20/26	0.5	147	4 phases	20/26	0.5	178
Standalone	20/26	1	71.5	2 phases	20/26	1	86.6	3 phases	20/26	1	105	4 phases	20/26	1	127
Standalone	20/26	3	53.6	2 phases	20/26	3	64.9	3 phases	20/26	3	78.7	4 phases	20/26	3	95.3
Standalone	20/26	5	42.2	2 phases	20/26	5	51.1	3 phases	20/26	5	61.9	4 phases	20/26	5	75
Standalone	20/26	7	33.2	2 phases	20/26	7	40.2	3 phases	20/26	7	48.7	4 phases	20/26	7	59
Standalone	20/26	10	26.1	2 phases	20/26	10	31.6	3 phases	20/26	10	38.3	4 phases	20/26	10	46.4
Standalone	20/26	20	21.5	2 phases	20/26	20	26.1	3 phases	20/26	20	31.6	4 phases	20/26	20	38.3
Standalone	20/26	31.75	17.8	2 phases	20/26	31.75	21.5	3 phases	20/26	31.75	26.1	4 phases	20/26	31.75	31.6

Table 4: MSEL pin strap resistor dividers for standalone device or the master device in parallel operation

		Slave 1		Slave 2		Slave 3	
STACK_CONFIG	OC_WARN/OC_FAULT (A)	Rbot (kΩ)	Rtop (kΩ)	Rbot (kΩ)	Rtop (kΩ)	Rbot (kΩ)	Rtop (kΩ)
2 phases	40/52	0	Open				
2 phases	30/39	Open	Open				
2 phases	20/26	14.7	48.7				
3 phases	40/52	10	Open	21.5	Open		
3 phases	30/39	12.1	Open	26.1	Open		
3 phases	20/26	10	33.2	21.5	71.5		
4 phases	40/52	6.81	Open	68.1	Open	31.6	Open
4 phases	30/39	8.25	Open	82.5	Open	38.3	Open
4 phases	20/26	6.81	22.6	68.1	226	31.6	105

Table 5: MSEL pin strap resistor dividers for the slave device in parallel operation

Output current limit adjust using PMBus

The output over current limit set by pin-strap can be overridden by configuration file or by using a PMBus command. See Electrical Specification for adjustment range.

Power good

The power good pin (PG) is used to signal to the system and indicates when the product is ready to provide regulated output voltage to the load. The power good output is open drain and internally pulled up to 5V. Any condition which causes the module stop, PG will be held low.

Switching frequency

The default switching frequency is 450 kHz, which yields optimal power efficiency. The switching frequency can be set to any values between 450 kHz and 900 kHz using the PMBus interface, but only 5 values are effective, see Table 6. The switching frequency will change the efficiency/power dissipation, load transient response and output ripple. The control loop must be re-optimized when changing the switching frequency.

FREQUENCY_SWITCH (Decoded)	Effective Switching Frequency (kHz)
411 ≤ FSW < 500 kHz	450
501 ≤ FSW < 600 kHz	550
601 ≤ FSW < 700 kHz	650
701 ≤ FSW < 820 kHz	750
821 ≤ FSW < 1000 kHz	900

Table 6: Supported Switching Frequency Setting

Synchronization

Synchronization is a feature that allows multiple products to be synchronized to a common frequency. Synchronized products powered from the same bus eliminate beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the slow beat frequencies (usually <10 kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.
The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC Output, working as a source driving the synchronization. All others on the same synchronization bus must be configured with SYNC Input. Default configuration is using the internal clock, independently of signal at the SYNC pin. See application note AN309 for further information.

Phase spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and efficiency losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized. The phase spreading of the product can be configured using the PMBus interface. See application note AN309 for further information.

For standalone devices, the phase position can be set to 0°, 90°, 120°, 180°, 240°, 270°. For devices in parallel operation, the phase position is fixed and can not be optimized in Flex Power Designer software. See section "Phase interleaving" for further information.

Soft-start and soft-stop

The soft-start and soft-stop control functionality allows the output voltage to ramp-up and ramp-down with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple controllers.

The rise time is the time taken for the output to ramp to its target voltage, while the fall time is the time taken for the output to ramp down from its regulation voltage to 0 V. The turn-on-delay time sets a delay from when the output is enabled until the output voltage starts to ramp up. The turn-off-delay time sets a delay from when the output is disabled until the output voltage starts to ramp down.

The default settings for the soft-start delay period and the soft-start ramp time is 10 ms. Hence, power-up is completed within 20 ms in default configuration using remote control.

In default configuration, soft-stop is disabled and the regulation of output voltage stops immediately when the output is disabled. Soft-stop can be enabled through the PMBus command ON_OFF_CONFIG. The delay and ramp times can be reconfigured using the PMBus commands TON_DELAY, TON_RISE, TOFF_DELAY and TOFF_FALL.

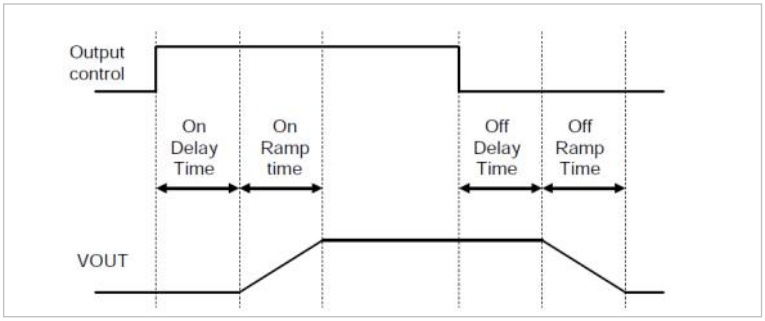


Figure 6: Illustration of soft-start and soft-stsop

Pre-bias startup capabilities

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual supply logic component, such as FPGAs or ASICs. There could also be still charged output capacitors when starting up shortly after turn-off. The product incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition.

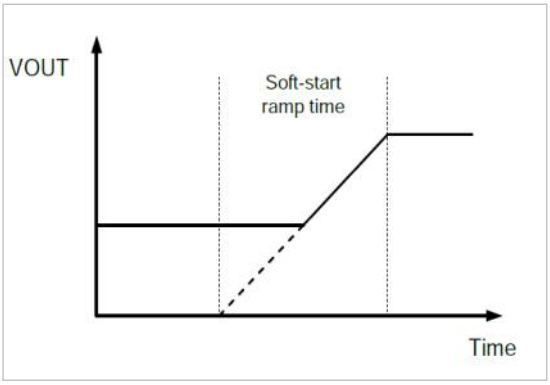


Figure 7: Illustration of pre-bias startup

Output voltage sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors such as FPGAs and ASICs that require one supply to reach its operating voltage prior to another.

Different types of multi-product sequencing are supported:

1. Time based sequencing: Configuring the start delay and rise time of each module through the PMBus interface and by connecting the CTRL pin of each product to a common enable signal.
2. Event based sequencing: Routing the PG pin signal of one module to the CTRL pin of the next module in the sequence.

These sequencing options are easily configured using the Flex Power Designer software. See application note AN310 for further information.

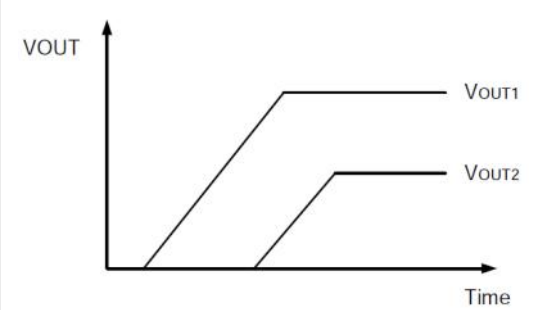


Figure 8: Illustration of output voltage sequencing

Parallel Operation (Current Sharing)

Up to 4 products can be operated in parallel to increase the output current capability of a single power rail. By connecting devices according to below table and configuring the devices as a current sharing rail, the units will share the current equally, enabling up to 100% utilization of the current capability for each device in the current sharing rail.

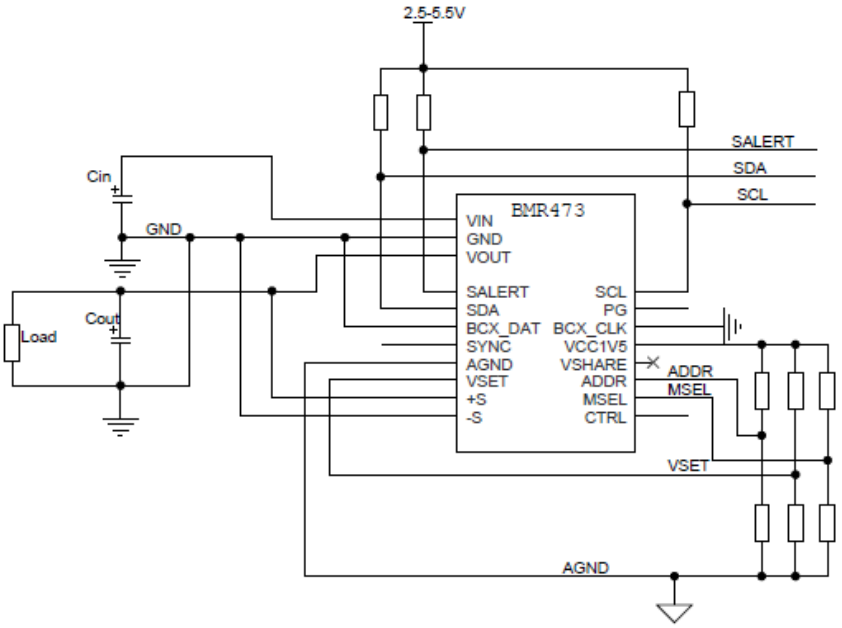


Figure 9: Circuit diagram for standalone operation

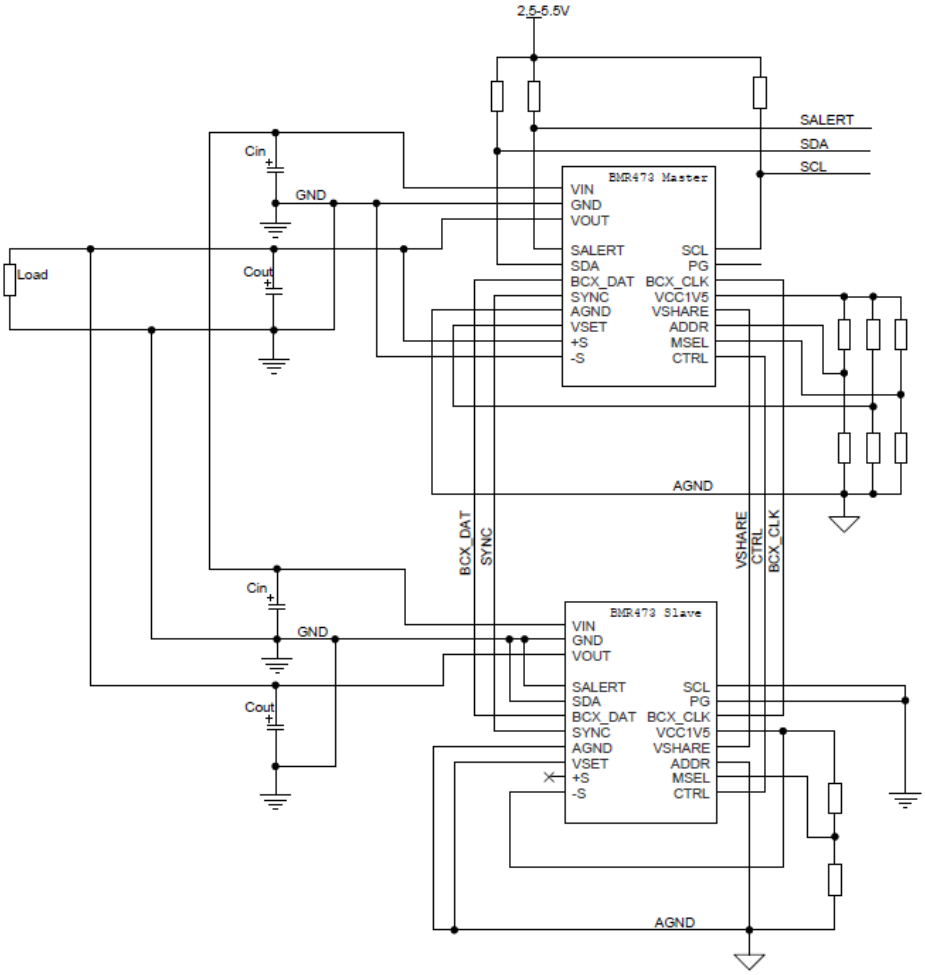


Figure 10: circuit diagram for 2 parallel operation

Pin No.	Designation	Standalone	Master	Slave
4A	SALERT	Connect to system PMBus or GND if not used	Connect to system PMBus or GND if not used	Short to GND
4B	SCL	Connect to system PMBus or GND if not used	Connect to system PMBus or GND if not used	Short to GND
5A	SDA	Connect to system PMBus or GND if not used	Connect to system PMBus or GND if not used	Short to GND
5B	PG	Connect to system PGD or GND if not used	Connect to system PGD or GND if not used	Short to GND
6A	BCX_DAT	Short to GND	Connect to BCX_DAT of the slave	Connect to BCX_DAT of the master
6B	BCX_CLK	Short to GND	Connect to BCX_CLK of the slave	Connect to BCX_CLK of the master
7A	SYNC	Connect to external Sync or floating	Connect to external sync or slave SYNC	Connect to SYNC of the master
7B	VCC1V5	Reference voltage for pin strapping	Reference voltage for mas-ter pin strapping	Reference voltage for slave pin strapping
8A	AGND	Ground reference for pin strapping	Ground reference for mas-ter pin strapping	Ground reference for slave pin strapping
8B	VSHARE	Floating	Connect to VSHARE of the slave	Connect to VSHARE of the master
9A	VSET	Programming VSET	Programming VSET for the master	Short to GND
9B	ADDR	Programming ADDR	Programming ADDR for the master	Short to GND
10A	+S	Connect to VOUT at output regulation point	Connect to VOUT at output regulation point	Floating
10B	MSEL	Programming MSEL	Programming MSEL of the master	Programming MSEL of the slave
11A	-S	Connect to GND at output regulation point	Connect to GND at output regulation point	Connect to VCC1V5, to indicate slave
11B	CTRL	Connect to system remote control	Connect to system remote control	Connect to CTRL of the master

Table 7: Digital pins connection for standalone/parallel operation

Output voltage sense (+SENSE/-SENSE pins)

+SENSE/-SENSE are the input of the remote sense amplifier. For standalone device or the master device in parallel operation, +SENSE/-SENSE should be connected to Vout/GND at output voltage regulation point. For the slave device in parallel operation, +SENSE should be left floating and –SENSE should be connected to its VCC1V5 pin to indicate the device as the slave.

VSHARE

In parallel operation, all devices share the same internal control voltage through VSHARE pin. The sensed current in each phase is regulated by the VSHARE voltage by internal transconductance amplifier, to achieve loop compensation and current balancing between different phases. The amplifier output voltage is compared with an internal PWM ramp to generate the PWM pulse.

Back-channel communication

To allow multiple devices with a shared output to communicate through a single PMBus address, the back-channel communication is impemented through BCX_CLK and BCX_DAT pins.

During power on reset (POR), the master reads the programmed values from the slaves to ensure all expected slaves are present and correctly phase-shifted. Then, the Master will load critical operating parameters to the slave devices to ensure correct operation of the stack.

During operation, the master device receives and responds to all PMBus communication, and slave devices do not need to be connected to the PMBus. If the master receives commands that require updates to the PMBus registers of the slave, the master relays these commands to the slaves. Additionally, the master periodically polls slave devices for status and telemetry information to maintain an accurate record of the telemetry and STATUS information for the full stack of paralleling devices.

Phase interleaving

The INTERLEAVE command is used to arrange multiple devices sharing a common SYNC signal in time. In a multi-phase parallel stack, the phase delay added to each device is equal to 360° / Number in Group × Order. To prevent misaligning the phases of a multi-phase stack, INTERLEAVE is read only when the device is configured as part of a multi-phase stack. The Read/Write status of the INTERLEAVE command is set based on the state of the STACK_CONFIG command at power-on and is not updated if STACK_CONFIG is later changed. If INTERLEAVE will be used to program the phase position of a stand-alone device, the device must be configured as standalone at power-on to ensure write capability of the INTERLEAVE command.

Number in Group	Order	Phase position (°)
1	0	0
2	0	0
2	1	180
3	0	0
3	1	120
3	2	240
4	0	0
4	1	90
4	2	180
4	3	270

Table 8: Supported phase interleaving settings

PCB layout considerations

The input capacitor should be placed as close to the input pins as possible. The output capacitor should be placed close to the load.

The routing of SYNC, BCX_CLK and BCX_DAT traces should be kept away from senstive analog signals.

The pin-strap resistors, should be placed close to the product to minimize loops that may pick up noise. Avoid current carrying planes under the pin-strap resistors and the PMBus signals.

Care should be taken in the routing of VSHARE connections between master and slave devices in parallel operation. The connections should be routed between AGND planes and avoid areas of high electric or magnetic fields.

Care should be taken in the routing of the connections from the sensed output voltage to the +SENSE and –SENSE terminals. These sensing connections should be routed as a differential pair, preferably between ground planes which are not carrying high currents. The routing should avoid areas of high electric or magnetic fields.

POWER MANAGEMENT

PMBus overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin. The following product parameters can continuously be monitored by a host: input voltage, output voltage/ current, duty cycle and internal temperature.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface.

Throughout this document, different PMBus commands are referenced. The Flex Power Designer software tool can be used to configure and monitor this product via the PMBus interface. More information is found on our website.

SMBus interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I²C (master must allow for clock stretching) or SMBus host device. In addition, the product is compatible with PMBus version 1.3 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports 100 kHz, 400 kHz and 1MHz bus clock frequency. The PMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\tau = R_P C_p \leq 1us$$

R_P is the pull-up resistor value and C_P is the bus load. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply between 2.7 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

It is recommended to always use PEC (Packet Error Check) when communicating via PMBus. There is an optional setting that makes PEC required which further increase communication robustness. This can be configured by setting bit 15 in command MISC_OPTIONS (0xED).

PMBus addressing (ADDR pin)

The resistor divider between the VCC1V5 pin and the AGND pin for the ADDR pin selects the range of PMBus address and SYNC direction. For standalone devices, the resistor divider also selects the Phase Shift between SYNC and the switch node. Recommended resistor values are shown in the table below. 1% tolerance resistors are required.

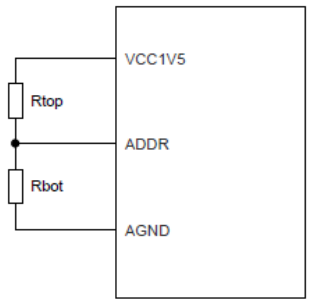


Figure 11: PMBus addressing with pin strap

Rbot=4.64kΩ			Rbot=5.62kΩ			Rbot=6.81kΩ			Rbot=8.25kΩ		
ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)
10h	0, Auto	Open	11h	0, Auto	Open	12h	0, Auto	Open	13h	0, Auto	Open
10h	0, In	21.5	11h	0, In	26.1	12h	0, In	31.6	13h	0, In	38.3
10h	90, In	11.5	11h	90, In	14	12h	90, In	16.9	13h	90, In	20.5
10h	120, In	7.15	11h	120, In	8.66	12h	120, In	10.5	13h	120, In	12.7
10h	180, In	4.64	11h	180, In	5.62	12h	180, In	6.81	13h	180, In	8.25
10h	240, In	3.16	11h	240, In	3.83	12h	240, In	4.64	13h	240, In	5.62
10h	270, In	2.05	11h	270, In	2.49	12h	270, In	3.01	13h	270, In	3.65
10h	0, Out	1.27	11h	0, Out	1.54	12h	0, Out	1.87	13h	0, Out	2.26
10h	180, Out	0.715	11h	180, Out	0.866	12h	180, Out	1.05	13h	180, Out	1.27

Rbot=10kΩ			Rbot=12.1kΩ			Rbot=14.7kΩ			Rbot=17.8kΩ		
ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)
14h	0, Auto	Open	15h	0, Auto	Open	16h	0, Auto	Open	17h	0, Auto	Open
14h	0, In	46.4	15h	0, In	56.2	16h	0, In	68.1	17h	0, In	82.5
14h	90, In	24.9	15h	90, In	30.1	16h	90, In	36.5	17h	90, In	44.2
14h	120, In	15.4	15h	120, In	18.7	16h	120, In	22.6	17h	120, In	27.4
14h	180, In	10	15h	180, In	12.1	16h	180, In	14.7	17h	180, In	17.8
14h	240, In	6.81	15h	240, In	8.25	16h	240, In	10	17h	240, In	12.1
14h	270, In	4.42	15h	270, In	5.36	16h	270, In	6.49	17h	270, In	7.87
14h	0, Out	2.74	15h	0, Out	3.32	16h	0, Out	4.02	17h	0, Out	4.87
14h	180, Out	1.54	15h	180, Out	1.87	16h	180, Out	2.26	17h	180, Out	2.74

Table 9: Resistor values for hard–wiring PMBus addresses

PMBus addressing (ADDR pin) - contd.

Rbot=21.5kΩ			Rbot=26.1kΩ			Rbot=31.6kΩ			Rbot=38.3kΩ		
ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)
18h	0, Auto	Open	19h	0, Auto	Open	1Ah	0, Auto	Open	1Bh	0, Auto	Open
18h	0, In	100	19h	0, In	121	1Ah	0, In	147	1Bh	0, In	178
18h	90, In	53.6	19h	90, In	64.9	1Ah	90, In	78.7	1Bh	90, In	95.3
18h	120, In	33.2	19h	120, In	40.2	1Ah	120, In	48.7	1Bh	120, In	59
18h	180, In	21.5	19h	180, In	26.1	1Ah	180, In	31.6	1Bh	180, In	38.3
18h	240, In	14.7	19h	240, In	17.8	1Ah	240, In	21.5	1Bh	240, In	26.1
18h	270, In	9.53	19h	270, In	11.5	1Ah	270, In	14	1Bh	270, In	16.9
18h	0, Out	5.9	19h	0, Out	7.15	1Ah	0, Out	8.66	1Bh	0, Out	10.5
18h	180, Out	3.32	19h	180, Out	4.02	1Ah	180, Out	4.87	1Bh	180, Out	5.9

Rbot=46.4kΩ			Rbot=56.2kΩ			Rbot=68.1kΩ			Rbot=82.5kΩ		
ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)
1Ch	0, Auto	Open	1Dh	0, Auto	Open	1Eh	0, Auto	Open	1Fh	0, Auto	Open
1Ch	0, In	215	1Dh	0, In	261	1Eh	0, In	316	1Fh	0, In	402
1Ch	90, In	115	1Dh	90, In	140	1Eh	90, In	169	1Fh	90, In	205
1Ch	120, In	71.5	1Dh	120, In	86.6	1Eh	120, In	105	1Fh	120, In	127
1Ch	180, In	46.4	1Dh	180, In	56.2	1Eh	180, In	68.1	1Fh	180, In	82.5
1Ch	240, In	31.6	1Dh	240, In	38.3	1Eh	240, In	46.4	1Fh	240, In	56.2
1Ch	270, In	20.5	1Dh	270, In	24.9	1Eh	270, In	30.1	1Fh	270, In	26.5
1Ch	0, Out	12.7	1Dh	0, Out	15.4	1Eh	0, Out	18.7	1Fh	0, Out	22.6
1Ch	180, Out	7.15	1Dh	180, Out	8.66	1Eh	180, Out	10.5	1Fh	180, Out	12.7

Rbot=4.64kΩ			Rbot=5.62kΩ			Rbot=6.81kΩ			Rbot=8.25kΩ		
ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)
20h	0, In	15.4	21h	0, In	18.7	22h	0, In	22.6	23h	0, In	27.4
20h	90, In	9.09	21h	90, In	11	22h	90, In	13.3	23h	90, In	16.2
20h	120, In	5.62	21h	120, In	6.81	22h	120, In	8.25	23h	120, In	10
20h	180, In	3.83	21h	180, In	4.64	22h	180, In	5.62	23h	180, In	6.81
20h	240, In	2.61	21h	240, In	3.16	22h	240, In	3.83	23h	240, In	4.64
20h	270, In	1.62	21h	270, In	1.96	22h	270, In	2.37	23h	270, In	2.87
20h	0, Out	0.953	21h	0, Out	1.15	22h	0, Out	1.4	23h	0, Out	1.69
20h	180, Out	0.511	21h	180, Out	0.619	22h	180, Out	0.75	23h	180, Out	0.909

Table 9: Resistor values for hard–wiring PMBus addresses

PMBus addressing (ADDR pin) - contd.

Rbot=10kΩ			Rbot=12.1kΩ			Rbot=14.7kΩ			Rbot=17.8kΩ		
ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)
24h	0, In	33.2	25h	0, In	40.2	26h	0, In	48.7	27h	0, In	59
24h	90, In	19.6	25h	90, In	23.7	26h	90, In	28.7	27h	90, In	34.8
24h	120, In	12.1	25h	120, In	14.7	26h	120, In	17.8	27h	120, In	21.5
24h	180, In	8.25	25h	180, In	10	26h	180, In	12.1	27h	180, In	14.7
24h	240, In	5.62	25h	240, In	6.81	26h	240, In	8.25	27h	240, In	10
24h	270, In	3.48	25h	270, In	4.22	26h	270, In	5.11	27h	270, In	6.19
24h	0, Out	2.05	25h	0, Out	2.49	26h	0, Out	3.01	27h	0, Out	3.65
24h	180, Out	1.1	25h	180, Out	1.33	26h	180, Out	1.62	27h	180, Out	1.96

Rbot=26.1kΩ			Rbot=31.6kΩ			Rbot=38.3kΩ			Rbot=46.4kΩ		
ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)
29h	0, In	86.6	2Ah	0, In	105	2Bh	0, In	127	2Ch	0, In	154
29h	90, In	51.1	2Ah	90, In	61.9	2Bh	90, In	75	2Ch	90, In	90.9
29h	120, In	31.6	2Ah	120, In	38.3	2Bh	120, In	46.4	2Ch	120, In	56.2
29h	180, In	21.5	2Ah	180, In	26.1	2Bh	180, In	31.6	2Ch	180, In	38.3
29h	240, In	14.7	2Ah	240, In	17.8	2Bh	240, In	21.5	2Ch	240, In	26.1
29h	270, In	9.09	2Ah	270, In	11	2Bh	270, In	13.3	2Ch	270, In	16.2
29h	0, Out	5.36	2Ah	0, Out	6.49	2Bh	0, Out	7.87	2Ch	0, Out	9.53
29h	180, Out	2.87	2Ah	180, Out	3.48	2Bh	180, Out	4.22	2Ch	180, Out	5.11

Rbot=56.2kΩ			Rbot=68.1kΩ			Rbot=82.5kΩ			Rbot=21.5kΩ		
ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)	ADDRESS	INTERLEAVE	Rtop (kΩ)
2Dh	0, In	187	2Eh	0, In	226	2Fh	0, In	274	48h	0, In	71.5
2Dh	90, In	110	2Eh	90, In	133	2Fh	90, In	162	48h	90, In	42.2
2Dh	120, In	68.1	2Eh	120, In	82.5	2Fh	120, In	100	48h	120, In	26.1
2Dh	180, In	46.4	2Eh	180, In	56.2	2Fh	180, In	68.1	48h	180, In	17.8
2Dh	240, In	31.6	2Eh	240, In	38.3	2Fh	240, In	46.4	48h	240, In	12.1
2Dh	270, In	19.6	2Eh	270, In	23.7	2Fh	270, In	28.7	48h	270, In	7.5
2Dh	0, Out	11.5	2Eh	0, Out	14	2Fh	0, Out	16.9	48h	0, Out	4.42
2Dh	180, Out	6.19	2Eh	180, Out	1.5	2Fh	180, Out	9.09	48h	180, Out	2.37

Table 9: Resistor values for hard–wiring PMBus addresses

Reserved addresses

Some addresses are reserved or assigned according to the SMBus standard specification and may not be usable. The following reserved addresses are invalid and can not be programmed: 0x0C, 0x28, 0x37, 0x61. Please refer to the SMBus standard specification for further information.

Non-volatile memory (NVM)

The product incorporates one Non-Volatile Memory area for storage of the PMBus command values, the User NVM.

The User NVM is pre-loaded with Flex factory default values. The User NVM is writable and open for customization. The values in NVM are loaded during initialization according to section Initialization Procedure, where after commands can be changed through the PMBus Interface.

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Output current	READ_IOUT
Temperature	READ_TEMPERATURE_1

Monitoring faults

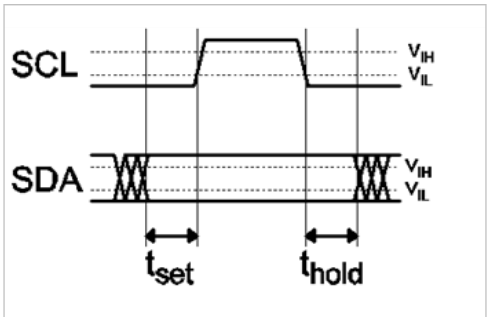
Fault conditions can be detected using the SALERT pin, which will be asserted low when any number of preconfigured fault or warning conditions occurs. The SALERT pin will be held low until faults and/or warnings are cleared by the CLEAR_FAULTS command, or until the output voltage has been re-enabled. It is possible to mask which fault conditions should not assert the SALERT pin by the command SMBALERT_MASK. In response to the SALERT signal, the user may read a number of status commands to find out what fault or warning condition occurred, see table below.

Fault and warning status	PMBus command
Overview, Power Good	STATUS_BYTE; STATUS_WORD
Output voltage level	STATUS _VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

I2C/PMBus timing

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the rising edge of the clock signal, SCL. If these times are violated, incorrect data may be captured or meta stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. This product supports the PEC (packet error checking) according to the SMBus specification.
When sending subsequent commands to the same module, it is recommended to insert additional delays according to the table below.

After sending PMBus command	Required delay before additional command
STORE_USER_ALL	100 ms
RESTORE_USER_ALL	100 ms
VOUT_MAX	10 ms
Any other command	2 ms after reading 10 ms after writing



Picture12: Set-up and hold times timing diagramm

Command protection

The user may write-protect PMBus commands in the User NVM by using the command WRITE_PROTECT.

Initialization procedure

The product follows an internal initialization procedure after power is applied to the VIN pins:

1. Self test and memory check.
2. The address pin-strap resistor is measured and the associated PMBus address is defined.
3. The output voltage pin-strap resistor is measured and the associated output voltage level will be loaded to operational RAM of PMBus command VOUT_COMMAND.
4. Values stored in the User NVM are loaded into operational RAM memory. If VOUT_COMMAND is set by pin-strap, at power up, the VOUT is based on pin strap.

Once this procedure is completed and the initialization time will take up to 10 ms to complete, the output voltage is ready to be enabled using the CTRL pin. The product is also ready to accept commands via the PMBus interface, which in case of writes will overwrite any values loaded during the initialization procedure.

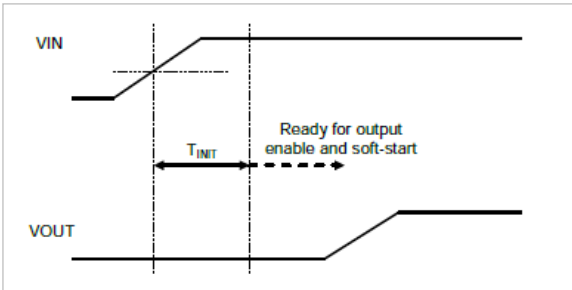


Figure 13 : Illustration of Initialization time