Technical Reference PMBus BMR473

This appendix contains a detailed reference of the PMBus commands supported by the product.

Data Formats

The products make use of a few standardized numerical formats, along with custom data formats. A detailed walkthrough of the above formats is provided in AN304, as well as in sections 7 and 8 of the PMBus Specification Part II. The custom data formats vary depending on the command, and are detailed in the command description.

Standard Commands

The functionality of commands with code 0x00 to 0xCF is usually based on the corresponding command specification provided in the PMBus Standard Specification Part II (see Power System Management Bus Protocol Documents below). However there might be different interpretations of the PMBus Standard Specification or only parts of the Standard Specification applied, thus the detailed command description below should always be consulted.

Forum Websites

The System Management Interface Forum (SMIF)

http://www.powersig.org/

The System Management Interface Forum (SMIF) supports the rapid advancement of an efficient and compatible technology base that promotes power management and systems technology implementations. The SMIF provides a membership path for any company or individual to be active participants in any or all of the various working groups established by the implementer forums.

Power Management Bus Implementers Forum

(PMBUS-IF)

http://pmbus.org/

The PMBus-IF supports the advancement and early adoption of the PMBus protocol for power management. This website offers recent PMBus specification documents, PMBus articles, as well as upcoming PMBus presentations and seminars, PMBus Document Review Board (DRB) meeting notes, and other PMBus related news.

PMBus – Power System Management Bus Protocol Documents

These specification documents may be obtained from the PMBus-IF website described above. These are required reading for complete understanding of the PMBus implementation. This appendix will not re-address all of the details contained within the two PMBus Specification documents.

Specification Part I - General Requirements Transport And Electrical Interface Includes the general requirements, defines the transport and electrical interface and timing requirements of hard wired signals.

Specification Part II - Command Language

Describes the operation of commands, data formats, fault management and defines the command language used with the PMBus.

SMBus – System Management Bus Documents

System Management Bus Specification, Version 2.0, August 3, 2000 This specification specifies the version of the SMBus on which Revision 1.2 of the PMBus Specification is based. This specification is freely available from the System Management Interface Forum Web site at: <u>http://www.smbus.org/specs/</u>

PMBus Command Summary and Factory Default Values of Standard Configuration

The factory default values provided in the table below are valid for the Standard configuration. Factory default values for other configurations can be found using the Flex Power Designer tool.

Code	Name	Data Format	Factory Defa	ult Value	Min Set	Max Set	Unit
			Standard		Value	Value	
			Configuration				
0x01	OPERATION	R/W Byte	BMR4731X01/ 0x04				
0x01	ON OFF CONFIG	R/W Byte	0x04 0x17				
0x02 0x03	CLEAR_FAULTS	Send Byte	0.17				
0x03 0x04	PHASE	R/W Byte					
0x04 0x10	WRITE_PROTECT		0x00				
0x10 0x15		R/W Byte	000				
	STORE_USER_ALL (Phase 0xFF)	Send Byte					
0x16	RESTORE_USER_ALL (Phase 0xFF)	Send Byte					
0x19	CAPABILITY	Read Byte					
Ox1B	SMBALERT_MASK_VOUT	SMBAlert	0x00				
	(STATUS_VOUT)	Mask					
Ox1B	SMBALERT_MASK_VOUT	SMBAlert	0x00				
	(Phase 0xFF)	Mask					
Ox1B	SMBALERT_MASK_IOUT	SMBAlert	0x00				
	(STATUS_IOUT)	Mask					
Ox1B	SMBALERT_MASK_IOUT (Phase	SMBAlert	0x00				
	OxFF)	Mask					
Ox1B	SMBALERT_MASK_INPUT	SMBAlert	0x00				
	(STATUS_INPUT)	Mask					
Ox1B	SMBALERT_MASK_INPUT	SMBAlert	0x00				
	(Phase OxFF)	Mask					
Ox1B	SMBALERT_MASK_TEMPERATU	SMBAlert	0x00				
0.15	RE (STATUS_TEMPERATURE)	Mask					
Ox1B	SMBALERT_MASK_TEMPERATU	SMBAlert	0x00				
0.15	RE (Phase 0xFF)	Mask	0.00				
Ox1B	SMBALERT_MASK_CML	SMBAlert	0x00				
0.10	(STATUS_CML)	Mask	000				
Ox1B	SMBALERT_MASK_CML (Phase 0xFF)	SMBAlert	0x00				
010		Mask	000				
Ox1B	SMBALERT_MASK_MFR_SPECIFI C (STATUS_MFR_SPECIFIC)	SMBAlert	0x00				
Ox1B	SMBALERT_MASK_MFR_SPECIFIC	Mask SMBAlert	0x00				
UXID	C (Phase 0xFF)	Mask	0000				
0x20	VOUT_MODE	Read Byte	0x97				
0x20 0x21		R/W Word	1 x Vout by p	in strap			
0x21 0x22	VOUT_TRIM	R/W Word	Unit Specific	nn-snup			
0x22 0x24	VOUT_MAX	R/W Word	Configured b	, nin	0.6	6.0	V
UXZ4	VOULMAX	K/W WOIG	strap	у рш-	0.0	0.0	v
0x25	VOUT_MARGIN_HIGH	R/W Word	0x021A	1.05			* Vout
0x26	VOUT_MARGIN_LOW	R/W Word	0x01E6	0.95			* Vout
0x27	VOUT_TRANSITION_RATE	R/W Word	0xE010	1.00	0.067	15.933	V/ms
0x29	VOUT_SCALE_LOOP	R/W Word	Configured b				,
······		,	strap	, I .			

Ox2B	VOUT_MIN	R/W Word	Configured by pin- strap		0.5	5.0	V
0x33	FREQUENCY_SWITCH	R/W Word	0x01C2 450.00		450	900	kHz
0x35	VIN_ON	R/W Word	0xF016 5.50		5.5	15	V
0x36	VIN_OFF	R/W Word	0xF012			15	V
0x37	INTERLEAVE	R/W Word	0/1012	1.00	4.5	10	
0x38	IOUT_CAL_GAIN	R/W Word	Unit Specifi	C			
0x39	IOUT_CAL_OFFSET (Phase 0)	R/W Word	Unit Specifi				
0x39	IOUT_CAL_OFFSET (Phase 1)	R/W Word	Unit Specifi				
0x39	IOUT_CAL_OFFSET (Phase 2)	R/W Word	Unit Specifi				
0x39	IOUT_CAL_OFFSET (Phase 3)	R/W Word	Unit Specifi				
0x40	VOUT_OV_FAULT_LIMIT	R/W Word	0x024C	1.15			*
0,710			0/10210	1110			Vout
0x41	VOUT_OV_FAULT_RESPONSE	R/W Byte	OxBF				
0x42		R/W Word	0x0233	1.10			*
0/112			0.10200				Vout
0x43	VOUT_UV_WARN_LIMIT	R/W Word	0x01CC	0.90			*
		,					Vout
0x44	VOUT_UV_FAULT_LIMIT	R/W Word	0x01B3	0.85			*
		-					Vout
0x45	VOUT_UV_FAULT_RESPONSE	R/W Byte	OxBF				
0x46	IOUT_OC_FAULT_LIMIT (Phase	R/W Word	0xF0D0	52.00	8	52	А
	0)						
0x46	IOUT_OC_FAULT_LIMIT (Phase	R/W Word	0xF0D0	52.00	8	52	А
0x46	1) IOUT_OC_FAULT_LIMIT (Phase	R/W Word	0xF0D0	52.00	8	52	•
UX46	-	R/W WOID	UXFUDU	52.00	0	52	А
0x46	2) IOUT_OC_FAULT_LIMIT (Phase	R/W Word	0xF0D0	52.00	8	52	A
UX46	3)	R/W WOID	UXFUDU	52.00	0	52	A
0x47	IOUT_OC_FAULT_RESPONSE	R/W Byte	OxBF				
0x47 0x4A	IOUT_OC_WARN_LIMIT (Phase	R/W Word	0xF0A0	40.00	8	52	Α
UX4A	0)	K/W WOIG	UXFUAU	40.00	0	52	A
0x4A	IOUT_OC_WARN_LIMIT (Phase	R/W Word	0xF0A0	40.00	8	52	А
0x4A	IOUT_OC_WARN_LIMIT (Phase	R/W Word	0xF0A0	40.00	8	52	A
0,44		K/W WOIG	UXIUAU	40.00	0	52	~
0x4A	IOUT OC WARN LIMIT (Phase	R/W Word	0xF0A0	40.00	8	52	A
0,44	3)	K/W WOIG	UXIUAU	40.00	0	52	~
0x4F	OT_FAULT_LIMIT (Phase 0)	R/W Word	0x0087	135.00	0	150	ംറ
0x4F	OT_FAULT_LIMIT (Phase 1)	R/W Word	0x0087	135.00	0	150	°C
0x4F	OT_FAULT_LIMIT (Phase 2)	R/W Word	0x0087	135.00	0	150	°C
0x4F 0x4F	OT_FAULT_LIMIT (Phase 3)	R/W Word	0x0087 0x0087	135.00	0	150	°C
0x4r 0x50	OT_FAULT_LIMIT (FIIdse 3)	R/W Byte	0x0087 0xBF	133.00	0	130	
0x50	OT_WARN_LIMIT (Phase 0)	R/W Word	0x07D	125.00	0	150	°C
0x51	OT_WARN_LIMIT (Phase 1)	R/W Word	0x007D 0x007D	125.00	0	150	°C
0x51	OT_WARN_LIMIT (Phase 2)	R/W Word	0x007D 0x007D	125.00	0	150	°C
0x51 0x51	· · · · · ·	R/W Word	0x007D 0x007D		0	150	°C
0x51 0x55	OT_WARN_LIMIT (Phase 3) VIN_OV_FAULT_LIMIT	R/W Word	0x007D 0x0010	125.00	6	16	V
0x55 0x56	VIN_OV_FAULT_RESPONSE		OxBF	10.00	0	10	v
0x56 0x58		R/W Byte	OxF016	5.50	4	11.25	V
	VIN_UV_WARN_LIMIT (Phase 0)	R/W Word		3.30	4	11.25	
0x58	VIN_UV_WARN_LIMIT (Phase	R/W Word	0xF016	5.50	4	11.25	V
	1 1 1		1		1		
0x58	1) VIN_UV_WARN_LIMIT (Phase	R/W Word	0xF016	5.50	4	11.25	V

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0x58	VIN_UV_WARN_LIMIT (Phase	R/W Word	0xF016	5.50	4	11.25	V
0x60	3) TON DELAY	R/W Word	0xF814	10.00	0	127.5	ms
0x61	TON_RISE	R/W Word	0xF028	10.00	0	31.75	ms
0x62	TON_MAX_FAULT_LIMIT	R/W Word	0xF800	0.00	Ű	01.70	ms
0x63	TON_MAX_FAULT_RESPONSE	R/W Byte	Ox3B	0.00			
0x64	TOFF_DELAY	R/W Word	0xF800	0.00	0	127.5	ms
0x65	TOFF_FALL	R/W Word	0xF002	0.50	0	31.75	ms
0x78	STATUS_BYTE (Phase 0)	Read Byte	0,	0.00	Ū	0.00	
0x78	STATUS_BYTE (Phase 1)	Read Byte					
0x78	STATUS_BYTE (Phase 2)	Read Byte					
0x78	STATUS_BYTE (Phase 3)	Read Byte					
0x79	STATUS_WORD (Phase 0)	R/W Word					
0x79	STATUS_WORD (Phase 1)	R/W Word					
0x79	STATUS_WORD (Phase 2)	R/W Word					
0x79	STATUS_WORD (Phase 3)	R/W Word					
0x7A	STATUS_VOUT	R/W Byte					
0x7B	STATUS_IOUT (Phase 0)	R/W Byte					
0x7B	STATUS_IOUT (Phase 1)	R/W Byte					
0x7B	STATUS_IOUT (Phase 2)	R/W Byte					
0x7B	STATUS_IOUT (Phase 3)	R/W Byte					
0x7C	STATUS_INPUT (Phase 0)	R/W Byte					
0x7C	STATUS_INPUT (Phase 1)	R/W Byte					
0x7C	STATUS_INPUT (Phase 2)	R/W Byte					
0x7C	STATUS_INPUT (Phase 3)	R/W Byte					
0x7D	STATUS_TEMPERATURE (Phase	R/W Byte					
0/4/2	0)						
0x7D	STATUS_TEMPERATURE (Phase	R/W Byte					
0x7D	STATUS_TEMPERATURE (Phase 2)	R/W Byte					
0x7D	STATUS_TEMPERATURE (Phase 3)	R/W Byte					
0x7E	STATUS_CML (Phase 0)	R/W Byte					
0x7E	STATUS_CML (Phase 1)	R/W Byte					
0x7E	STATUS_CML (Phase 2)	R/W Byte					
0x7E	STATUS_CML (Phase 3)	R/W Byte					
0x7F	STATUS_OTHER	Read Byte					
0x80	STATUS_MFR_SPECIFIC (Phase 0)	R/W Byte					
0x80	STATUS_MFR_SPECIFIC (Phase 1)	R/W Byte					
0x80	STATUS_MFR_SPECIFIC (Phase 2)	R/W Byte					
0x80	STATUS_MFR_SPECIFIC (Phase 3)	R/W Byte					
0x88	READ_VIN (Phase 0)	Read Word					
0x88	READ_VIN (Phase 1)	Read Word					
0x88	READ_VIN (Phase 2)	Read Word					
0x88	READ_VIN (Phase 3)	Read Word					
0x8B	READ_VOUT (Phase 0)	Read Word					
0x8B	READ_VOUT (Phase 1)	Read Word					
0x8B	READ_VOUT (Phase 2)	Read Word					
0x8B	READ_VOUT (Phase 3)	Read Word					
0x8C	READ_IOUT (Phase 0)	Read Word					



0x8C	READ_IOUT (Phase 1)	Read Word					
0x8C	READ_IOUT (Phase 2)	Read Word					
0x8C	READ IOUT (Phase 3)	Read Word					
0x8C	READ IOUT (Per Rail)	Read Word					
0x8D	READ_TEMPERATURE_1 (Phase	Read Word					
	0)						
0x8D	READ_TEMPERATURE_1 (Phase	Read Word					
	1)						
0x8D	READ_TEMPERATURE_1 (Phase	Read Word					
	2)						
0x8D	READ_TEMPERATURE_1 (Phase	Read Word					
	3)						
0x8D	READ_TEMPERATURE_1 (Per	Read Word					
	Rail)						
0x98	PMBUS_REVISION	Read Byte					
0x99	MFR_ID	R/W Block3	Unit Specific				
0x9A	MFR_MODEL	R/W Block3	Unit Specific				
0x9B	MFR_REVISION	R/W Block3	Unit Specific				
0x9E	MFR_SERIAL	R/W Block3	Unit Specific				
0xAD	IC_DEVICE_ID	Read Block6					
0xAE	IC_DEVICE_REV	Read Block2					
OxB1	USER_DATA_01 (Phase 0xFF)	R/W Block5	0xC43FF82311				
0xD0	TELEMETRY_CONFIG	R/W Block6	0x0300030303	03			
0xDA	READ_ALL	Read Block14					
OxDB	STATUS_ALL	Read Block7					
0xDC	STATUS_PHASE (Phase 0xFF)	Read Word					
0xE3	PGOOD_CONFIG	R/W Word	0x006A				
0xE4	SYNC_CONFIG	R/W Byte	0xF0			ļ	
0xEC	STACK_CONFIG	R/W Word	0x0000				
0xED	MISC_OPTIONS	R/W Word	0x0000			ļ	
OxEE	PIN_DETECT_OVERRIDE	R/W Word	0x192D				
OxEF	SLAVE_ADDRESS	R/W Byte	0x14				
0xF0	NVM_CHECKSUM	Read Word					
0xF1	SIMULATE_FAULT	R/W Word	0x0000				

PMBus Command Details

OPERATION (0x01)

Description: Sets the desired PMBus enable and margin operations.

Bit	Function	Description	Value	Function	Description
7:6	Enable	Make the device enable or disable.	00	Immediate Off	Disable immediately without controlled ramp-down or sequencing.
			01	Soft Off	Disable by controlled ramp- down timings or sequencing.
			10	Enable	Enable device to the set voltage or margin state, using ramp up timings / sequencing.
5:4	Margin	Select between margin high/low states or nominal	00	Nominal	Operate at nominal output voltage.
		output.	01	Margin Low	Operate at margin low voltage set in VOUT_MARGIN_LOW.
			10	Margin High	Operate at margin high voltage set in VOUT_MARGIN_HIGH.
3:2	Act on Fault	Set 10b to act on fault or set to 01b to ignore fault.	01	Ignore Faults	Ignore Faults when in a margined state. The overvoltage/undervoltage warnings and faults are ignored and do not trigger shutdown or STATUS updates.
			10	Act on Faults	Act on Faults when in a margined state. The device will handle appropriate overvoltage/undervoltage warnings and faults and respond as programmed by the warning limit or fault response command.

ON_OFF_CONFIG (0x02)

Description: Configures how the device is controlled by the CTRL pin and the PMBus.

Bit	Function	Description	Value	Function	Description
4	Powerup Operation		0	Ignore CTRL pin or PMBus	Unit starts power conversion any time the input power is present regardless of the state of the CTRL pin.
			1	CTRL pin or PMBus	Device does not power up until commanded by the CTRL pin or OPERATION command.
3	PMBus Enable Mode	Controls how the device responds to the PMBus	0	Ignore PMBus command	Ignores the on/off portion of the OPERATION command.
		command OPERATION.	1	Use PMBus command	Device requires on by OPERATION command to enable the output voltage.



2	Enable Pin Mode	Controls how the device responds to the CTRL pin.	0	Ignore CTRL pin	Device ignores the CTRL pin.
			1	Use CTRL pin	Device requires the CTRL pin to be asserted to enable the output voltage.
1	Enable Pin Polarity	Polarity of the CTRL pin.	0	Active Low	CTRL pin will cause device to enable when driven low.
			1	Active High	CTRL pin will cause device to enable when driven high.
0	Disable Action	CTRL pin action when commanding the output to	0	Soft Off	Use the configured turn off delay and fall time.
		turn off.	1	Immediate Off	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

CLEAR_FAULTS (0x03)

Description: Clears all fault status bits

PHASE (0x04)

Description: Used to configure, control, and monitor individual phases. The phase configuration needs to be established before any phase-dependent command can be successfully excuted.

Bit	Description	Format
7:0	Selects a specific phase on a multi-phase output rail. Listed values for phase selection: 0x00 PHASE, 0X01 PHASE, 0x02 PHASE, 0X03 and 0XFF TOTAL PHASE (all phases as a single entity).	Integer Unsigned

WRITE_PROTECT (0x10)

Description: The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation.

Bit	Description	Value	Function	Description
7:0		0x80	Disable all writes	Disable all writes except to the WRITE_PROTECT command.
		0x40	Enable operation	Disable all writes except to the WRITE_PROTECT and OPERATION commands.
		0x20	Enable control and Vout commands	Disable all writes except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG and VOUT_COMMAND commands.
		0x00	Enable all commands	Enable writes to all commands.

STORE_USER_ALL (0x15)

Addressing: Phase Description: Commands the device to copy the entire contents of the operating memory to the matching locations in the non-volatile user store memory.

RESTORE_USER_ALL (0x16)

Addressing: Phase

Description: Commands the device to copy the entire contents of the non-volatile User Store Memory to the matching locations in the operating memory.

CAPABILITY (0x19)

Description: This command provides a way for a host system to determine some key capabilities of a PMBus device.

Bit	Function	Description	Value	Function	Description
7	Packet Error Checking	Packet error checking.	0	Not Supported	Packet Error Checking not supported.
			1	Supported	Packet Error Checking is supported.
6:5	Maximum Bus Speed	Maximum bus speed.	00	100kHz	Maximum supported bus speed is 100 kHz.
			01	400kHz	Maximum supported bus speed is 400 kHz.
			10	1 MHz	Maximum supported bus speed is 1 MHz.
4	Smbalert	SMBALERT	0	No Smbalert	The device does not have a SMBALERT# pin and does not support the SMBus Alert Response protocol.
			1	Have Smbalert	The device does have a SMBALERT# pin and does support the SMBus Alert Response protocol.
3	Numeric Format	Numeric format.	0	LINEAR or DIRECT Format	Numeric data is in LINEAR or DIRECT format.
			1	IEEE Half Precision Floating Point Format	Numeric data is in IEEE half precision floating point format.
2	AVSBus Support	AVSBus support.	0	AVSBus Not Supported	AVSBus not supported.
			1	AVSBus Supported	AVSBus supported.

SMBALERT_MASK_VOUT (0x1B)

Status Registers: STATUS_VOUT (0x7A)

Description: SMBALERT_MASK bits for the STATUS_VOUT command. The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Vout OV		0	Pull SALERT	
	Fault		1	Ignore	
6	Vout OV		0	Pull SALERT	
	Warn		1	Ignore	
5			0	Pull SALERT	

	Vout UV Warn	1	Ignore	
4	Vout UV Fault	0	Pull SALERT	
		1	Ignore	
3	Vout	0	Pull SALERT	
	Min/Max Fault	1	Ignore	
2	Ton Max Fault	0	Pull SALERT	
		1	Ignore	

SMBALERT_MASK_IOUT (0x1B)

Status Registers: STATUS_IOUT (0x7B)

Description: SMBALERT_MASK bits for the STATUS_IOUT command. The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	lout OC Fault		0	Pull SALERT	
			1	Ignore	
5	lout OC Warn		0	Pull SALERT	
			1	Ignore	

SMBALERT_MASK_INPUT (0x1B)

Status Registers: STATUS_INPUT (0x7C)

Description: SMBALERT_MASK bits for the STATUS_INPUT command. The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Vin		0	Pull SALERT	
	Overvoltage Fault		1	Ignore	
5	Vin UV Warn		0	Pull SALERT	
			1	Ignore	
3	Low Vin Fault		0	Pull SALERT	
			1	Ignore	

SMBALERT_MASK_TEMPERATURE (0x1B)

Status Registers: STATUS_TEMPERATURE (0x7D)

Description: SMBALERT_MASK bits for the STATUS_TEMPERATURE command. The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Overtempera		0	Pull SALERT	
	ture Fault		1	Ignore	
6	Overtempera		0	Pull SALERT	
	ture Warn		1	Ignore	

SMBALERT_MASK_CML (0x1B)

Status Registers: STATUS_CML (0x7E)

Description: SMBALERT_MASK bits for the STATUS_CML command. The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7			0	Pull SALERT	

	Invalid Or Unsupported Command Received	1	Ignore	
6	Invalid Or	0	Pull SALERT	
	Unsupported Data Received	1	Ignore	
5	Packet Error	0	Pull SALERT	
	Check Failed	1	Ignore	
4	Memory Error	0	Pull SALERT	
		1	Ignore	
1	Other	0	Pull SALERT	
	Communicati on Fault	1	Ignore	

SMBALERT_MASK_MFR_SPECIFIC (0x1B)

Status Registers: STATUS_MFR_SPECIFIC (0x80)

Description: SMBALERT_MASK bits for the STATUS_MFR_SPECIFIC command. The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Power-On		0	Pull SALERT	
	Reset Fault		1	Ignore	
6	Power-On		0	Pull SALERT	
	Self-Check		1	Ignore	
3	Reset		0	Pull SALERT	
			1	Ignore	
2	BCX fault		0	Pull SALERT	
			1	Ignore	
1	Sync fault		0	Pull SALERT	
			1	Ignore	

VOUT_MODE (0x20)

Description: Controls how future VOUT-related commands parameters will be interpreted.

Bit	Function	Description	Format
4:0	Parameter	Five bit two's complement EXPONENT for the MANTISSA delivered as	Integer Signed
		the data bytes for VOUT_COMMAND in VOUT_LINEAR Mode.	

Bit	Function	Description	Value	Function	Description
7	Rel	Selection of Absolute or Relative data format.	1	Relative	Relative Data Format.
6:5	Mode	Selection of mode for representation of output voltage parameters.	00	Linear	Linear Mode Format.

VOUT_COMMAND (0x21)

Description: Sets the nominal value of the output voltage from 0.6V to 5V.

Bit	Description	Format	Unit
15:0	Sets the nominal value of the output voltage.	Vout	V
		Mode	
		Unsigned	
		(Exp = -9)	

VOUT_TRIM (0x22)

Description: Configures a fixed offset to be applied to the output voltage when enabled.

Bit	Description	Format	Unit
15:0	Sets VOUT trim value. The range is limited to +/-31 mV.	Vout	V
		Mode	
		Signed	
		(Exp = -9)	

VOUT_MAX (0x24)

Description: Configures the maximum allowed output voltage.

Bit	Description	Format	Unit
15:0	If the device is commanded to a Vout value higher than this level, the output	Vout	V
	voltage will be clamped to this level.	Mode	
		Unsigned	
		(Exp = -9)	

VOUT_MARGIN_HIGH (0x25)

Description: Configures the target for margin-up commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin high.	Vout	*
		Mode	Vout
		Unsigned	
		(Exp = -9)	

VOUT_MARGIN_LOW (0x26)

Description: Configures the target for margin-down commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin low.	Vout	*
		Mode	Vout
		Unsigned	
		(Exp = -9)	

VOUT_TRANSITION_RATE (0x27)

Description: Sets the transition rate when changing output voltage.

Bit	Description	Format	Unit
15:0	Configures the transition time for margining and on-the-fly VOUT_COMMAND	Linear	V/ms
	changes.		

VOUT_SCALE_LOOP (0x29)

Description: Allows PMBus devices to map between the commanded voltage, and the voltage at the control circuit.

Bit	Description	Format
15:0	Choose scaling factor. Recommended value depending on Vout: 0.5 for Vout in	Linear
	range 0.5 to 1.5 V 0.25 for Vout in range 1 to 3 V 0.125 for Vout in range 2 to 6 V	

VOUT_MIN (0x2B)

Description: Configures the minimum allowed output voltage.

Bit	Description	Format	Unit



15:0	If the device is commanded to a Vout value lower than this level, the output voltage	Vout	V
	will be clamped to this level.	Mode	
		Unsigned	
		(Exp = -9)	

FREQUENCY_SWITCH (0x33)

Description: Controls the switching frequency.

Bit	Description	Format	Unit
15:0	Sets the switching frequency in kHz. The specified range is 450 - 900 kHz. The effective switching frequency is limited to a limited set of values: 450 kHz, 550 kHz, 650 kHz, 750 kHz, 900 kHz	Linear	kHz

VIN_ON (0x35)

Description: Input voltage must be above this level before the output can be enabled.

Bit	Description	Format	Unit
15:0	Sets the VIN ON threshold in 0.25 V steps in the range 5.5 - 15 V.	Linear	V

VIN_OFF (0x36)

Description: Sets the value of the PVIN input voltage, in Volts, at which the unit should stop power conversion.

Bit	Description	Format	Unit
15:0	Sets the VIN OFF threshold in 0.25 V steps. The specified range is 2.25 - 18.25 V.	Linear	V

INTERLEAVE (0x37)

Description: Configures the phase offset with respect to a common SYNC clock.

Bit	Function	Description	Format
11:8	Group ID Number	Value 0-15. Sets an ID number to a group of interleaved rails.	Integer Unsigned
7:4	Number in Group	Value 1 to 4. Sets the number of phases positions and the phase shift for each value of ORDER.	Integer Unsigned
3:0	Order within the group	Value 0 to NUM_GROUP - 1. Each value of ORDER adds a phase shift equal to 360° / NUM_GROUP.	Integer Unsigned

IOUT_CAL_GAIN (0x38)

Description: Sets the current sense resistance.

Bit	Description	Format	Unit
15:0	Sets the effective impedance for current sensing at +25°C.	Linear	mΩ

IOUT_CAL_OFFSET (0x39)

Addressing: Phase

Description: Sets the current-sense offset.

Bit	Description	Format	Unit
15:0	Sets an offset to IOUT readings. Use to compensate for delayed measurements of	Linear	А
	current ramp.		

VOUT_OV_FAULT_LIMIT (0x40)

Description: Sets the overvoltage fault threshold relative to the current VOUT_COMMAND.

Bit Descri	ption F	Format	Unit
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15:0	Sets the VOUT overvoltage fault threshold, which is a fixed percentage of the current	Vout	*
	output voltage target.	Mode	Vout
		Unsigned	
		(Exp = -9)	

VOUT_OV_FAULT_RESPONSE (0x41) Description: Sets the VOUT OV fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the	00	Ignore Fault	The PMBus device continues operation without interruption.
		device pulls SALERT low and sets the related fault bit in the status registers.	01	Shutdown After Delay	The PMBus device continues operation for the delay time specified by bits [2:0].
			10	Shutdown Immediately	The device shuts down immediately.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.



			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output overvoltage delay time for respond after delay and HICCUP.	0	0	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			1	1	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			2	2	Shutdown delay of 3 PWM_CLK, HICCUP equal to 2 times TON_RISE.
			3	3	Shutdown delay of 3 PWM_CLK, HICCUP equal to 3 times TON_RISE.
			4	4	Shutdown delay of 3 PWM_CLK, HICCUP equal to 4 times TON_RISE.
			5	5	Shutdown delay of 7 PWM_CLK, HICCUP equal to 5 times TON_RISE.
			6	6	Shutdown delay of 7 PWM_CLK, HICCUP equal to 6 times TON_RISE.
			7	7	Shutdown delay of 7 PWM_CLK, HICCUP equal to 7 times TON_RISE.

VOUT_OV_WARN_LIMIT (0x42) Description: Sets the overvoltage warning threshold relative to the current VOUT_COMMAND.

Bit	Description	Format	Unit
15:0	Sets the VOUT overvoltage warning threshold, which is a fixed percentage of the	Vout	*
	current output voltage target.	Mode	Vout
		Unsigned	
		(Exp = -9)	

VOUT_UV_WARN_LIMIT (0x43)

Description: Sets the undervoltage warning threshold relative to the current VOUT_COMMAND.

Bit	Description	Format	Unit
15:0	Sets the VOUT undervoltage warning threshold, which is a fixed percentage of the	Vout	*
	current output voltage target.	Mode	Vout
		Unsigned	
		(Exp = -9)	

VOUT_UV_FAULT_LIMIT (0x44)

Description: Sets the undervoltage fault threshold relative to the current VOUT_COMMAND.

Bit	Description	Format	Unit
15:0	Sets the VOUT undervoltage fault threshold, which is a fixed percentage of the	Vout	*
	current output voltage target.	Mode	Vout
		Unsigned	
		(Exp = -9)	

VOUT_UV_FAULT_RESPONSE (0x45)

Description: Sets the VOUT UV fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the	00	Ignore Fault	The PMBus device continues operation without interruption.
		device pulls SALERT low and sets the related fault bit in the status registers.	01	Shutdown After Delay	The PMBus device continues operation for the delay time specified by bits [2:0].
			10	Shutdown Immediately	The device shuts down immediately.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.

TECHNICAL REFERENCE DOC PMBus general details: BMR 473 1X01/001



			100	Potr (Atimor	The PMP is device attempts
			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output undervoltage delay time for respond after delay and HICCUP.	0	0	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			1	1	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			2	2	Shutdown delay of 3 PWM_CLK, HICCUP equal to 2 times TON_RISE.
			3	3	Shutdown delay of 3 PWM_CLK, HICCUP equal to 3 times TON_RISE.
			4	4	Shutdown delay of 3 PWM_CLK, HICCUP equal to 4 times TON_RISE.
			5	5	Shutdown delay of 7 PWM_CLK, HICCUP equal to 5 times TON_RISE.
			6	6	Shutdown delay of 7 PWM_CLK, HICCUP equal to 6 times TON_RISE.
			7	7	Shutdown delay of 7 PWM_CLK, HICCUP equal to 7 times TON_RISE.

IOUT_OC_FAULT_LIMIT (0x46)

Addressing: Phase

Description: Sets the output over-current peak limit for per phase.

Bit	Description	Format	Unit
15:0	Sets the IOUT overcurrent peak fault threshold for each phase with PHASE command set to 0x00 - 0x03. Sets the IOUT overcurrent peak fault threshold for all phases with PHASE command set to 0xFF. The analog hardware supports values from 8 A to 62 A in 2 A steps. Adjustable range from 0-62A. Linear format with LSB=0.25A. Note that the effective current limit of the multi-phase stack is equal to the lowest IOUT_OC_FAULT_LIMIT setting times the number of phases in the stack.	Linear	A

IOUT_OC_FAULT_RESPONSE (0x47) Description: Sets the output total over-current fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the	00	Ignore Fault	The PMBus device continues operation without interruption.
		device pulls SALERT low and sets the related fault bit in the status registers.	10	Shutdown After Delay	The PMBus device continues operation for the delay time specified by bits [2:0].
			11	Shutdown Immediately	The device shuts down immediately.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.

TECHNICAL REFERENCE DOC PMBus general details: BMR 473 1X01/001



			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output overcurrent delay time for respond after delay and HICCUP.	0	0	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			1	1	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.
			2	2	Shutdown delay of 3 PWM_CLK, HICCUP equal to 2 times TON_RISE.
			3	3	Shutdown delay of 3 PWM_CLK, HICCUP equal to 3 times TON_RISE.
			4	4	Shutdown delay of 3 PWM_CLK, HICCUP equal to 4 times TON_RISE.
			5	5	Shutdown delay of 7 PWM_CLK, HICCUP equal to 5 times TON_RISE.
			6	6	Shutdown delay of 7 PWM_CLK, HICCUP equal to 6 times TON_RISE.
			7	7	Shutdown delay of 7 PWM_CLK, HICCUP equal to 7 times TON_RISE.

IOUT_OC_WARN_LIMIT (0x4A)

Addressing: Phase

Description: Sets the value of the output current that causes the overcurrent detector to indicate an overcurrent warning condition. IOUT_OC_WARN_LIMIT is a phased command. Each phase will report an output current overcurrent warning independently.

Bit	Description	Format	Unit
15:0	Sets the value of the overcurrent warning threshold for each phase with PHASE	Linear	А
	command set to 0x00 - 0x03. The analog hardware supports values from 8 A to 62 A		
	in 2 A steps. Adjustable range from 0-62A. Linear format with LSB=0.25A.		

OT_FAULT_LIMIT (0x4F)

Addressing: Phase

Description: Sets the over-temperature fault limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature fault threshold. Adjustable range from 0-160°C in 1°C	Linear	°C
	steps. Setting 255°C value will disable the over-temperature fault limit without		
	disabling the on-die Bandgap thermal shutdown.		

OT_FAULT_RESPONSE (0x50)

Description: Sets the over-temperature fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the	00	Ignore Fault	The PMBus device continues operation without interruption.
		device pulls SALERT low and sets the related fault bit in the status registers.	01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
			11	Disable, Resume When OK	The device shuts down (disables the output) until the temperature is below the over-temperature warn limit, then restarts according to the retry setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.



	001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:] along with the delay time unit specified for that particular fault.
	010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
	011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
	100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
	101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
	110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
	111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.



2:0	Retry Time and Delay Time	Sets the over-temperature delay time for respond after delay and HICCUP.	0	10 ms	Shutdown delay of 10 ms, HICCUP equal to TON_RISE, HICCUP delay equal to TON_RISE.
			1	1 ms	
			2	2 ms	
			3	3 ms	
			4	4 ms	
			5	5 ms	
			6	6 ms	
			7	7 ms	

OT_WARN_LIMIT (0x51)

Addressing: Phase

Description: Sets the over-temperature warn limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature warning threshold. Adjustable range from 0-160°C in 1°C	Linear	°C
	steps. Setting 255°C value will disable disable the OT_WARN_LIMIT function.		

VIN_OV_FAULT_LIMIT (0x55)

Description: Sets the input over-voltage fault limit.

Bit	Description	Format	Unit
15:0	Sets the VIN overvoltage fault threshold. Values 4 - 20 V in 1 V steps.	Linear	V

VIN_OV_FAULT_RESPONSE (0x56) Description: Sets the input over-voltage fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the	00	Ignore Fault	The PMBus device continues operation without interruption.
		device pulls SALERT low and sets the related fault bit in the status registers.	01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.



	1		I		
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			101	Retry 5 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			110	Retry 6 times	The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay Time	Sets the output over-voltage delay time for respond after delay and HICCUP.	0	0	Shutdown delay of 1 PWM_CLK, HICCUP equal to TON_RISE.

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	1	1	Shutdown delay of 1
			PWM_CLK, HICCUP equal to
			TON_RISE.
	2	2	Shutdown delay of 3
			PWM_CLK, HICCUP equal to 2
			times TON_RISE.
	3	3	Shutdown delay of 3
			PWM_CLK, HICCUP equal to 3
			times TON_RISE.
	4	4	Shutdown delay of 3
			PWM_CLK, HICCUP equal to 4
			times TON_RISE.
	5	5	Shutdown delay of 7
			PWM_CLK, HICCUP equal to 5
			times TON_RISE.
	6	6	Shutdown delay of 7
			PWM_CLK, HICCUP equal to 6
			times TON_RISE.
	7	7	Shutdown delay of 7
			PWM_CLK, HICCUP equal to 7
			times TON_RISE.

VIN_UV_WARN_LIMIT (0x58)

Addressing: Phase

Description: Sets the input under-voltage warning limit.

Bit	Description	Format	Unit
15:0	Sets the VIN undervoltage warning threshold.	Linear	V

TON_DELAY (0x60)

Description: Sets the turn-on delay time

Bit	Description	Format	Unit
15:0	Sets the time, from when a start condition is received (as programmed by the	Linear	ms
	ON_OFF_CONFIG command) until the output voltage starts to rise.		

TON_RISE (0x61)

Description: Sets the turn-on ramp-up time.

Bit	Description	Format	Unit
15:0	Sets the rise time of VOUT after ENABLE and On Delay. The time can range from 0 ms	Linear	ms
	to 31.75 ms in 0.25 ms steps. Values less than 0.5 ms are supported as 0.5 ms.		

TON_MAX_FAULT_LIMIT (0x62)

Description: Sets an upper limit on how long the unit can attempt to power up the output without reaching the target voltage.

Bit	Description	Format	Unit
15:0	Sets the upper limit time. The time can range from 0 ms to 127 ms in 0.5 ms steps.	Linear	ms
	Value 0 ms disables the TON_MAX functionality.		

TON_MAX_FAULT_RESPONSE (0x63)

Description: Instructs the device on what action to take in response to TON_MAX fault.

	Bit	Function	Description	Value	Function	Description
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7:6	Response	Describes the device	00	Ignore Fault	The PMBus device continues
7.0	Kesponse	interruption operation. For all modes set by bits [7:6], the	00	Ignore Fault	operation without interruption.
		device pulls SALERT low and sets the related fault bit in the status registers.	01	Perform Retries while Operating	The PMBus device continues operation for the delay time specified by bits [2:0] and the delay time unit specified for that particular fault. If the fault condition is still present at the end of the delay time, the unit responds as programmed in the Retry Setting (bits [5:3]).
			10	Disable and Retry	The device shuts down (disables the output) and responds according to the retry setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			001	Retry Once	The PMBus device attempts to restart 1 time. If the device fails to restart, it disables the output and remains off until the fault is cleared as described in Section 10.7. The time between the start of each attempt to restart is set by the value in bits [2:] along with the delay time unit specified for that particular fault.
			010	Retry Twice	The PMBus device attempts to restart 2 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			011	Retry 3 times	The PMBus device attempts to restart 3 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			100	Retry 4 times	The PMBus device attempts to restart 4 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.



			101	Retry 5 times Retry 6 times	The PMBus device attempts to restart 5 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device. The PMBus device attempts to restart 6 times. If the device fails to restart, it disables the output and remains off until either: a reset signal is asserted, or a bias power is removed from the device.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time and Delay	Sets the output over-voltage delay time for respond after	0	1 ms	Shutdown delay of 1 ms, HICCUP equal to TON_RISE.
	Time	delay and HICCUP.	1	1 ms	Shutdown delay of 1 ms, HICCUP equal to 1 times TON_RISE.
			2	2 ms	Shutdown delay of 2 ms, HICCUP equal to 2 times TON_RISE.
			3	3 ms	Shutdown delay of 3 ms, HICCUP equal to 3 times TON_RISE.
			4	4 ms	Shutdown delay of 4 ms, HICCUP equal to 4 times TON_RISE.
			5	5 ms	Shutdown delay of 5 ms, HICCUP equal to 5 times TON_RISE.
			6	6 ms	Shutdown delay of 6 ms, HICCUP equal to 6 times TON_RISE.
			7	7 ms	Shutdown delay of 7 ms, HICCUP equal to 7 times TON_RISE.

TOFF_DELAY (0x64)

Description: Sets the turn-off delay.

Bit	Description	Format	Unit
15:0	Sets the delay time from DISABLE to start of the fall of the output voltage. Normally the time can range from 0 ms up to 127.5 ms in 0.5 ms steps. An internal delay of up to 50 µs will be added to TOFF_DELAY, even if TOFF_DELAY is equal to 0 ms.	Linear	ms

TOFF_FALL (0x65)

Description: Sets the turn-off ramp-down time.

Bit	Description	Format	Unit
15:0	Sets the fall time for VOUT after DISABLE and Off Delay. The time can range from 0 ms	Linear	ms
	to 31.75 ms in 0.25 ms steps. Values less than 0.5 ms will be implemented as 0.5 ms.		

STATUS_BYTE (0x78)

Addressing: Phase

Description: Returns a brief fault/warning status byte. Setting and clearing of supported bits must be done in the individual status registers. For example, Clearing VOUT_OVF in STATUS_VOUT also clears VOUT_OV in STATUS_BYTE.

Bit	Function	Description	Value	Description
7	Busy	A fault was declared because the device was	0	No fault
		busy and unable to respond.	1	Fault
6	Off	This bit is asserted if the unit is not providing	0	No fault
		power to the output due to not being enabled,	1	Fault
		i.e. not set when output shut down due to fault.		
5	Vout Overvoltage	An output overvoltage fault has occurred.	0	No fault
	Fault		1	Fault
4	lout Overcurrent	An output overcurrent fault has occurred.	0	No fault
	Fault		1	Fault
3	Vin Undervoltage	An input undervoltage fault has occurred.	0	No fault
	Fault		1	Fault
2	Temperature	A temperature fault or warning has occurred.	0	No fault
			1	Fault
1	Communication/Lo	A communications, memory or logic fault has	0	No fault
	gic	occurred.	1	Fault

STATUS_WORD (0x79)

Addressing: Phase

Description: Returns an extended fault/warning status byte. Writing 0080h to STATUS_WORD will clear the BUSY bit, if set. Writing 0180h to STATUS_WORD will clear both the BUSY bit and UNKNOWN bit, if set.

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has	0	No fault
		occurred.	1	Fault
14	lout	An output current fault or warning has	0	No Fault.
		occurred.	1	Fault.
13	Input	An input voltage, input current, or input power	0	No Fault.
		fault or warning has occurred.	1	Fault.
12	Mfr	A manufacturer specific fault or warning has	0	No Fault.
		occurred.	1	Fault.
11	Power-Good	The Power-Good signal, if present, is negated.	0	No Fault.
			1	Fault.
9	Other	An other fault has occurred.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was	0	No Fault.
		busy and unable to respond.	1	Fault.
6	Off	This bit is asserted if the unit is not providing	0	No Fault.
		power to the output due to not being enabled, i.e. not set when output shut down due to fault.	1	Fault.
5	Vout Overvoltage	An output overvoltage fault has occurred.	0	No Fault.
	Fault		1	Fault.
4	lout Overcurrent	An output overcurrent fault has occurred.	0	No Fault.
	Fault		1	Fault.
3	Vin Undervoltage	An input undervoltage fault has occurred.	0	No Fault.
	Fault		1	Fault.



2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Lo	A communications, memory or logic fault has	0	No fault.
	gic	occurred.	1	Fault.

STATUS_VOUT (0x7A)

Description: Returns Vout-related fault/warning status bits. All supported bits can be cleared either by CLEAR_FAULTS, or individually by writing 1b to the STATUS_VOUT (0x7A) register in their position.

Bit	Function	Description	Value	Description
7	Vout OV Fault	Latched flag of Vout over-voltage fault has	0	No Fault.
		occurred.	1	Fault.
6	Vout OV Warn	Latched flag of Vout over-voltage warning has	0	No Fault.
		occurred.	1	Fault.
5	Vout UV Warn	Latched flag of Vout under-voltage warning	0	No Fault.
		has occurred .	1	Fault.
4	Vout UV Fault	Latched flag of Vout under-voltage fault has	0	No Fault.
		occurred.	1	Fault.
3	Vout Min/Max Fault	Latched flag of Vout min/max fault or warning	0	No Fault.
		has occurred .	1	Fault.
2	Ton Max Fault	Latched flag of Ton max fault or warning has	0	No Fault.
		occurred .	1	Fault.

STATUS_IOUT (0x7B)

Addressing: Phase

Description: Returns lout-related fault/warning status bits. All supported bits can be cleared either by CLEAR_FAULTS, or individually by writing 1b to the STATUS_IOUT (0x7B) register in their position.

Bit	Function	Description	Value	Description
7	lout OC Fault	Latched flag of lout over-current fault has	0	No Fault.
		occurred.	1	Fault.
5	lout OC Warn	Latched flag of lout over-current warning has	0	No Fault.
		occurred.	1	Fault.
4	lout UC Fault	Latched flag of lout under-current fault has	0	No Fault.
		occurred.	1	Fault.
3	Current Share Fault	Latched flag of current share fault has	0	No Fault.
		occurred.	1	Fault.

STATUS_INPUT (0x7C)

Addressing: Phase

Description: Returns VIN/IIN-related fault/warning status bits. All supported bits can cleared either by CLEAR_FAULTS, or individually by writing 1b to the STATUS_INPUT register (0x7C) in their position.

Bit	Function	Description	Value	Description
7	Vin Overvoltage	Latched flag of input over-voltage fault has	0	No Fault.
	Fault	occurred.	1	Fault.
6	Vin OV Warn	Latched flag of input over-voltage warning has	0	No Fault.
		occurred.	1	Fault.
5	Vin UV Warn	Latched flag of input under-voltage warning	0	No Fault.
		has occurred.	1	Fault.
4	Vin UV Fault	Latched flag of input under-voltage fault has	0	No Fault.
		occurred.	1	Fault.
3	Low Vin Fault	Latched flag of shutdown unit due to	0	No Fault.
		insufficient VIN .	1	Fault.
2	lin Oc Fault		0	No Fault.



		Latched flag of input over-current fault has occurred.	1	Fault.
1	lin Oc Warn	Latched flag of input over-current warning has	0	No Fault.
		occurred.	1	Fault.
0	Pin Op Warn	Latched flag of input over-power warning has	0	No Fault.
		occurred.	1	Fault.

STATUS_TEMPERATURE (0x7D)

Addressing: Phase

Description: Returns the temperature-related fault/warning status bits. All supported bits can be cleared either by CLEAR_FAULTS, or individually by writing 1b to the STATUS_TEMPERATURE (0x7D) register in their position.

Bit	Function	Description	Value	Description
7	Overtemperature	Latched flag of over-temperature fault has	0	No Fault.
	Fault	occurred.	1	Fault.
6	Overtemperature	Latched flag of over-temperature warn has	0	No Fault.
	Warn	occurred.	1	Fault.

STATUS_CML (0x7E)

Addressing: Phase

Description: Returns Communication/Logic/Memory-related fault/warning status bits. All supported bits can be cleared either by CLEAR_FAULTS, or individually by writing 1b to the STATUS_CML (0x7E) register in their position.

Bit	Function	Description	Value	Description
7	Invalid Or	Invalid Or Unsupported Command Received.	0	No Invalid Command
	Unsupported			Received.
	Command		1	Invalid Command
	Received			Received.
6	Invalid Or	Invalid Or Unsupported Data Received.	0	No Invalid Data
	Unsupported Data			Received.
	Received		1	Invalid Data Received.
5	Packet Error Check	Packet Error Check (PEC) Failed.	0	No Failure.
	Failed		1	Failure.
4	Memory Error	A memory error was detected.	0	No Fault.
			1	Fault.
1	Other	A PMBus command tried to write to a read-only	0	No Fault.
	Communication	or protected command, or a communication	1	Fault.
	Fault	fault other than the ones listed in this table has		
		occurred.		

STATUS_OTHER (0x7F)

Description: Returns one data byte with information not specified in the other STATUS_BYTE.

Bit	Description	Value	Description
0	The device was the first to assert SMBALERT.	1	First to assert SMBALERT.
		0	The device was not the first to assert SMBALERT.
			This could mean either
			that the SMBALERT signal is not asserted
			(or has since been
			cleared), or that it is
			asserted, but this device was not the first
			on the bus to assert it.

STATUS_MFR_SPECIFIC (0x80)

Addressing: Phase

Description: Returns manufacturer specific status information. All supported bits may be cleared either by CLEAR_FAULTS, or individually by writing 1b to the STATUS_MFR_SPECIFIC (0x80) register in their position.

Bit	Function	Description	Value	Description
7	Power-On Reset	Power-on reset fault has occurred.	0	No Fault.
	Fault		1	Fault.
6	Power-On Self-	Showing the status of the Power-On Self-Check.	0	Power On Self-Check is
	Check			complete. All
				expected BCX slaves
				have responded.
			1	Power-On Self-Check is
				in progress. One or
				more BCX slaves have
				not responded.
3	Reset	VOUT_COMMAND has been reset without	0	RESET_VOUT event has
		PMBus commands.		not occurred.
			1	RESET_VOUT event has
				occurred.
2	BCX fault	Back-channel communications fault has	0	No Fault.
		occurred.	1	Fault.
1	Sync fault	Sync fault has occurred.	0	No Fault.
			1	Fault.

READ_VIN (0x88)

Addressing: Phase Description: Returns the measured input voltage.

Bit	Description	Format	Unit
15:0	Returns the input voltage reading. When PHASE = FFh, READ_VIN returns the input	Linear	V
	voltage of the master device.		

READ_VOUT (0x8B)

Addressing: Phase

Description: Returns the measured output voltage.

Bit	Description	Format	Unit
15:0	Returns the output voltage reading.	Vout	V
		Mode	
		Unsigned	
		(Exp = -9)	

READ_IOUT (0x8C)

Addressing: Phase

Description: Returns the measured output current.

Bit	Description		Format	Unit
15:0	Returns the output current reading. When PH	IASE = FFh, READ_IOUT returns the total	Linear	А
	current for the stack of devices.			

READ_TEMPERATURE_1 (0x8D)

Addressing: Phase

Description: Returns the maximum power stage temperature.



Bit	Description	Format	Unit
15:0	When PHASE = FFh, READ_TEMPERATURE_1 returns the temperature of the hottest of	Linear	°C
	device in the stack of devices.		

PMBUS_REVISION (0x98)

Description: Returns the PMBus revision number for this device.

Bit	Function	Description	Value	Function	Description
7:4	Part I Revision	Part I Revision.	0011	1.3	Part I Revision 1.3.
3:0	Part II	Part II Revision.	0011	1.3	Part II Revision 1.3.
	Revision				

MFR_ID (0x99)

Description: Sets the manufacturer ID String.

Bit	Description	Format
23:0	Maximum of 3 bytes.	Byte Array

MFR_MODEL (0x9A)

Description: Sets the manufacturer model string.

Bit	Description	Format
23:0	Maximum of 3 bytes.	Byte Array

MFR_REVISION (0x9B)

Description: Sets the manufacturer revision string.

Bit	Description	Format
23:0	Maximum of 3 bytes.	Byte Array

MFR_SERIAL (0x9E)

Description: Sets the manufacturer serial number.

Bit	Description	Format
23:0	3-byte serial number assigned by manufacturer.	Byte Array

IC_DEVICE_ID (0xAD)

Description: Reports identification information.

Bit	Description	Format
47:0	Reports identification information.	Byte Array

IC_DEVICE_REV (0xAE)

Description: Reports revision information.

Bit	Description	Format
15:0	Reports revision information.	Byte Array

USER_DATA_01 (0xB1)

Addressing: Phase

Description: Configures the control loop compensation settings.

Bit	Function	Description	Format
39:38	SEL_CZI High	High bits component of CZI scalar.	Byte Array
25:24	SEL_CZI Low	Low bits component of CZI scalar.	Byte Array



23:22	SEL_CZV High	High bits component of CZV sc			Byte Array
9:8	SEL_CZV Low	Low bits component of CZV sco	alar.		Byte Array
Bit	Function	Description	Value	Function	Description
37:33	CPI	Selects the value of current	00000	0 pF	
		loop filter capacitor.	00001	3.2 pF	
			00010	6.4 pF	
			00011	9.6 pF	
			00100	12.8 pF	
			00101	16 pF	
			00110	19.2 pF	
			00111	22.4 pF	
			01000	25.6 pF	
			01001	28.8 pF	
			01010	32 pF	
			01011	35.2 pF	
			01100	38.4 pF	
			01101	41.6 pF	
			01110	44.8 pF	
			01111	48 pF	
			10000	51.2 pF	
			10001	54.4 pF	
			10010	57.6 pF	
			10011	60.8 pF	
			10100	64 pF	
			10101	67.2 pF	
			10110	70.4 pF	
			10111	73.6 pF	
			11000	76.8 pF 80 pF	
			11001	83.2 pF	
			11010	86.4 pF	
			11100	89.6 pF	
			11100	92.8 pF	
			11110	96 pF	
			11111	99.2 pF	
32	CZI multiplier	Selects the value of current	0	1	
0Z		loop integrating capacitor multiplier.	1	2	
31:26	RVI	Selects the value of current	000000	0 kΩ	
		loop mid-band gain resistor.	000001	5 kΩ	
			000010	10 kΩ	
			000011	15 kΩ	
			000100	20 kΩ	
			000101	25 kΩ	
			000110	30 kΩ	
			000111	35 kΩ	
			001000	40 kΩ	
			001001	45 kΩ	
			001010	50 kΩ	
			001011	55 kΩ	
			001100	60 kΩ	
			001101	65 kΩ	
			001110	70 kΩ	
			001111	75 kΩ	

TECHNICAL REFERENCE DOC PMBus general details: BMR 473 1X01/001



[1			
			010000	80 kΩ	
			010001	85 kΩ	
			010010	90 kΩ	
			010011	95 kΩ	
			010100	100 kΩ	
			010101	105 kΩ	
			010110	110 kΩ	
			010111	115 kΩ	
			011000	120 kΩ	
			011001	125 kΩ	
			011010	130 kΩ	
			011011	135 kΩ	
			011100	140 kΩ	
			011100	140 kΩ	
			011110	150 kΩ	
			011111	155 kΩ	
			100000	160 kΩ	
			100001	165 kΩ	
			100010	170 kΩ	
			100011	175 kΩ	
			100100	180 kΩ	
			100101	185 kΩ	
			100110	190 kΩ	
			100111	195 kΩ	
			101000	200 kΩ	
			101001	205 kΩ	
			101010	210 kΩ	
			101010	215 kΩ	
			101100	210 kΩ	
			101100	225 kΩ	
			101110	223 kΩ	
			101110	230 kΩ	
			110000	240 kΩ	
			110001	245 kΩ	
			110010	250 kΩ	
			110011	255 kΩ	
			110100	260 kΩ	
			110101	265 kΩ	
			110110	270 kΩ	
			110111	275 kΩ	
			111000	280 kΩ	
			111001	285 kΩ	
			111010	290 kΩ	
			111011	295 kΩ	
			111100	300 kΩ	
			111101	305 kΩ	
			111110	310 kΩ	
			111111	315 kΩ	
21:17	CPV	Selects the value of voltage	00000	0 pF	
21.17		loop filter capacitor.	00000	6.25 pF	
			00001		
				12.5 pF	
			00011	18.75 pF	
			00100	25 pF	
			00101	31.25 pF	
			00110	37.5 pF	

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		1		
			00111	43.75 pF
			01000	50 pF
			01001	56.25 pF
			01010	62.5 pF
			01011	68.75 pF
			01100	75 pF
			01101	81.25 pF
			01110	87.5 pF
			01111	93.75 pF
			10000	100 pF
			10000	106.25 pF
			10010	
				112.5 pF
			10011	118.75 pF
			10100	125 pF
			10101	131.25 pF
			10110	137.5 pF
			10111	143.75 pF
			11000	150 pF
			11001	156.25 pF
			11010	162.5 pF
			11011	168.75 pF
			11100	175 pF
			11100	181.25 pF
			11110	187.5 pF
			11111	
15.10				193.75 pF
15:10	RVV	Selects the value of voltage	000000	0 κΩ
		loop mid-band gain resistor.	000001	5 κΩ
			000010	10 kΩ
			000011	15 kΩ
			000100	20 kΩ
			000101	25 kΩ
			000110	30 kΩ
			000111	35 kΩ
			001000	40 kΩ
			001001	45 kΩ
			001010	50 kΩ
			001011	55 kΩ
			001100	60 kΩ
			001101	65 kΩ
			001101	70 kΩ
			001110	75 kΩ
			010000	80 kΩ
			010001	85 kΩ
			010010	90 kΩ
			010011	95 kΩ
			010100	100 kΩ
			010101	105 kΩ
			010110	110 kΩ
			010111	115 kΩ
			011000	120 kΩ
			011001	125 kΩ
			011010	130 kΩ
			011010	135 kΩ
1			011100	140 kΩ
			011100	145 kΩ

TECHNICAL REFERENCE DOC PMBus general details: BMR 473 1X01/001



			011110	15010	
			011110	150 kΩ	
			011111	155 kΩ	
			100000	160 kΩ	
			100001	165 kΩ	
			100010	170 kΩ	
			100011	175 kΩ	
			100100	180 kΩ	
			100101	185 kΩ	
			100110	190 kΩ	
			100111	195 kΩ	
			101000	200 kΩ	
			101001	205 kΩ	
			101010	210 kΩ	
			101011	215 kΩ	
			101100	220 kΩ	
			101101	225 kΩ	
			101110	230 kΩ	
			101111	235 kΩ	
			110000	240 kΩ	
			110001	245 kΩ	
			110010	250 kΩ	
			110011	255 kΩ	
			110100	260 kΩ	
			110101	265 kΩ	
			110110	270 kΩ	
			110111	275 kΩ	
			111000	280 kΩ	
			111001	285 kΩ	
			111010	290 kΩ	
			111011	295 kΩ	
			111100	300 kΩ	
			111101	305 kΩ	
			111110	310 kΩ	
			111111	315 kΩ	
5:4	GMV	Selects the value of voltage	00	25 µS	
5.4	GIVIV	error transconductance.	00	25 μS 50 μS	
			10	100 μS	
			10		
1:0	GMI	Selects the value of current	00	200 µS 25 µS	
1.0	GIVII	error transconductance.	00		
		enormansconductance.		50 µ\$	
			10	100 µS	
			11	200 µS	

TELEMETRY_CONFIG (0xD0)

Description: Configures the priority and averaging for each channel of the internal telemetry system. The internal telemetry system shares a single ADC across each measurement. The priority setting allows the user to adjust the relative rate of measurement of each telemetry value. The ADC will first measure each value with a priority A value. With each pass through all priority A measurements, one priority B measurement will be taken. With each pass through all priority C measurement will be taken.

Bit	Function	Description	Value	Function	Description
31:30	READ_VIN	Assigns priority A-C to input	00	A priority	
	Priority	voltage telemetry.	01	B priority	
			10	C priority	

			11	Disable input voltage
				telemetry.
26:24	READ_VIN Rolling Avg	READ_VIN Rolling average of 2^N samples.	000	1 sample (N=0)
			001	2 samples (N=1)
			010	4 samples (N=2)
			011	8 samples (N=3)
			100	16 samples (N=4)
			101	32 samples (N=5)
23:22	READ_TEMPE	Assigns priority A-C to output	00	A priority
	RATURE_1	temperature telemetry. The	01	B priority
	Priority	temperature telemetry cannot be disabled because it is used for Over-temperature Protection.	10	C priority
18:16	READ_TEMPE RATURE_1	READ_TEMPERATURE_1 Rolling average of 2^N samples.	000	1 sample (N=0)
	Rolling Avg		001	2 samples (N=1)
			010	4 samples (N=2)
			011	8 samples (N=3)
			100	16 samples (N=4)
			101	32 samples (N=5)
15:14	READ_IOUT	Assigns priority A-C to output	00	A priority
	Priority	current telemetry.	01	B priority
			10	C priority
			11	Disable output current telemetry.
10:8	READ_IOUT Rolling Avg	READ_IOUT Rolling average of 2^N samples.	000	1 sample (N=0)
			001	2 samples (N=1)
			010	4 samples (N=2)
			011	8 samples (N=3)
			100	16 samples (N=4)
			101	32 samples (N=5)
7:6	READ_VOUT	Assigns priority A-C to output	00	A priority
	Priority	voltage telemetry.	01	B priority
			10	C priority

			11	Disable output voltage telemetry.	
2:0	READ_VOUT Rolling Avg	READ_VOUT Rolling average of 2^N samples.	000	1 sample (N=0)	
			001	2 samples (N=1)	
			010	4 samples (N=2)	
			011	8 samples (N=3)	
			100	16 samples (N=4)	
			101	32 samples (N=5)	

READ_ALL (0xDA)

Description: Returns a 14-byte block of STATUS_WORD and telemetry values. This can reduce bus utilization by combining multiple read functions into a single command.

Bit	Function	Description	Format	Unit
79:64	Read Vin	Returns the input voltage reading. When PHASE = FFh, READ_VIN returns the input voltage of the master device.	Linear	V
63:48	Read Temperature 1	When PHASE = FFh, READ_TEMPERATURE_1 returns the temperature of the hottest of device in the stack of devices.	Linear	°C
47:32	Read lout	Returns the output current reading. When PHASE = FFh, READ_IOUT returns the total current for the stack of devices.	Linear	A
31:16	Read Vout	Returns the output voltage reading.	Vout Mode Unsigned (Exp = -9)	V

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has		No fault
		occurred.	1	Fault
14	lout	An output current fault or warning has	0	No Fault.
		occurred.	1	Fault.
13	Input	An input voltage, input current, or input power	0	No Fault.
		fault or warning has occurred.	1	Fault.
12	Mfr	A manufacturer specific fault or warning has	0	No Fault.
		occurred.	1	Fault.
11	Power-Good	The Power-Good signal, if present, is negated.	0	No Fault.
			1	Fault.
9	Other	her An other fault has occurred.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was	0	No Fault.
		busy and unable to respond.		Fault.
6	Off	This bit is asserted if the unit is not providing	0	No Fault.
		power to the output due to not being enabled,	1	Fault.
		i.e. not set when output shut down due to fault.		
5	Vout Overvoltage	An output overvoltage fault has occurred.	0	No Fault.
	Fault		1	Fault.
4		An output overcurrent fault has occurred.	0	No Fault.



	Iout Overcurrent Fault		1	Fault.
3	Vin Undervoltage	An input undervoltage fault has occurred.	0	No Fault.
	Fault		1	Fault.
2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Lo A communications, memory or logic fault has		0	No fault.
	gic	occurred.	1	Fault.

STATUS_ALL (0xDB) Description: Returns 7-byte block of STATUS command codes. This can reduce bus utilization to read multiple faults.

Bit	Function	Description	Value	Description
55	Power-On Reset	Power-on reset fault has occurred.	0	No Fault.
	Fault		1	Fault.
54	Power-On Self-	Showing the status of the Power-On Self-Check.	0	Power On Self-Check is
	Check			complete. All
				expected BCX slaves
				have responded.
			1	Power-On Self-Check is
				in progress. One or
				more BCX slaves have
C 1	Davat		0	not responded.
51	Reset	VOUT_COMMAND has been reset without	0	RESET_VOUT event has
		PMBus commands.	1	not occurred. RESET_VOUT event has
			I	_
50	BCX fault	Back-channel communications fault has	0	occurred. No Fault.
50	BCX IQUII	occurred.	1	Fault.
49	Sync fault	Sync fault has occurred.	0	No Fault.
47	Sync Iduli	sync rauli has occurred.	1	Fault.
40	First to Alert	The device was the first to assert SMBALERT.	1	
40	FIRST TO AIEIT	The device was the first to assert smbalert.	0	First to assert SMBALERT. The device was not the
			0	first to assert SMBALERT.
				This could mean either
				that the SMBALERT
				signal is not asserted
				(or has since been
				cleared), or that it is
				asserted, but this
				device was not the first
				on the bus to assert it.
39	Invalid Or	Invalid Or Unsupported Command Received.	0	No Invalid Command
	Unsupported			Received.
	Command		1	Invalid Command
	Received			Received.
38	Invalid Or	Invalid Or Unsupported Data Received.	0	No Invalid Data
	Unsupported Data			Received.
	Received		1	Invalid Data Received.
37	Packet Error Check	Packet Error Check (PEC) Failed.	0	No Failure.
	Failed		1	Failure.
36	Memory Error	A memory error was detected.	0	No Fault.
			1	Fault.
33			0	No Fault.

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	Other	A PMBus command tried to write to a read-only	1	Fault.
	Communication	or protected command, or a communication		
	Fault	fault other than the ones listed in this table has		
		occurred.		
31	Overtemperature	Latched flag of over-temperature fault has	0	No Fault.
	Fault	occurred.	1	Fault.
30	Overtemperature	Latched flag of over-temperature warn has	0	No Fault.
	Warn	occurred.	1	Fault.
23	Vin Overvoltage	Latched flag of input over-voltage fault has	0	No Fault.
	Fault	occurred.	1	Fault.
22	Vin OV Warn	Vin OV Warn Latched flag of input over-voltage warning has		No Fault.
		occurred.	1	Fault.
21	Vin UV Warn	Latched flag of input under-voltage warning	0	No Fault.
		has occurred.	1	Fault.
20	Vin UV Fault	Latched flag of input under-voltage fault has	0	No Fault.
		occurred.	1	Fault.
19	Low Vin Fault	Latched flag of shutdown unit due to	0	No Fault.
		insufficient VIN .	1	Fault.
18	lin Oc Fault	Latched flag of input over-current fault has	0	No Fault.
		occurred.	1	Fault.
17	lin Oc Warn	Latched flag of input over-current warning has	0	No Fault.
		occurred.	1	Fault.
16	Pin Op Warn	Latched flag of input over-power warning has	0	No Fault.
		occurred.	1	Fault.
15	lout OC Fault	Latched flag of lout over-current fault has	0	No Fault.
		occurred.	1	Fault.
13	lout OC Warn	Latched flag of lout over-current warning has	0	No Fault.
		occurred.	1	Fault.
12	lout UC Fault	Latched flag of lout under-current fault has	0	No Fault.
		occurred.	1	Fault.
11	Current Share Fault	Latched flag of current share fault has	0	No Fault.
		occurred.	1	Fault.
7	Vout OV Fault	Latched flag of Vout over-voltage fault has	0	No Fault.
		occurred.	1	Fault.
6	Vout OV Warn	Latched flag of Vout over-voltage warning has	0	No Fault.
		occurred.	1	Fault.
5	Vout UV Warn	Latched flag of Vout under-voltage warning	0	No Fault.
		has occurred .	1	Fault.
4	Vout UV Fault	Latched flag of Vout under-voltage fault has	0	No Fault.
		occurred.	1	Fault.
3	Vout Min/Max Fault	Latched flag of Vout min/max fault or warning	0	No Fault.
		has occurred .	1	Fault.
2	Ton Max Fault	Latched flag of Ton max fault or warning has	0	No Fault.
		occurred.	1	Fault.

STATUS_PHASE (0xDC)

Addressing: Phase

Description: When PHASE = FFh or 80h, reads to this command return a data word detailing which phases have experienced fault conditions. When PHASE != FFh, reads to this command return a data word detailing which fault(s) the current PHASE has experienced. PHASE number assignment is per PHASE_CONFIG.

Bit	Function	Description	Value	Description
3	Phase 4 Fault		0	



		The module assigned to PHASE=3 has experienced a fault. Set PHASE = 3, and read STATUS_WORD or STATUS_ALL for more information.	1	
2	Phase 3 Fault	The module assigned to PHASE=2 has experienced a fault. Set PHASE = 2, and read STATUS_WORD or STATUS_ALL for more information.	0	
1	Phase 2 Fault	The module assigned to PHASE=1 has experienced a fault. Set PHASE = 1, and read STATUS_WORD or STATUS_ALL for more information.	0	
0	Phase 1 Fault	The module assigned to PHASE=0 has experienced a fault. Set PHASE = 0, and read STATUS_WORD or STATUS_ALL for more information.	0	

PGOOD_CONFIG (0xE3) Description: Provides control of the delays asserting and releasing PGOOD.

Bit	Function	Description	Value	Function	Description
15:12	PGOOD Off	Sets Delay from the detection	0x0	1 PWM CLK	
	Delay	of an unmasked Fault or	0x1	3 PWM CLKs	
	/	Warning event to the assertion	0x2	5 PWM CLKs	
		of PGOOD low. 0d: Delay	0x3	9 PWM CLKs	
		PGOOD high-low: 1 PWM CLK	0x4	17 PWM CLKs	
		1d-15d: Delay PGOOD high-	0x5	33 PWM CLKs	
		low: 2^N+1 PWM CLKs	0x6	65 PWM CLKs	
			0x7	129 PWM	
			••••	CLKs	
			0x8	257 PWM	
			0,10	CLKs	
			0x9	513 PWM	
				CLKs	
			0xA	1025 PWM	
				CLKs	
			OxB	2049 PWM	
				CLKs	
			0xC	4097 PWM	
				CLKs	
			0xD	8193 PWM	
				CLKs	
			0xE	16385 PWM	
				CLKs	
			OxF	32769 PWM	
				CLKs	
11:8	PGOOD On	Sets Delay from the detection	0x0	1 PWM CLK	
	Delay	of no unmasked Fault or	0x1	3 PWM CLKs	
		Warning events to the release	0x2	5 PWM CLKs	
		of PGOOD low. 0d: Delay	0x3	9 PWM CLKs	
		PGOOD low-high: 1 PWM CLK	0x4	17 PWM CLKs	
		1d-15d: Delay PGOOD low-	0x5	33 PWM CLKs	
		high: 2^N+1 PWM CLKs	0x6	65 PWM CLKs	
			0x7	129 PWM	
				CLKs	

flex.

			0x8	257 PWM	
			0.00	CLKs	
			0x9	513 PWM	
			0.7	CLKs	
			0xA	1025 PWM	
			UXA	CLKs	
			OxB	2049 PWM	
			UXD	CLKs	
			0xC	4097 PWM	
			UNC	CLKs	
			0xD	8193 PWM	
			UXD	CLKs	
			0xE	16385 PWM	
			UXE	CLKs	
			OxF	32769 PWM	
			UXF	CLKs	
7	PGOOD	Controls if Output Overveltage	0		PCOOD amorted low by
/		Controls if Output Overvoltage	0	True	PGOOD asserted low by
	Output	Fault should assert PGOOD low.	1	False	Output Overvoltage Fault
	Overvoltage Fault		I	Faise	PGOOD not asserted low by
			0	Turre	Output Overvoltage Fault
6	PGOOD	Controls if Output Overvoltage	0	True	PGOOD asserted low by
	Output	Warning should assert PGOOD			Output Overvoltage Warning
	Overvoltage	low.	1	False	PGOOD not asserted low by
	Warning		-	-	Output Overvoltage Warning
5	PGOOD	Controls if Output	0	True	PGOOD asserted low by
	Output	Undervoltage Fault should	-		Output Undervoltage Fault
	Undervoltage	assert PGOOD low.	1	False	PGOOD not asserted low by
4	Fault		<u>^</u>	-	Output Undervoltage Fault
4	PGOOD	Controls if Output	0	True	PGOOD asserted low by
	Output	Undervoltage Warning should			Output Undervoltage
	Undervoltage	assert PGOOD low.	-		Warning
	Warning		1	False	PGOOD not asserted low by
					Output Undervoltage
0			<u>^</u>		Warning
3	PGOOD	Controls if Output Overcurrent	0	True	PGOOD asserted low by
	Output	Warning should assert PGOOD	-		Output Overcurrent Warning
	Overcurrent	low.	1	False	PGOOD not asserted low by
-	Warning			-	Output Overcurrent Warning
2	PGOOD	Controls if Output Overcurrent	0	True	PGOOD asserted low by
	Output	Fault should assert PGOOD low.			Output Overcurrent Fault
	Overcurrent		1	False	PGOOD not asserted low by
	Fault		-		Output Overcurrent Fault
1	PGOOD	Controls if Input Overvoltage	0	True	PGOOD asserted low by Input
	Input	Warning should assert PGOOD			Overvoltage Warning
	Overvoltage	low.	1	False	PGOOD not asserted low by
	Warning				Input Overvoltage Warning
0	PGOOD	Controls if Input Overvoltage	0	True	PGOOD asserted low by Input
	Input	Fault should assert PGOOD low.			Overvoltage Fault
	Overvoltage		1	False	PGOOD not asserted low by
	Fault				Input Overvoltage Fault

SYNC_CONFIG (0xE4) Description: Configures synchronization options.

Bit	Function	Description	Value	Function	Description



7:6	Sync Dir	When SYNC_DIR = 11b - Enable Auto Detect, the SYNC_IN or	00	SYNC Disabled	
		SYNC_OUT will be selected	01	Sync out	
		based on the state of the SYNC	10	Sync in	
		pin when the enable Condition, as defined by ON_OFF_CONFIG is met.	11	Auto Detect Sync	
5	Sync Edge	Synchronizes to falling or rising	0	Falling Edge	
		edge of SYNC.	1	Rising Edge	

STACK_CONFIG (0xEC)

Description: Configures multi-phase stack settings.

Bit	Function	Description				Format
7:4	BCX Start	BCX address for stack master.				Integer Unsigned
					-	
Bit	Function	Description	Value	Function	Description	n
3:0	BCX Stop	Configures multi-phase stack	0000	Stand Alone,		
		settings.		1 Phase		
			0001	1 Slave, 2		
				Phases		
			0010	2 Slaves, 3		
				Phases		
			0011	3 Slaves, 4		
				Phases		

MISC_OPTIONS (0xED) Description: Configures miscellaneous settings.

Bit	Function	Description	Value	Function	Description
15	Require	Enables/Disables Packet Error	0		Disabled
	Packet Error Check	Check.	1		Enabled
14	Reset on Shutdown	Resets VOUT_COMMAND to VBOOT on shutdown.	0		VOUT_COMMAND will be unchanged following a shutdown.
			1		VOUT_COMMAND will be changed to VBOOT on a Control or OPERATION shutdown.
13	Reset on Fault	Resets VOUT_COMMAND to VBOOT on fault restart.	0		VOUT_COMMAND will be unchanged following a Fault Restart.
			1		VOUT_COMMAND will be changed to VBOOT on Restart from a Fault when Fault Retry is set to Retry after Fault.
12	Reset	Sets the function of the PGOOD/RESET pin.	0	PGOOD	
3	Pull-up	Sets the pull-up of the PGD/RESET_B pin when RESET# = 1b.	0	Disabled	Disabled
2	Fault Count	Fault count.	0	Counts down 1 cycle	Fault Counter counts down one cycle on PWM cycle without fault.

			1	Resets to 0	Fault Counter resets counter to 0 on PWM cycle without fault.
1:0	ADC	Sets the ADC resolution.	00	12-bit	
	Resolution		01	10-bit	
			10	8-bit	
			11	6-bit	

PIN_DETECT_OVERRIDE (0xEE)

Description: Prevents the Default or User Store values from over-writing the pin-programmed value.

Bit	Function	Description	Value	Function	Description
12	STACK_CONF	Decides if STACK_CONFIG will	0	NVM	
	IG	be restored from NVM or pin	1	Pin Detection	
		detection at power-up or			
11	SYNC_CONFI	RESTORE. Decides if SYNC_CONFIG will	0	NVM	
11	G	be restored from NVM or pin	1	Pin Detection	
	Ũ	detection at power-up or		Thr Boroenon	
		RESTORE.			
9	COMPENSATI	Decides if	0	NVM	
	ON_CONFIG	COMPENSATION_CONFIG will			
		be restored from NVM or pin detection at power-up or			
		RESTORE.			
8	SLAVE_ADDR	Decides if SLAVE_ADDRESS will	0	NVM	
	ESS	be restored from NVM or pin	1	Pin Detection	
		detection at power-up or			
5	INTERLEAVE	RESTORE. Decides if INTERLEAVE will be	0	NVM	
5		restored from NVM or pin	1	Pin Detection	
		detection at power-up or			
		RESTORE.			
3	TON_RISE	Decides if TON_RISE will be	0	NVM	
		restored from NVM or pin detection at power-up or	1	Pin Detection	
		RESTORE.			
2	IOUT_OC_FA	Decides if	0	NVM	
	ULT/WARN_LI	IOUT_OC_FAULT_LIMIT and	1	Pin Detection	
	MIT	IOUT_OC_WARN_LIMIT will be			
		restored from NVM or pin			
		detection at power-up or RESTORE.			
1	FREQUENCY_	Decides if FREQUENCY_SWITCH	0	NVM	
	SWITCH	will be restored from NVM or			
		pin detection at power-up or			
	Vout Doletta -	RESTORE.		NVM	
0	Vout Related Commands	Decides if VOUT_COMMAND, VOUT_SCALE_LOOP,	0	Pin Detection	
	Communus	VOUT_SCALE_LOOF, VOUT_MAX, and VOUT_MIN will			
		be restored from NVM or pin			
		detection at power-up or			
		RESTORE.			

SLAVE_ADDRESS (0xEF)

Description: Used to program or read-back the slave address of digital communication. When a slave address is updated, the device starts responding to the new address immediately.

Bit	Description	Format
6:0	Sets or retrieves the PMBus slave address. There are a number of slave address values	Integer Unsigned
	which are reserved in the SMBus specification. The following reserved addresses are	
	invalid and can not be programmed: 0x0C, 0x28, 0x37 and 0x61.	

NVM_CHECKSUM (0xF0)

Description: Reports the CRC-16 (polynomial 0x8005) checksum for the current NVM settings.

Bit	Description	Format
15:0	CRC16 for EEPROM settings.	Integer Unsigned

SIMULATE_FAULT (0xF1)

Description: Simulates fault and warning conditions by triggering the output of the detection circuit for that controls it. Multiple faults and/or warnings can be simulated at once.

Bit	Function	Description	Value	Description
15	Fault Persist	Persist simulated faults.	0	Simulated faults are automatically removed after one Fault response.
			1	Simulated faults persist until SIMULATE_FAULT is written again.
14	Sim Temp OTF	Simulate over-temperature fault	0	
12	Sim IOUT OCF	Simulate output current over-current fault.	0	
11	Sim VIN UVLO	Simulate VIN undervoltage lockout.	0	
10	Sim VIN OVF	Simulate VIN over-voltage fault.	0	
9	Sim VOUT UVF	Simulate VOUT under-voltage fault.	0	
8	Sim VOUT OVF	Simulate VOUT over-voltage fault.	0	
7	Warn Persist	n Persist Persist simulated warnings.	0	Simulated warnings are automatically removed after one Fault response.
			1	Simulated warnings persist until SIMULATE_FAULT is written again.
4	Sim IOUT OCW	Simulate output current over-current warning.	0	
3	Sim VIN UVW	Simulate VIN under-voltage warning.	0	
1	Sim VOUT UVW	Simulate VOUT under-voltage warning.	0	
0	Sim VOUT OVW	Simulate VOUT over-voltage warning.	0	

