Technical Specification

BMR4742001 series PoL Regulators Input 6-15 V, Output up to 80 A / 198 W	1/28701-BMR474 Rev. A May 2021 © Flex

Key Features

- Small Package
  33 x 8.6 x 19 mm (1.299 x 0.339 x 0.748 in)
- 0.6 V- 3.3 V output voltage range
- Maximum output current 80 A
- High efficiency, typ. 95.1% at 12Vin, 3.3 Vout full load
- Fast load transient response
- Configuration and monitoring via PMBus
- Synchronization and phase spreading
- Meets safety requirements according to IEC/EN/UL 62368-1
- MTBF 23.19 Mh

General Characteristics

- Configuration support via Flex Power Designer
- Monotonic soft start up
- Input under voltage & over voltage protection
- Output over current & over voltage protection
- Differential remote sense
- Remote control & Power Good
- Output voltage setting via pin-strap or PMBus
- Over temperature protection
- Highly automated manufacturing ensures quality
- ISO 9001/14001 certified supplier

Safety Approvals

Design for Environment

Meets requirements in high-temperature lead-free soldering processes.

Contents

Ordering Information

Product program	Output
BMR4742001/001	0.6 – 3.3 V, 80A, 198W

Product number and Packaging

BMR474$n_1n_2n_3n_4$/$n_5n_6n_7n_8$									
Options	n_1	n_2	n_3	n_4	/	n_5	n_6	n_7	n_8
Mechanical	o								
Lead length		o							
Hardware Variants			o	o					
Configuration file						o	o	o	
Packaging									o

Options	Description	
n_1	2 3	Single in line (SIP), open frame Single in line (SIP), heat sink
n_2	0	4.57 mm pin
n_3n_4	01	Standard variant
$n_5n_6n_7$	001	Standard configuration (positive Remote Control logic)
n_8	B	Tray (1 full package contains 100 pcs products.)

Example: Product number BMR4742001/001B equals an open frame, PMBus and pin strap, positive RC logic, standard configuration variant with tray packaging.

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF= 1/λ) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Flex uses Telcordia SR-332 Issue 4 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 4 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state failure rate, λ	Std. deviation, σ
43 nFailures/h	6.1 nFailures/h

MTBF (mean value) for the BMR474 series= 23.19 Mh.
MTBF at 90% confidence level = 19.65 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2011/65/EU and 2015/863 and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, DIBP and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Flex Power products are found in the Statement of Compliance document.

Flex Power fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Flex Power General Terms and Conditions of Sale.

Limitation of Liability

Flex does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

Safety Specification

General information

Flex Power DC/DC converters and DC/DC regulators are designed in accordance with the safety standards IEC 62368-1, EN 62368-1 and UL 62368-1 *Audio/video, information and communication technology equipment - Part 1: Safety requirements*

IEC/EN/UL 62368-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Electrically-caused fire
- Injury caused by hazardous substances
- Mechanically-caused injury
- Skin burn
- Radiation-caused injury

On-board DC/DC converters, Power interface modules and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without “conditions of acceptability”. Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

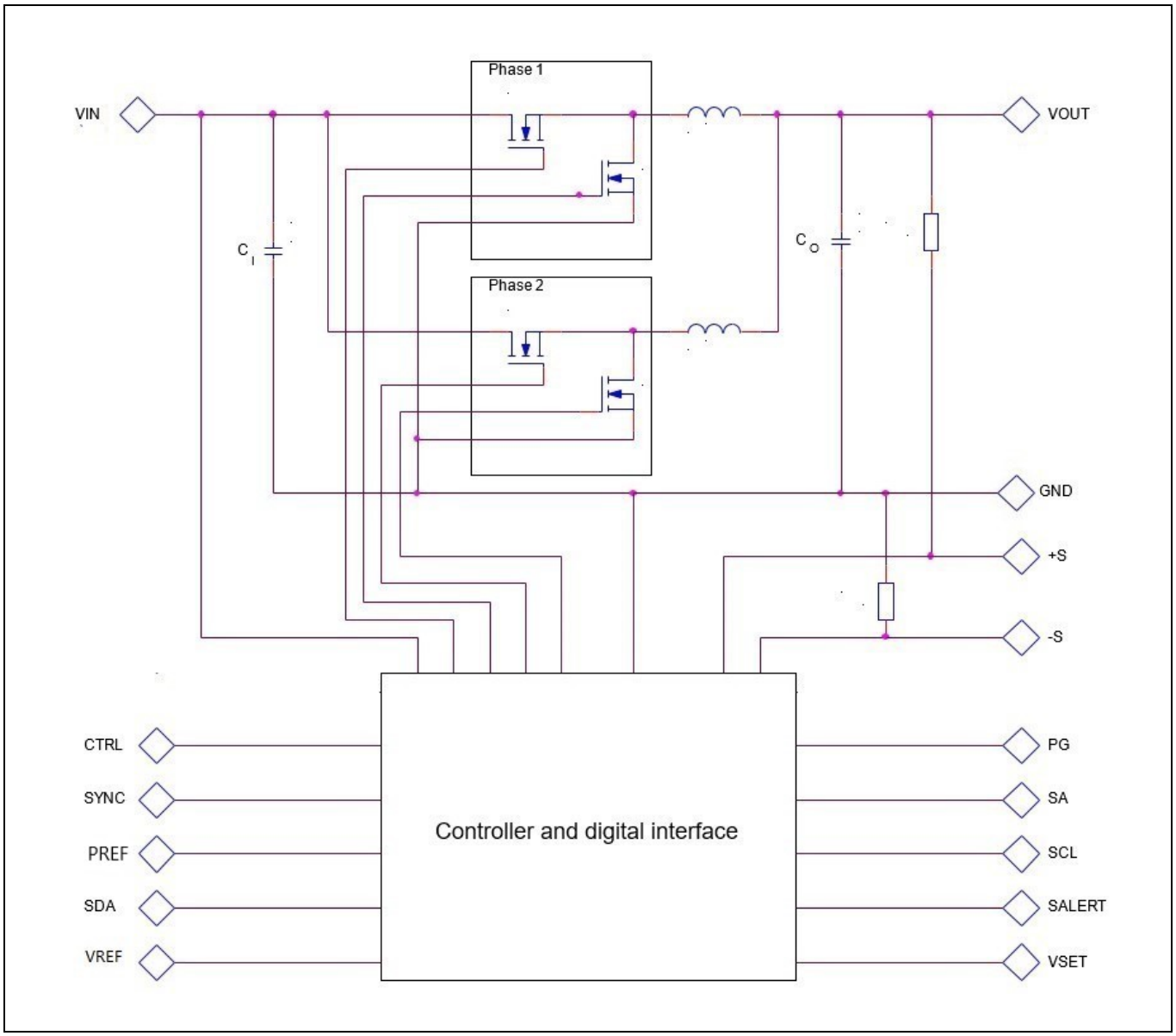
Component power supplies for general use shall comply with the requirements in IEC/EN/UL 62368-1. Product related standards, e.g. IEEE 802.3af *Power over Ethernet*, and ETS-300132-2 *Power interface at the input to telecom equipment, operated by direct current (dc)* are based on IEC/EN/UL 60950-1 with regards to safety.

Flex Power DC/DC converters, Power interface modules and DC/DC regulators are UL 62368-1 recognized and certified in accordance with EN 62368-1. The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

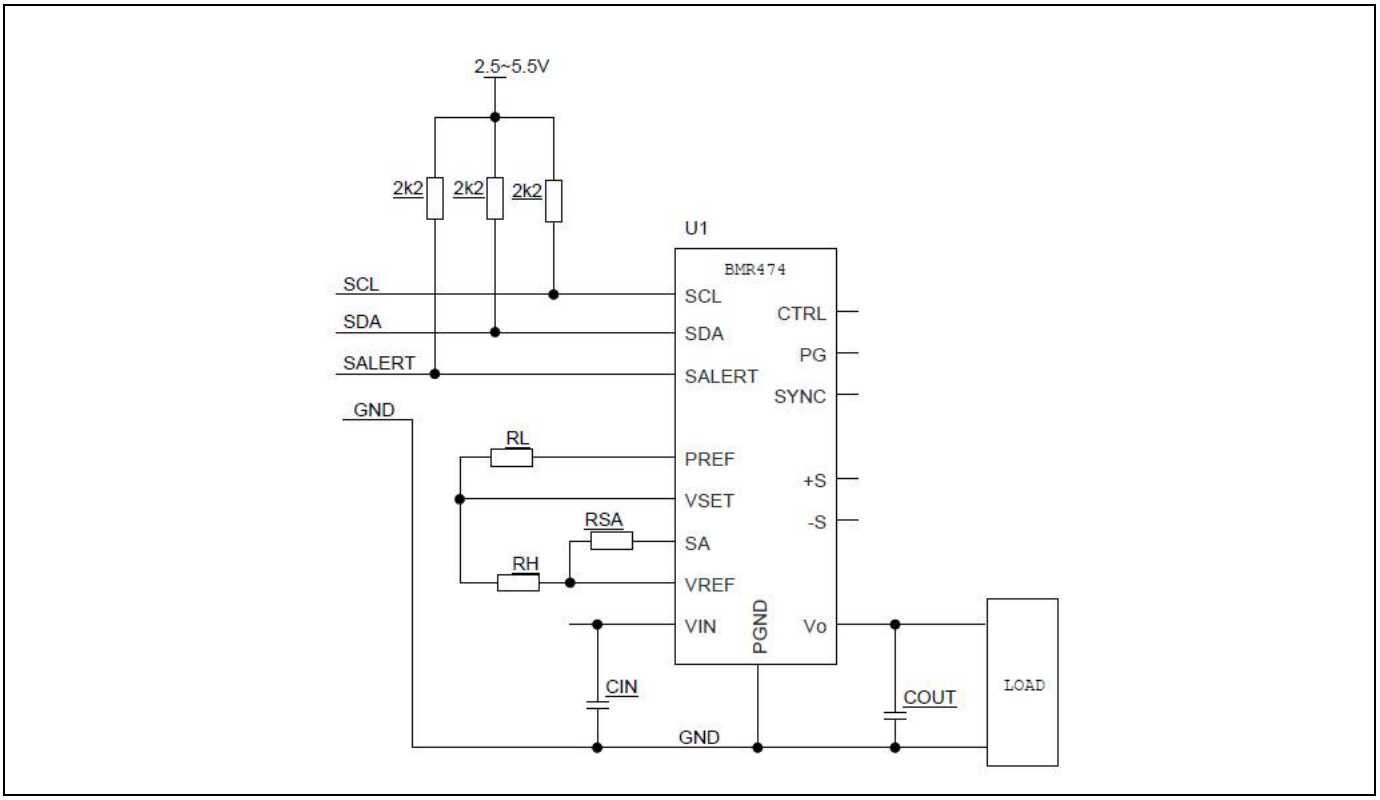
Non - isolated DC/DC regulators

The DC/DC regulator output is ES1 energy source if the input source meets the requirements for ES1 according to IEC/EN/UL 62368-1.

Internal Circuit Diagram



Typical Application Circuit



Standalone operation with PMBus communication.

Absolute Maximum Ratings

Characteristics		min	typ	max	Unit
T_{P1}	Operating temperature	-40		125	°C
T_S	Storage temperature (Ambient)	-40		125	°C
V_I	Input voltage (See Operating Information Section for input and output voltage relations)	-0.3		16	V
Signal I/O voltage	CTRL, SA, SALERT, SCL, SDA, VSET, SYNC, PG	-0.3		3.6	V
Ground voltage differential	-S, AGND, GND	-0.3		0.3	V
Analog pin voltage	V_O, +S	-0.3		3.7	V
	VREF	-0.3		1.65	V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the Electrical Specification section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. See technical paper TP023 for details on how data retention time of the Non-Volatile Memory (NVM) of the product is affected by high temperature.

Configuration File

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the Standard configuration, unless otherwise specified. The Standard configuration is designed to fit most application needs. Changes in Standard configuration might be required to optimize performance in specific application.

Common Electrical Specification

This section includes parameter specifications common to all product versions within the product series. Typically these are parameters defined by the digital controller of the products. In the table below PMBus commands for configurable parameters are written in capital letters.

T_{P1} = -40 to +85 °C, V_I = 6 to 15 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 12 V, max I_O, unless otherwise specified under Conditions.
V_O defined by pin-strap. Typical values for PMBus configurable parameters are given for standard (default) configuration.

Characteristics		Conditions	min	typ	max	Unit
f_{SW} = $1/T_{SW}$	Switching Frequency (default value)	0.6V≤ Vo ≤1.8V		500		kHz
		1.8V < Vo ≤3.3V		800		
	Switching Frequency Range, Note 1	PMBus configurable FREQUENCY_SWITCH	450		850	kHz
	Switching Frequency Set-point Accuracy		-10		10	%
	External Sync input Pulse Width		100			ns
	Sync output duty cycle		40	50	60	%
	SYNC allowable frequency difference	External sync	-50		50	kHz

T_{INIT}	Initialization Time	From V_I > ~2.7 V to ready to be enabled	20	ms
T_{ONdel_tot}	Output voltage Total On Delay Time	Enable by input voltage	T_{INIT} + T_{ONdel}	
		Enable by CTRL pin	T_{ONdel}	
T_{ONdel}	Output voltage On Delay Time	Turn on delay duration	0	ms
		Range PMBus configurable TON_DELAY	0 – 127.5	ms
		Accuracy (actual delay vs set value)	-10/+10	%
T_{OFFdel}	Output voltage Off Delay Time	Turn off delay duration, Note 2	0	ms
		Range PMBus configurable TOFF_DELAY	0 – 127.5	ms
		Accuracy (actual delay vs set value)	-10/+10	%
T_{ONrise} / $T_{OFFfall}$	Output voltage On/Off Ramp Time (0-100%-0 of V_O)	Turn on ramp duration	5	ms
		Turn off ramp duration	Disabled in standard configuration. Turn off immediately upon expiration of Turn off delay.	
		Ramp duration range PMBus configurable TON_RISE/TOFF_FALL	0 – 31.75	ms

Characteristics		Conditions	min	typ	max	Unit
Power Good, PG	PG threshold	Rising		90		% V_O
		Falling		85		% V_O
Input Under Voltage Protection, IUVP	IUVP threshold	0.6V≤ Vo ≤2.5V		5		V
		2.5< Vo ≤3.3V		6.5		
	IUVP threshold range	PMBus configurable VIN_UV_FAULT_LIMIT	4.0		11.25	V
	IUVP hysteresis			0.75		V
	Set point accuracy		-250		250	mV
	IUVP response delay			0		µs
	Fault response	VIN_UV_FAULT_RESPONSE		Shutdown, automatic restart, 50 ms. Note 3		
Input Over Voltage Protection, IOVP	IOVP threshold			16		V
	IOVP threshold range	PMBus configurable VIN_OV_FAULT_LIMIT	4		18	V
	Set point accuracy		-2		2	%
	IOVP response delay			0		µs
	Fault response	VIN_OV_FAULT_RESPONSE		Shutdown, automatic restart, 50 ms. Note 3		
Output Voltage Fixed Over Voltage Protection	Fixed OVP threshold			3.6		V
	Fixed OVP threshold range	PMBus configurable	0.6		3.7	V
	Fixed OVP threshold resolution	Resolution		0.1		V
	Accuracy		-50		50	mV
Output Voltage Tracking Over/Under Voltage Protection, OVP/UVP	UVP threshold			Vo-0.192		V
	UVP threshold range	PMBus configurable VOUT_UV_FAULT_LIMIT	Vo-0.448		Vo-0.032	V
	OVP threshold			Vo+0.192		V
	OVP threshold range	PMBus configurable VOUT_OV_FAULT_LIMIT	Vo+0.032		Vo+0.448	V
	UVP/OVP response time			0		µs
	Fault response	VOUT_UV_FAULT_RESPONSE VOUT_OV_FAULT_RESPONSE		Shutdown, automatic restart, 50 ms. Note 3		
Over Current Protection, OCP	OCP threshold	Set value for total output		105		A
	OCP threshold range	PMBus configurable IOUT _OC_FAULT_LIMIT	1		1023	A
	Protection delay			0		ms
	Fault response	IOUT_OC_FAULT_RESPONSE		Latched		
Over Temperature Protection, OTP Position P2,P3, Note 4	OTP threshold			140		°C
	OTP threshold range	PMBus configurable OT_FAULT_LIMIT	90		160	°C
	Fault response	OT_FAULT_RESPONSE		Latched		

Characteristics		Conditions	min	typ	max	Unit
Monitoring Accuracy	Input voltage READ_VIN		-2		2	%
	Output voltage READ_VOUT		-5		5	mV
	Output current READ_IOUT, Note 5	T_{P1} = 25 °C, V_O = 1.0 V		±5		A
	Temperature READ_TEMPERATURE_1	Internal temperature of hottest power stage	-2.5		2.5	°C

V_{OL}	Logic output low signal level	SCL, SDA, SYNC, SALERT, PG Sink/source current = 20 mA			0.4	V
V_{OH}	Logic output high signal level		2.25			V
V_{IL}	Logic input low	SCL, SDA, CTRL, SYNC			0.8	V
V_{IH}	Logic input high		1.35			V
I_{I_LEAK}	Logic leakage current	SCL, SDA, SYNC, SALERT, PG	-10		10	µA
C_{I_PIN}	Logic pin input capacitance	SCL, SDA, CTRL, SYNC		10		pF
R_{I_PU}	Logic pin internal pull-up resistance	SCL, SDA, SALERT		No internal pull-up		
		CTRL to +3.3V		10		kΩ
f_{SMB}	Supported SMBus Operating frequency		0.05		2	MHz
T_{BUF}	SMBus Bus free time	STOP bit to START bit	0.5			µs
t_{set}	SMBus SDA setup time from SCL		0.26			µs
t_{hold}	SMBus SDA hold time from SCL		0			µs
	SMBus START/STOP condition setup/hold time from SCL		0.26			µs
T_{low}	SCL low period		0.5			µs
T_{high}	SCL high period		0.26		50	µs

Note 1. There are configuration changes to consider when changing the switching frequency. The switching frequency below 450 kHz is not recommended due to increased ripple current. Changing switching frequency might have other impacts, please check with Flex FAE.
Note 2. A default value of 0 ms forces the device to Immediate Off behavior with TOFF_FALL ramp-down setting being ignored.
Note 3. Automatic restart ~50 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart.
Note 4. See section Over Temperature Protection (OTP). The value is internal temperature of power stage.
Note 5. Monitoring Accuracy of output current is optimized for V_I = 12 V and V_O = 1.0 V.

Product Electrical Specification

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T_{P1} = -40 to +85 °C, V_I = 6 to 15 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
V_O defined by pin strap. Standard configuration.
Tested with external C_{IN} = 1000 µF/12 mΩ OS-CON + 4 x 22 µF Ceramic, C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic.
In the test set-up sense lines are open and all the output voltage measurements are made on output pins.

Characteristics			Conditions	min	typ	max	Unit
V_I	Input voltage		0.6 ≤Vo ≤2.5	6		15	V
			2.5 <Vo ≤3.3V	7.5		15	V
	Input voltage slew rate		Monotonic			10	V/ms
Vo	Output voltage adjustment range			0.6		3.3	V
	Output voltage adjustment including PMBus margining			0.54		3.63	V
	Output voltage pinstrap set-point resolution, Note 6		0.6V≤ Vo ≤2.77V,		10		mV
	Output voltage accuracy,		Including line, load, temp	-1		1	% V_O
	Internal resistance +S/-S to VOUT/GND				47		Ω
	+S bias current					50	µA
	-S bias current			-55			µA
	Line regulation	I_O = max I_O	V_O = 0.6 V		1		mV
			V_O = 1.0 V		2		
			V_O = 1.8 V		2		
			V_O = 2.5 V		3		
			V_O = 3.3 V (Vin: 7.5~15V)		3		
	Load regulation	I_O = 0 - 100%	V_O = 0.6 V		3		mV
			V_O = 1.0 V		3		
			V_O = 1.8 V		2		
			V_O = 2.5 V		2		
			V_O = 3.3 V		2		
V_{Oac}	Output ripple & noise (up to 20 MHz bandwidth)		V_O = 0.6 V		4.5		mVp-p
			V_O = 1.0 V		5.0		
			V_O = 1.8 V		7.0		
			V_O = 2.5 V fsw=800KHz		6.0		
			V_O = 3.3 V fsw=800KHz		6.5		
I_O	Output current		V_O = 0.6 V	0		80	A
			V_O = 1.0 V				
			V_O = 1.8 V				
			V_O = 2.5 V	0		60	
			V_O = 3.3 V				
I_{lim}	Current limit threshold		V_O = 0.6 V		105		A
			V_O = 1.0 V				
			V_O = 1.8 V				
			V_O = 2.5 V		85		A
			V_O = 3.3 V				
η	Efficiency	50% of max I_O	V_O = 0.6 V		86.9		%
			V_O = 1.0 V		90.9		
			V_O = 1.8 V		93.6		
			V_O = 2.5V		94.1		
			V_O = 3.3 V, Note 7		95		
		I_O = max I_O	V_O = 0.6 V		84.2		%
			V_O = 1.0 V		89.1		
			V_O = 1.8 V		92.5		
			V_O = 2.5V		94.1		
			V_O = 3.3 V, Note 7		95.1		

P_d	Power dissipation at max I_O		V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 2.5V V_O = 3.3 V, Note 7	9 9.8 11.6 9.4 10.1		W
P_{li}	Input idling power	I_O = 0	V_O = 0.6 V V_O = 1.0 V V_O = 1.8 V V_O = 2.5 V V_O = 3.3 V, Note 7	1.2 1.3 2.2 2.6 3.0		W
P_{CTRL}	Input standby power		Turned off with CTRL-pin	0.44		W
C_I	Internal input capacitance			88		µF
C_O	Internal output capacitance			400		µF
C_{IN}	External input capacitance			1000		µF
C_{OUT}	External output capacitance			4500	12500	µF

Note 6. See section 'Output Voltage Adjust using Pin-strap Resistor'
Note 7. Switching frequency 800kHz for Vo=2.5V and 3.3V, 500kHz for Vo=0.6V, 1.0V, 1.8V

Typical Output Characteristics, V_O = 0.6 V

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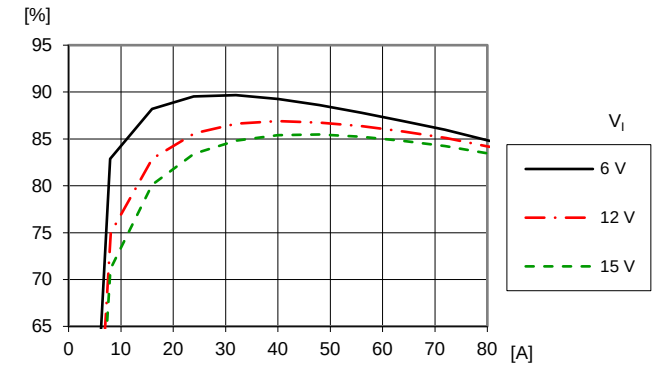
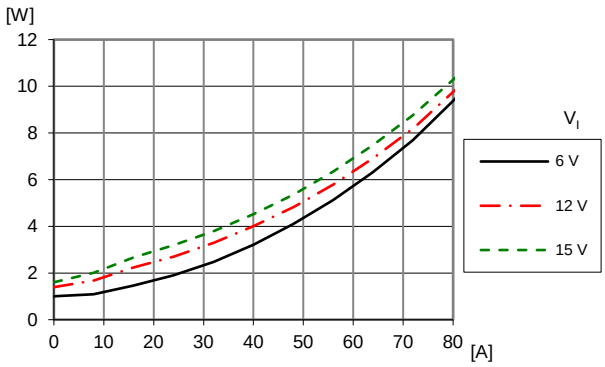
Standard configuration unless otherwise specified, T_{P1} = +25 °C

Efficiency



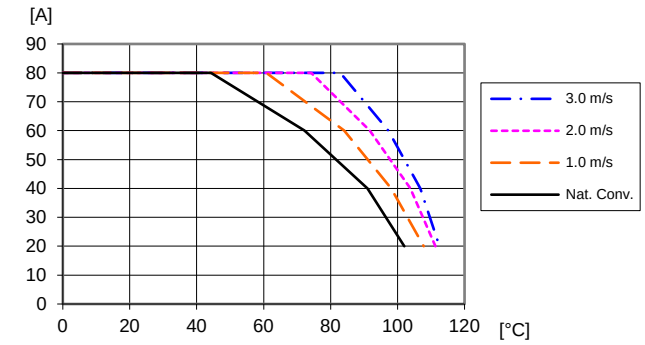
Efficiency vs. load current and input voltage.

Power Dissipation



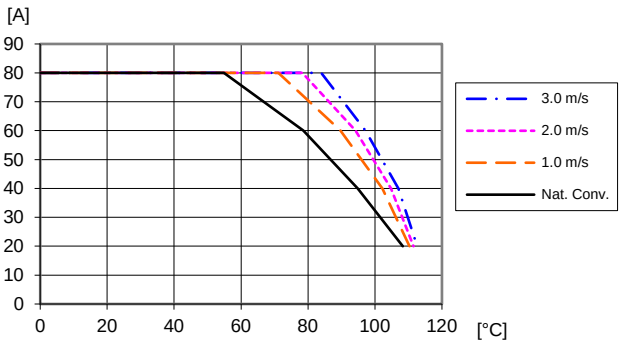
Dissipated power vs. load current and input voltage.

Output Current Derating for open frame version



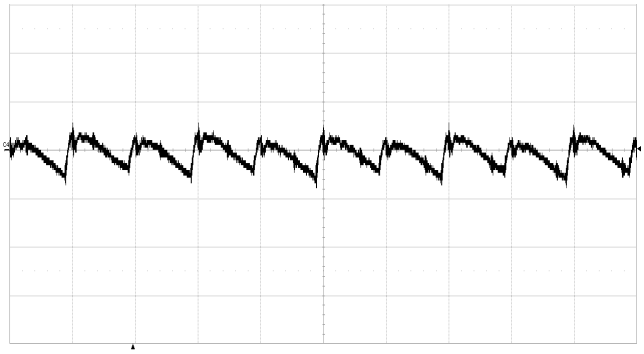
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Current Derating for heatsink version



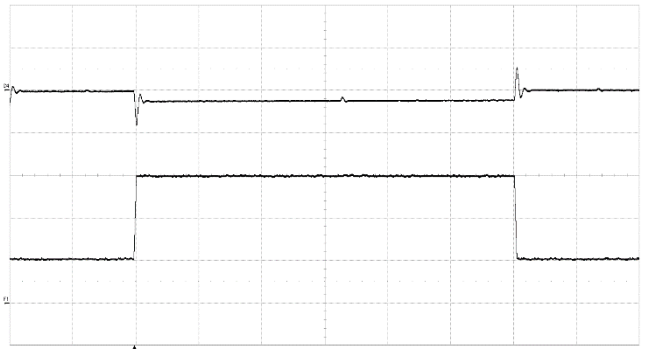
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = max I_O,
C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic
Scale: 2 mV/div, 1 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response



Output voltage response to load current step change (20–60–20 A) at V_I = 12 V, C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic,
di/dt = 2 A/µs, ACLL=1
Scale top: 50mV/div, scale bottom: 20 A/div, time scale 500 µs/div.

Typical Output Characteristics, V_O = 1.0 V

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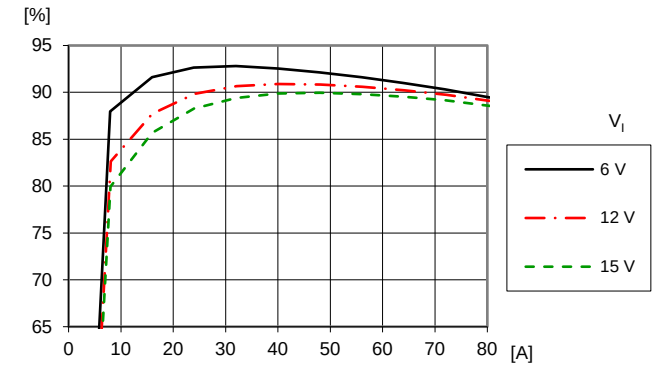
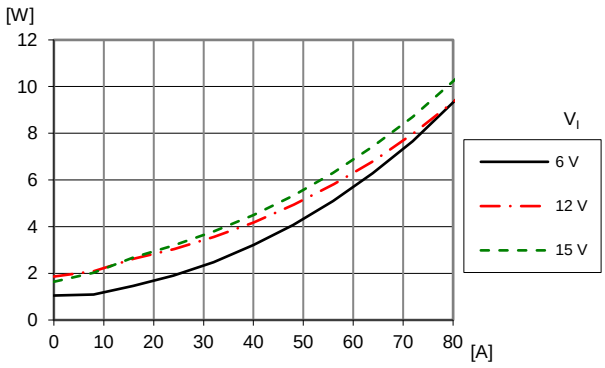
Standard configuration unless otherwise specified, T_{P1} = +25 °C

Efficiency



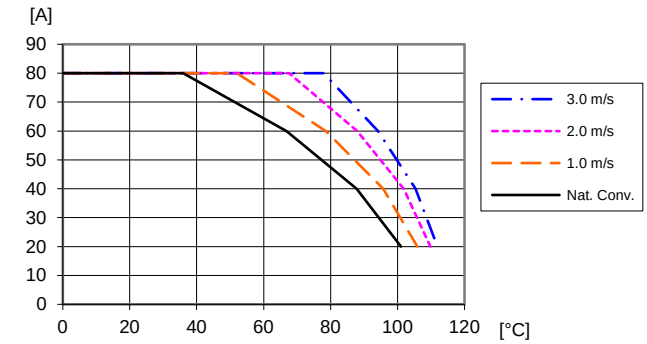
Efficiency vs. load current and input voltage.

Power Dissipation



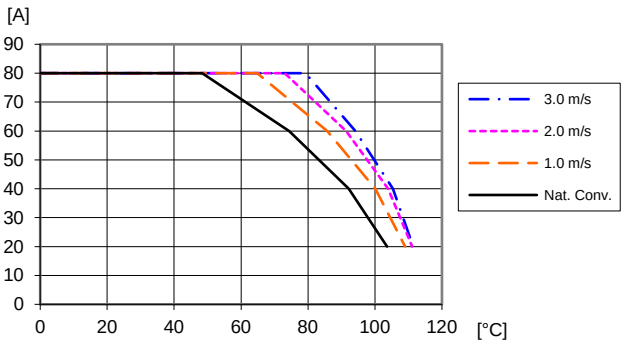
Dissipated power vs. load current and input voltage.

Output Current Derating for open frame version



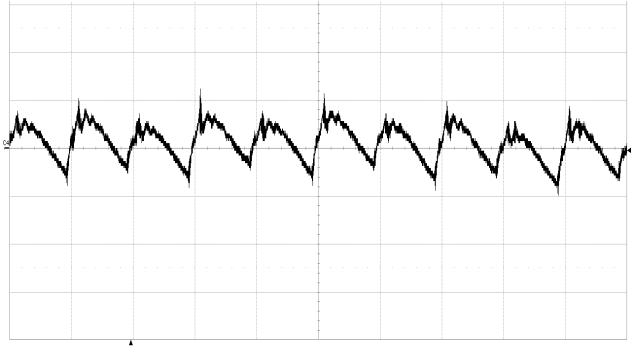
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Current Derating for heatsink version



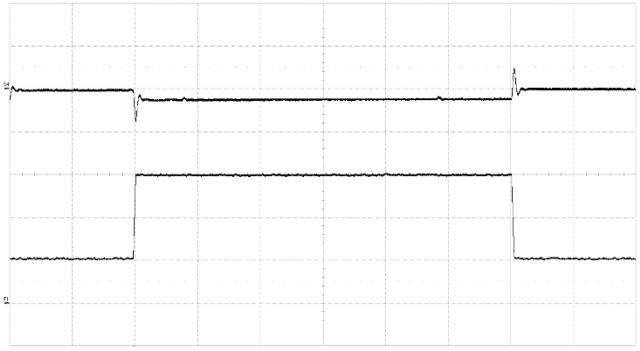
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = max I_O,
C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic
Scale: 2 mV/div, 1 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response



Output voltage response to load current step change (20–60–20 A) at
V_I = 12 V, C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic,
di/dt = 2 A/µs, ACLL=1
Scale top: 50mV/div, scale bottom: 20 A/div, time scale 500 µs/div.

Typical Output Characteristics, V_O = 1.8 V

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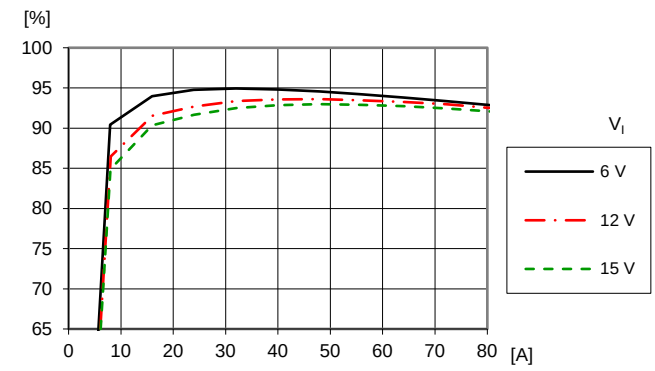
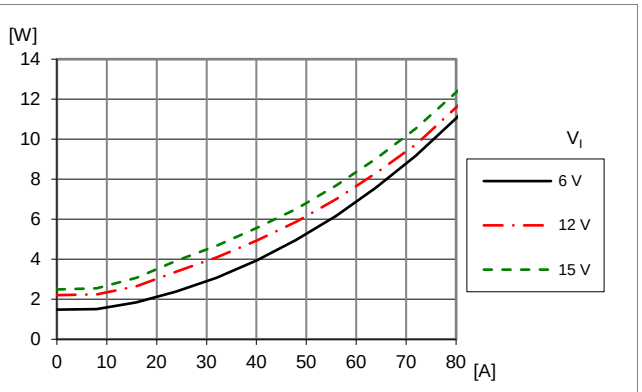
Standard configuration unless otherwise specified, T_{P1} = +25 °C

Efficiency



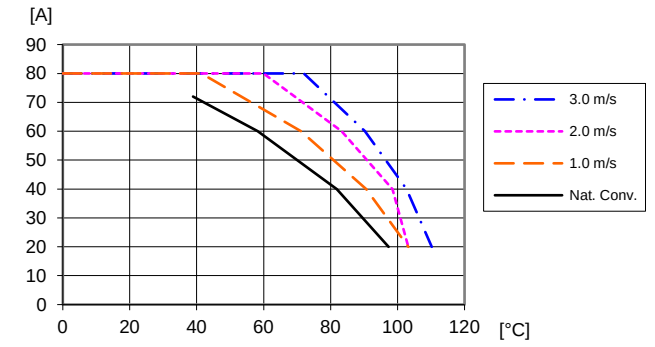
Efficiency vs. load current and input voltage.

Power Dissipation



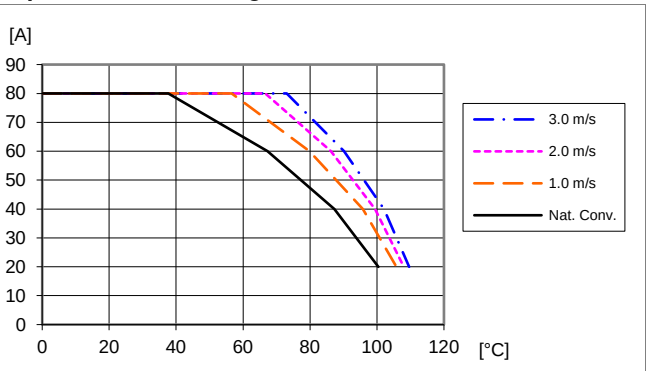
Dissipated power vs. load current and input voltage.

Output Current Derating for open frame version



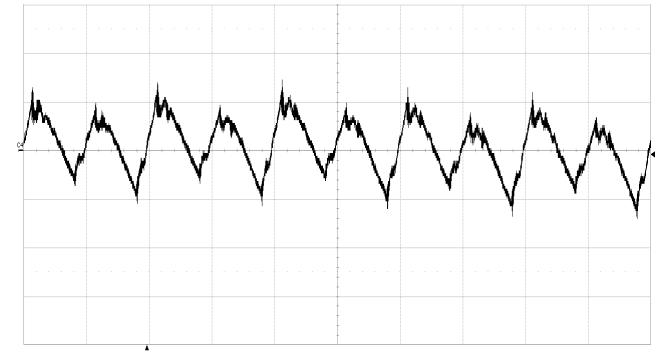
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Current Derating for heatsink version



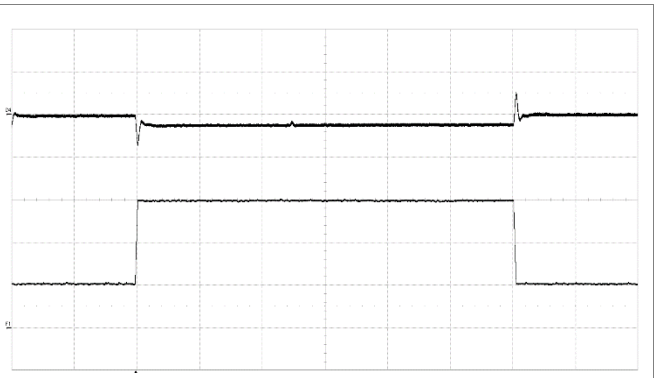
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = max I_O,
C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic
Scale: 2 mV/div, 1 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response



Output voltage response to load current step change (20–60–20 A) at V_I = 12 V, C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic, di/dt = 2 A/µs, ACLL=3.5
Scale top: 50mV/div, scale bottom: 20 A/div, time scale 500 µs/div.

Typical Output Characteristics, V_O = 2.5 V

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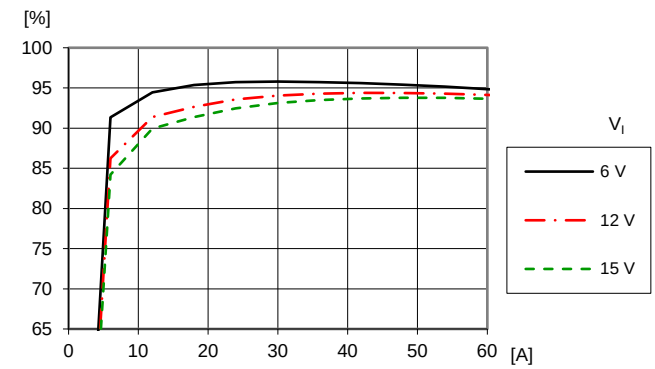
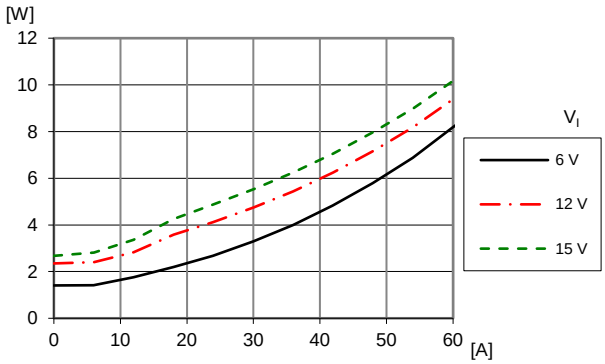
Standard configuration unless otherwise specified, T_{P1} = +25 °C

Efficiency



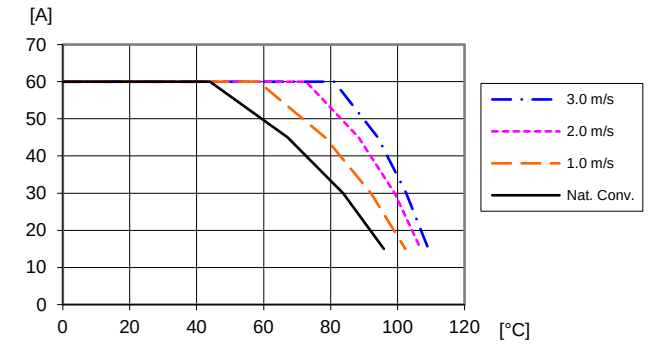
Efficiency vs. load current and input voltage.

Power Dissipation



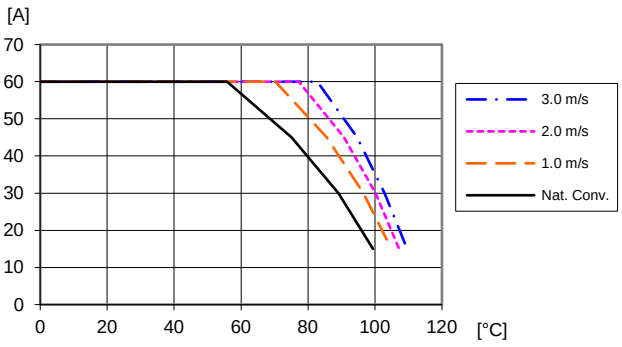
Dissipated power vs. load current and input voltage.

Output Current Derating for open frame version



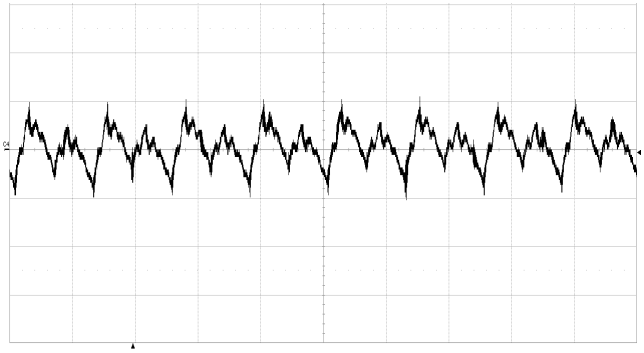
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Current Derating for heatsink version



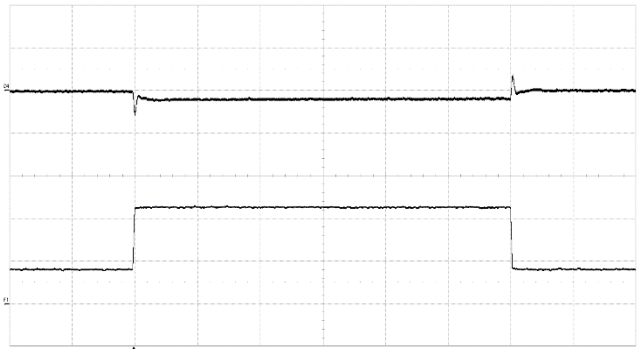
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = max I_O,
C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic
Scale: 2 mV/div, 1 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response



Output voltage response to load current step change (15–45–45 A) at V_I = 12 V, C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic, di/dt = 2 A/µs, ACLL=3
Scale top: 50mV/div, scale bottom: 20 A/div, time scale 500 µs/div.

Typical Output Characteristics, V_O = 3.3 V

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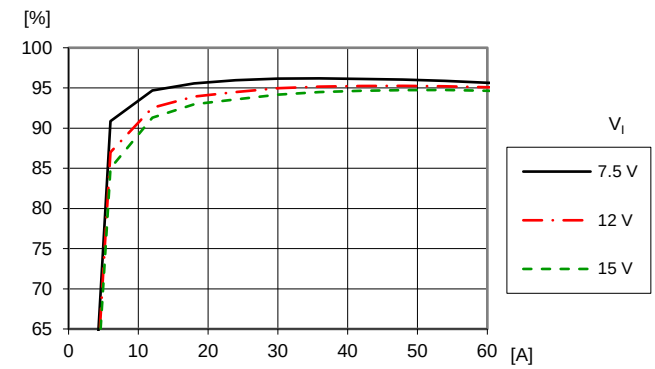
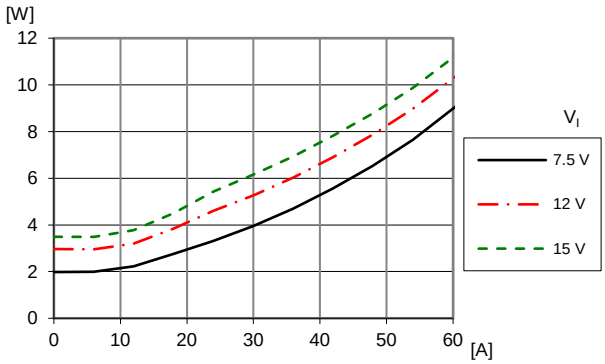
Standard configuration unless otherwise specified, T_{P1} = +25 °C

Efficiency



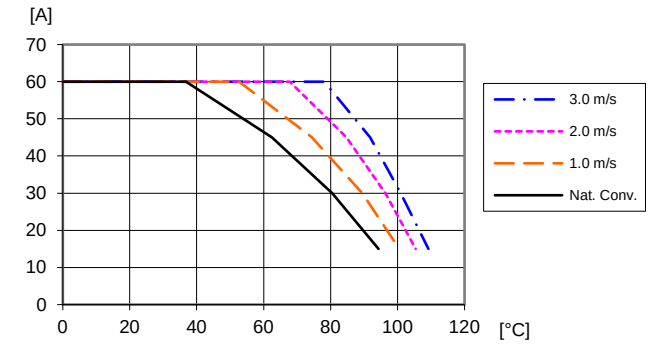
Efficiency vs. load current and input voltage.

Power Dissipation



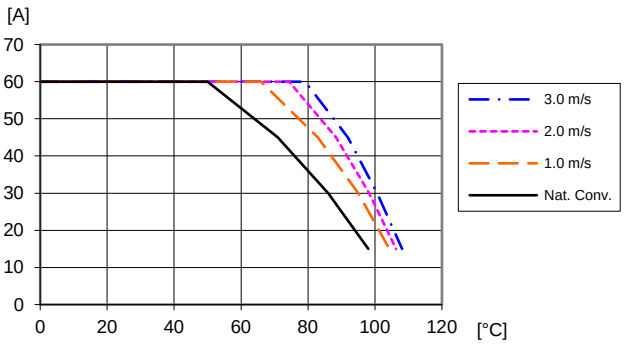
Dissipated power vs. load current and input voltage.

Output Current Derating for open frame version



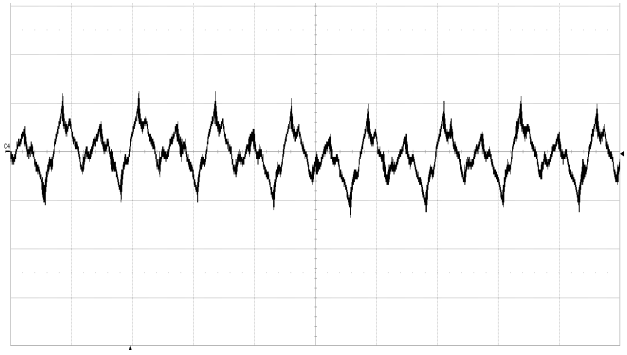
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Current Derating for heatsink version



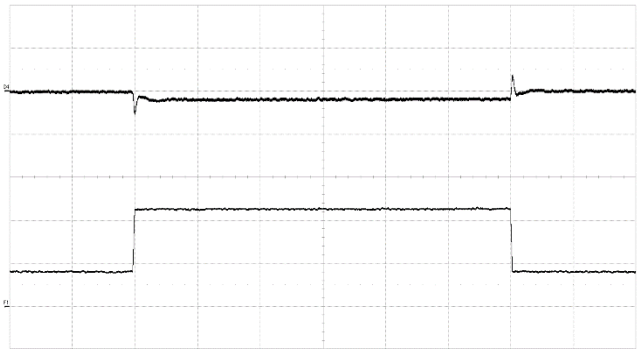
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = max I_O,
C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic
Scale: 2 mV/div, 1 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response



Output voltage response to load current step change (15–45–15 A) at V_I = 12 V, C_{OUT} = 10 x 330 µF/10 mΩ + 12 x 100 µF Ceramic,
di/dt = 2 A/µs, ACLL=2.3
Scale top: 50mV/div, scale bottom: 20 A/div, time scale 500 µs/div.

Typical On/Off Characteristics

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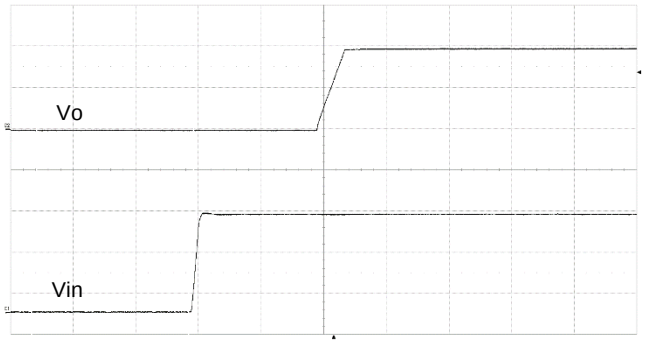
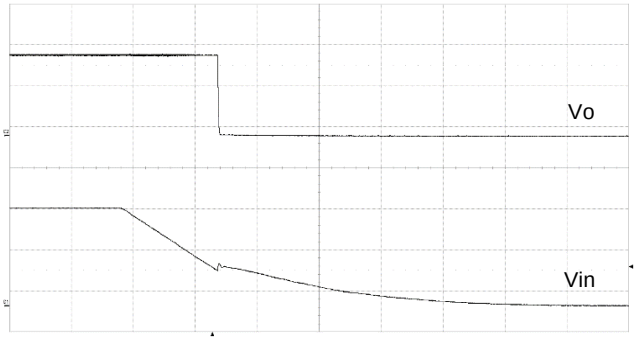
Standard configuration, T_{P1} = +25 °C, V_O = 1.0 V

Enable by input voltage



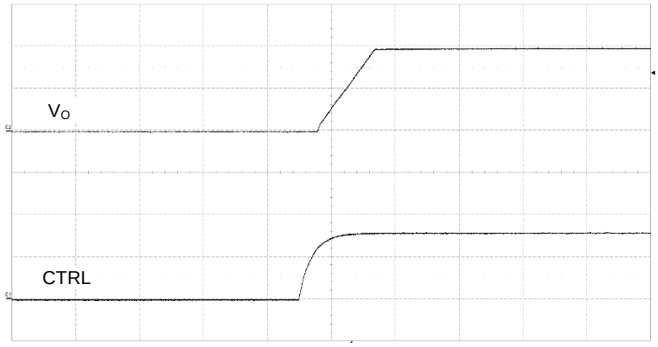
Output enabled by applying V_I. V_I = 12 V, I_O = max I_O.
TON_DELAY =0ms, TON_RISE = 5 ms
Scale top: 0.5 V/div, Scale bottom: 5V/div, time scale: 10 ms/div.

Disable by input voltage



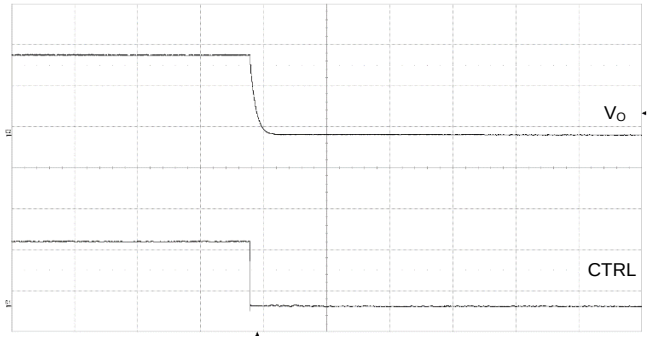
Output disabled by removing V_I. V_I = 12 V, I_O = max I_O.
Scale top: 0.5V/div, scale bottom: 5V/div, time scale: 5 ms/div.

Enable by CTRL pin



Output enabled by CTRL pin. V_I = 12 V, I_O = max I_O.
TON_DELAY =0ms, TON_RISE = 5 ms.
Scale top: 0.5V/div, Scale bottom: 2 V/div, 5 ms/div.

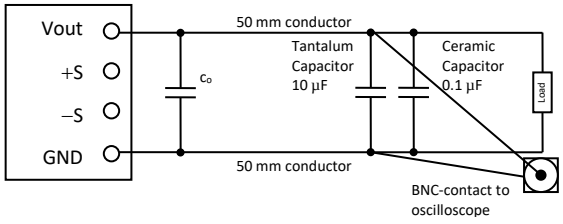
Disable by CTRL pin



Output disabled by CTRL pin. V_I = 12 V, I_O = max I_O.
Scale top: 0.5v/div, Scale bottom: 2 V/div, 0.5 ms/div.

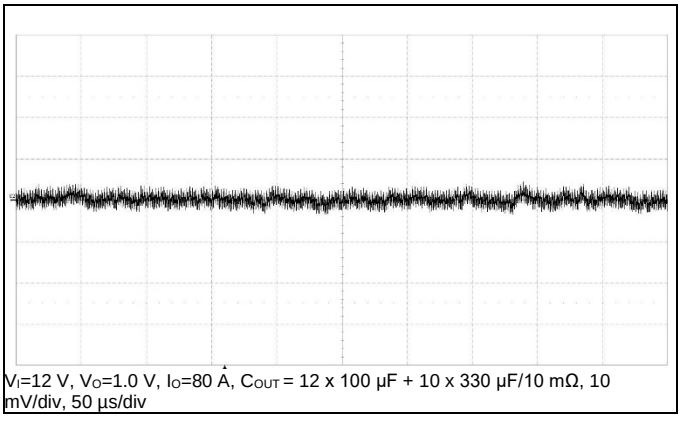
Output Ripple and Noise

Output ripple and noise are measured according to figure below. A 50 mm conductor works as a small inductor forming together with the two capacitances a damped filter.



Output ripple and noise test set-up.

The default loop compensation setting is designed to provide stability, accurate line and load regulation and good transient performance for a wide range of operating conditions (switching frequency, input voltage, output voltage, output capacitance). Inherent from the implementation and normal to the product there will be some low frequency ripple at the output, in addition to the fundamental switching frequency output ripple. This low frequency ripple is not related to instability of control loop. The total output ripple and noise is maintained at a low level.



V_I=12 V, V_O=1.0 V, I_O=80 A, C_{OUT} = 12 x 100 µF + 10 x 330 µF/10 mΩ, 10 mV/div, 50 µs/div

Example of low frequency ripple at the output.

PMBus Interface

Power Management Overview

This product incorporates a wide range of configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults.

The product's standard configuration is suitable for a wide range of operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface.

Throughout this document, different PMBus commands are referenced. A detailed description of each command is provided in the appendix at the end of this specification.

The Flex Power Designer software suite can be used to configure and monitor this product via the PMBus interface. For more information please contact your local Flex sales representative.

SMBus Interface

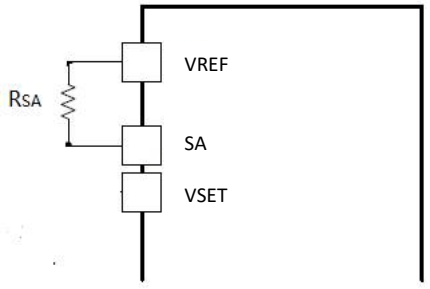
The product can be used with any standard two-wire I^2C or SMBus host device. See Electrical Specification for allowed clock frequency range. In addition, the product is compatible with PMBus version 1.2 and includes an SALERT line to help mitigate limitations related to continuous fault monitoring. The PMBus signals SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

$$\tau = R_P C_p \leq 1\mu s$$

where R_p is the pull-up resistor value and C_p is the bus loading. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.5 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.
See application note AN304 for details on interfacing the product with a microcontroller.

PMBus Addressing (SA)

The SMBus address should be configured by resistor connected between the SA pins and the VREF pin, and there is a 20k resistor inside module between SA and AGND. As shown in the Typical Application Circuit. Recommended resistor values for hard-wiring PMBus addresses are shown in the table below. 1% tolerance resistors are required.



R_{SA} [kΩ]	SMBus ADDRESS	R_{SA} [kΩ]	SMBus ADDRESS
1300	58h	16.2	6Ah
422	59h	14.3	6Bh
249	5Ah	12.4	6Ch
169	5Bh	11	6Dh
127	5Ch	9.53	6Eh
102	5Dh	8.45	6Fh
82.5	5Eh	7.15	70h
68.1	5Fh	6.19	71h
59	60h	5.11	72h
43.2	62h	4.22	73h
38.3	63h	3.4	74h
33.2	64h	2.61	75h
29.4	65h	1.87	76h
26.1	66h	1.15	77h
23.2	67h		
20.5	68h		
18.2	69h		

Reserved Addresses

Addresses listed in the table below are reserved or assigned according to the SMBus specification and may not be usable. Refer to the SMBus specification for further information.

Address	Comment
0x00	General Call Address / START byte
0x01	CBUS address
0x02	Address reserved for different bus format
0x03 - 0x07	Reserved for future use
0x08	SMBus Host
0x09 - 0x0B	Assigned for Smart Battery
0x0C	SMBus Alert Response Address
0x28	Reserved for ACCESS.bus host
0x2C - 0x2D	Reserved by previous versions of the SMBus specification

0x37	Reserved for ACCESS.bus default address
0x61	SMBus Device Default Address
0x78 - 0x7B	10-bit slave addressing
0x7C - 0x7F	Reserved for future use

Monitoring via PMBus
It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

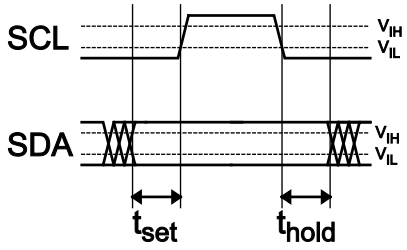
Parameter	PMBus Command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Output current	READ_IOUT
Highest temperature of smart power stage (T_{P2} or T_{P3})	READ_TEMPERATURE_1

Monitoring Faults
Fault conditions can be detected using the SALERT pin, which will be asserted low when any number of pre-configured fault or warning conditions occurs. The SALERT pin will be held low until faults and/or warnings are cleared by the CLEAR_FAULTS command, or until the output voltage has been re-enabled.
It is possible to mask which fault conditions should not assert the SALERT pin by the command MFR_SMBALERT_MASK.

In response to the SALERT signal, the user may read a number of status commands to find out what fault or warning condition occurred, see table below.

Fault & Warning Status	PMBus Command
Overview, Power Good	STATUS_WORD STATUS_BYTE
Output voltage level	STATUS_VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

PMBus / I2C Timing



Setup and hold times timing diagram.

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the falling edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. Refer to the SMBus specification, for SMBus electrical and timing requirements.

The product supports PEC (Packet Error Checking) according to the SMBus specification.

When sending subsequent commands to the same module, it is recommended to insert additional delays according to the table below.

After sending PMBus Command	Required delay before additional command
STORE_USER_ALL	100 ms
RESTORE_USER_ALL	100 ms
VOUT_MAX	10 ms
Any other command	2 ms after reading 10 ms after writing

Non-Volatile Memory (NVM)
The product incorporates one Non-Volatile Memory areas for storage of the PMBus command values, does not have different Default NVM and User NVM.

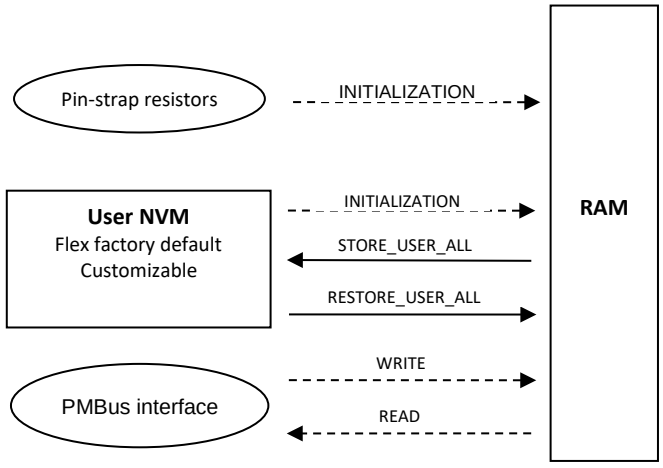


Illustration of memory areas of the product.

The User NVM is pre-loaded with Flex factory default values. The User NVM is writable and open for customization. The values in NVM are loaded during initialization according to section Initialization Procedure, whereafter commands can be changed through the PMBus Interface. The STORE_USER_ALL command will store the changed parameters to the User NVM.

Command Protection

The user may write-protect specific PMBus commands in the User NVM by using the command MFR_SPECIFIC_WRITE PROTECT

Initialization Procedure

The product follows an internal initialization procedure after power is applied to the VIN pins:

1. Self test and memory check.
2. The address pin-strap resistor is measured and the associated PMBus address is defined.
3. The output voltage pin-strap resistor is measured and the associated output voltage level will be loaded to operational RAM of PMBus command VOUT_COMMAND.
4. Values stored in the User NVM are loaded into operational RAM memory. If VOUT_COMMAND is set by pin-strap, at power up, the V_{OUT} is based on pin strap.

Once this procedure is completed and the Initialization Time will take up to 20ms to complete, the output voltage is ready to be enabled using the CTRL pin. The product is also ready to accept commands via the PMBus interface, which in case of writes will overwrite any values loaded during the initialization procedure.

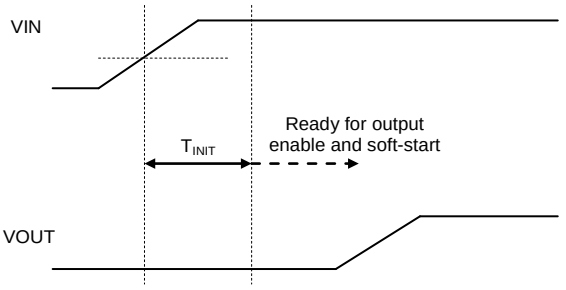


Illustration of Initialization time.

Operating Information

Input Voltage

The input voltage range 6-15V (7.5~15Vin for 3.3Vout) makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter.

Input Under Voltage Protection (IUVP)

The product monitors the input voltage and will turn-on and turn-off at configured thresholds (see Electrical Specification). The turn-on input voltage threshold is set higher than the corresponding turn-off threshold. Hence, there is a hysteresis between turn-on and turn-off input voltage levels. Once the input voltage falls below the turn-off threshold, the device can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the outupt voltage is re-enabled.
2. Immediate shutdown of output voltage while the input voltage is below the turn-off threshold. Operation resumes automatically and the output is enabled when the input voltage risen above the turn-on threshold.

The default response is option 2. The IUVP function can be reconfigured using the PMBus commands
VIN_UV_FAULT_LIMIT (turn-off threshold),
VIN_ON (turn on threshold)
VIN_UV_WARN_LIMIT (warning threshold) and
VIN_UV_FAULT_RESPONSE.

Input Over Voltage Protection (IOVP)

The product monitors the input voltage continously and will respond as configured when the input voltage rises above the configured threshold level (see Electrical Specification). Refer to section “Input Over Voltage Protection” for functionality, response configuration options and default setting.

Once the input voltage rise over the input over voltage threshold, the device can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage while the input voltage is below the threshold. Operation resumes automatically and the output is enabled when the input voltage fall below the turn-on threshold.

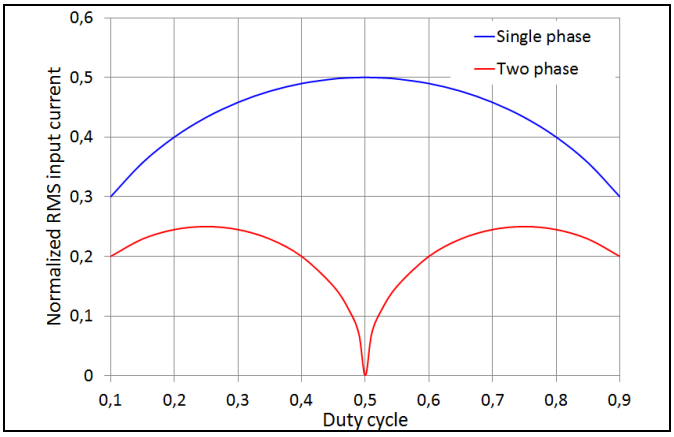
The default response is option 2. The IOVP function can be reconfigured using the PMBus commands VIN_OV_FAULT_LIMIT (turn-off threshold), VIN_OV_WARN_LIMIT (warning threshold) and VIN_OV_FAULT_RESPONSE.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. If the input voltage source contains significant inductance, the addition of a capacitor with low ESR at the input of the product will ensure stable operation.

External Input Capacitors

The product operate in a two-phase (single output) mode which gives lower input rippple, see picture below. Thus, ripple-current-rating requirements for the input capacitors are lower relatively to a single phase converter.



The input ripple RMS current in a buck converter can be estimated to

$$I_{inputRMS} = I_{load}\sqrt{D(0.5-D)}$$ (valid for $D < 0.5$, two-phase)

Where I_{load} is the output load current and D is the duty cycle. The maximum input ripple current becomes $I_{load}/4$ for two-phase from $I_{load}/2$ for single-phase. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor, and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors.

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage at large load transients.

If several products are connected in a phase spreading setup the amount of input ripple current, and capacitance per product, can be reduced. As shown in the above formula. The amount of input ripple current for such setup can be estimated using the Flex Power Designer software and capacitor selection can be made based on this number.

Ceramic input capacitors must be placed closely and with low impedance connections to the VIN and GND pins in order to be effective. See application note AN323 for further guidelines on how to choose and apply input capacitors.

External Output Capacitors

The output capacitor requirement depends on two considerations; output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to achieve a small output deviation. Improved transient response can also be achieved by adjusting the settings of the control loop of the product. Adding output capacitance decreases loop band - width.

It is recommended to locate low ESR ceramic and low ESR electrolytic/polymer capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts and cabling for more effective capacitance.

Optimization of output filter together with load step simulations can be made through the Flex Power Designer software. See application note AN321 for further guidelines on how to choose and apply output capacitors.

Control Loop

The products use a fully digital control loop that achieves precise control of the entire power conversion process, resulting in a very flexible device that is also very easy to use.

An off-time control algorithm is implemented that responds very quickly to output current changes, achieving a very small

total output voltage variation with less output capacitance than traditional PWM controllers, thus saving cost and board space. Transient response tuning is accomplished by changing the parameters using the COMPENSATION_CONFIG (USER_DATA_01) command.

Several parameters are related to control loop performance fine tuning.
DCLL: DC load line, which is V_{OUT} droop voltage, higher DCLL means lower voltage at higher current, set to 0 mΩ if droop is not used.

ACLL: AC load line, which is the gain of the proportional path, lower ACLL means higher BW which leads to fast transient response.
INT TC: Integrator time constant, lower integrator time constant means fast settling time.
RAMP: a signal has a slope proportional to the number of phases and switching frequency setting. Higher RAMP makes the loop tend towards voltage mode control, and helpful to decrease jitter.
INT Gain: the integration path gain.
AC Gain: amplify gain for compensation voltage.

All above parameters have been fine-tuned for good load transient performance, refer to the load step waveform with specified output capacitors.
Users can simply fine tune the ACLL for desired load step result and keep other parameters with default value. Lower ACLL will achieve faster transient responses, lower output undershoot and overshoot but it may affect the stability so please use it with caution.

Load transient response

The product achieves fast load transient performance using the inherently variable switching frequency characteristics off-time control. Figure 1 illustrates the load insertion behavior, in which PWM pulses are generated with faster frequency than the steady-state frequency, to provide more energy to the output voltage, improving undershoot performance. Figure 2 illustrates the load release behavior, in which PWM pulses can be delayed to avoiding charging extra energy to the load until the output voltage reaches the peak overshoot.
When there is a sudden load increase, the output voltage immediately drops. The controller device reacts to this drop by lowering the voltage on internal VCOMP signal. This forces PWM pulses to fire more frequently, which causes the inductor current to rapidly increase. As the converter output current reaches the new load current, the device reaches a steady-state operating condition and the PWM switching resumes the steady-state frequency.
When there is a sudden load release, the output voltage immediately overshoots. The control loop reacts to this rise by increasing the voltage of the internal VCOMP signal. This rise forces the PWM pulses to be delayed until the converter output current reaches the new load current. At that point, the switching resumes and steady - state switching continues.

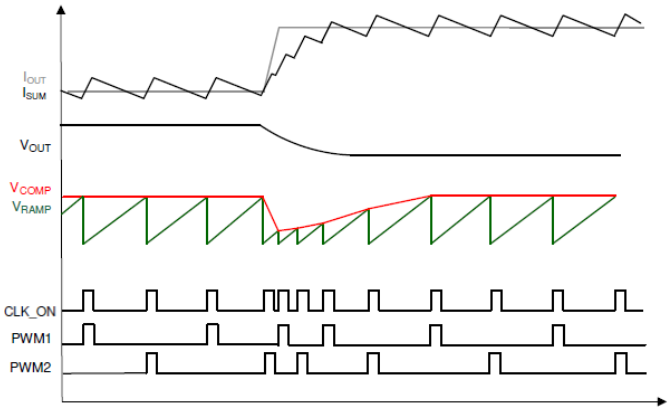


Figure 1 Load insertion response

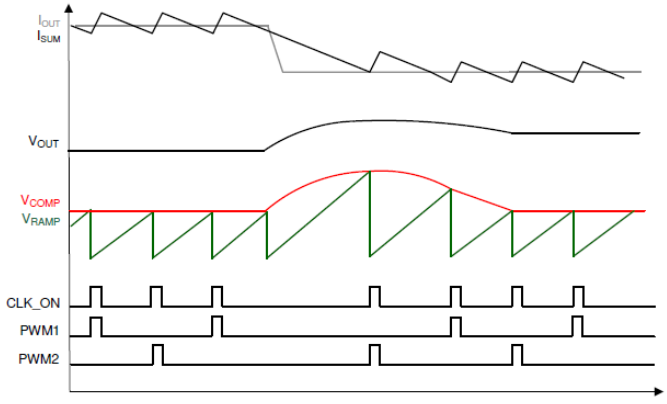
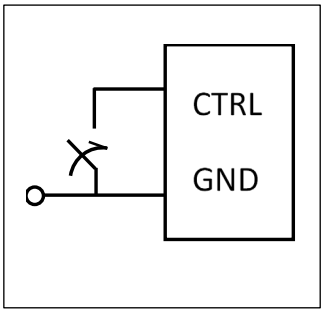


Figure 2 Load release response

Remote Sense

The following options are available to enable and disable this device:

1. Output voltage is enabled through the CTRL pin.



The product is equipped with remote control function. The CTRL pin polarity can be configured active high or active low using PMBus command ON_OFF_CONFIG. In active high (positive) mode, CTRL pin should be left open to turn on product. Turn off is achieved by connecting the CTRL pin to GND. And active low (negative) vice versa.

2. Output voltage is enabled using the PMBus command OPERATION.

The CTRL pin has an internal 10 kΩ pull-up resistor to 3.3 V. The external device must have a sufficient sink current ability

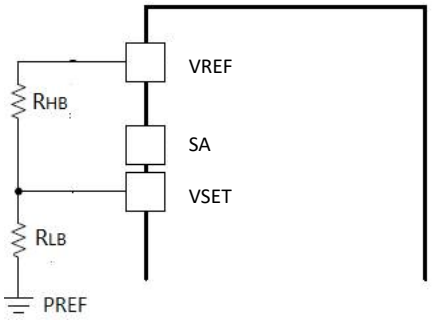
to be able pull CTRL pin voltage down below logic low threshold level (see Electrical Characteristics). When the CTRL pin is left open, the voltage on the CTRL pin is pulled up to 3.3V.

The CTRL pins should be held low whenver a configuration file or script is used to configure the module, or a PMBus command ON_OFF_CONFIG is sent that could potentially damage the application circuit.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to enabling the output voltage.

Output Voltage Adjust using Pin-strap Resistor

Using an external pin-strap resistor divider, R_{HB} and R_{LB}, the output voltage can be set to several predefined levels shown in the Table 1. Only the voltage levels specified in the table can be set by resistor divider. The resistor should be applied between the VREF pin and the PREF pin as shown in the Typical Application Circuit. Maximum 1% tolerance resistors are required.



The resistor is sensed only during the initialization procedure after input voltage is applied. Changing the resistor value during normal operation will not change the output voltage.

Output Voltage Adjust using PMBus

The module can also use the PMBus command to set the output voltage. After setting the register PIN_DETECT_OVERRIDE(EEh) as below:

Config the 'PD BOOT' with 'NVM', then use VOUT_COMMAND to set the output voltage.
Make sure a new VOUT_COMMAND is not sent 15 ms prior to enabling the output, until after power good (PG) is asserted.

Voltage Margining Up/Down

Using the PMBus interface, it is possible to adjust the output voltage to predefined levels above or below the nominal voltage setting in order to determine whether the load device is capable of operating outside its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit outside its typical operating range. This functionality can also be used to test of supply voltage supervisors. The margin limits can be reconfigured using the PMBus commands VOUT_MARGIN_LOW and VOUT_MARGIN_HIGH. Margining is activated by the command OPERATION and can be used regardless of the output voltage being enabled by the CTRL pin or by the PMBus.

Output Voltage Range Limitation

The output voltage range that is possible to set by configuration or by the PMBus interface, it is hardware limited by the pin-strap resistor divider also.

Vout pinstrap value	VOUT_SCALE_LOOP	VOUT_MAX default value
0.6 to 1.87V	1.00	1.870V
1.880 to 3.3V	1.00	3.740V

VOUT_MAX default for when pin-strap set V_{OUT}

When using pin-strap to set V_{OUT}, the default maximum output voltage is set to the value in above table. This protects the application circuit from an over voltage in case accidental PMBus command.
The output voltage limit can be reconfigured to a lower value than default value by writing the PMBus command VOUT_MAX.

Output Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. Support two-stage overvoltage protection, Tracking OVP and Fixed OVP.
For Tracking OVP, the VOUT_OV_FAULT_LIMIT sets an over-voltage threshold relative to the current VOUT. Updates the VOUT_COMMAND cause the value of VOUT_OV_FAULT_LIMIT to be re-calculated, but do not change the actual offset threshold.

The default OVP threshold is 0.192V above the current output voltage. The product can be configured to respond in different ways to the output voltage exceeding the OVP limit:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continous restart attempts of the output voltage with a preset interval ("hiccup" mode).

The default response is option 1. The OVP limit and fault response can be reconfigured using the PMBus commands

VOUT_OV_FAULT_LIMIT, VOUT_OV_FAULT_RESPONSE and VOUT_OV_WARN_LIMIT.

For Fixed OVP, it is a fixed limit, V_{OUT} above which is not safe to operate. If triggered power conversion is disabled, this fault is treated as potentially catastrophic, and can't be cleared without a power recycle. The default value is 3.6V. It is programable through MFR_PROTECTIOM_CONFIG command.

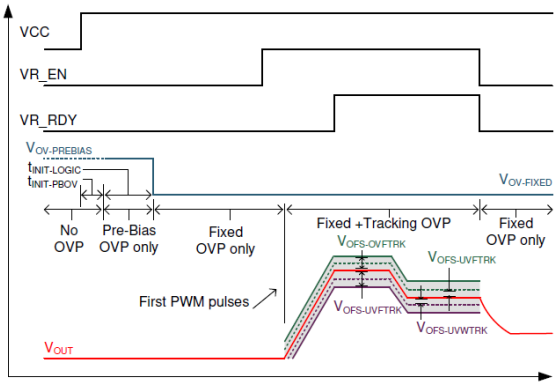
Output Under Voltage Protection (UVP)

The product includes output under voltage limiting circuitry for protection of the load. Support Tracking UVP protection. For Tracking UVP, VOUT_UV_FAULT_LIMIT sets an under-voltage threshold relative to the current VOUT. Updates the VOUT_COMMAND cause the value of OUT_UV_FAULT_LIMIT to be re-calculated, but do not change the actual offset threshold.

The default UVP threshold is 0.192V below the current output voltage. The product can be configured to respond in different ways to the output voltage below the UVP limit:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continous restart attempts of the output voltage with a preset interval ("hiccup" mode).

The default response is option 1. The UVP limit and fault response can be reconfigured using the PMBus commands VOUT_UV_FAULT_LIMIT, VOUT_UV_FAULT_RESPONSE and VOUT_UV_WARN_LIMIT.



Over voltage and under voltage protection

Power Good

The power good pin (PG) is used to signal to the system, indicates when the product is ready to provide regulated output voltage to the load. Any condition which causes the module stop, PG will be held low.

Over Current Protection (OCP)

The product includes robust current limiting circuitry for protection at continuous overload. After ramp-up is complete the product can detect an output overload/short condition. The following OCP response options are available:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continous restart attempts of the output voltage with a preset interval ("hiccup" mode).

The default response is option 1. Note that delayed shutdown is not supported. The load distribution should be designed lower than the specified Maximum output current. The OCP limit and response can be reconfigured using the PMBus commands IOUT_ OC_FAULT_LIMIT and IOUT_OC_FAULT_RESPONSE.

Under Current Protection (UCP)

The product includes robust current limiting circuitry for protection at continuous reversed current. Refer to section Over Current Protection for response configuration options and default setting. The UCP limit and response can be reconfigured using the PMBus commands IOUT_UC_FAULT_LIMIT and IOUT_UC_FAULT_RESPONSE.

Switching Frequency

The switching frequency can be re-configured in a certain range using the PMBus command FREQUENCY_SWITCH. Refer to Electrical Specification for default switching frequency and range.

Changing the switching frequency will affect efficiency and power dissipation, load transient response (control loop characteristics) and output ripple. Control loop settings may need to be adjusted. For more information, please contact with your local sales representative.

Note that the effective switching frequency will be twice as much as the configured one since the product has two phases.

For output voltage range from 0.6V to 1.8V, the default switching frequency is 500KHz. And for output voltage range from 2.5V to 3.3V, 800KHz would be better to improve idling power and ripple.

Synchronization

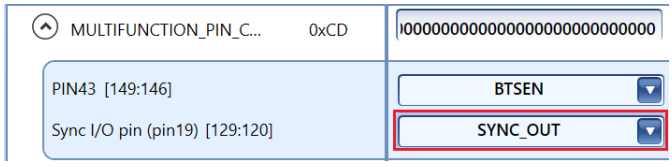
Two or more products may be synchronized with an external clock to eliminate beat frequencies reflected back to the input supply rail. Eliminating the slow beat frequencies (usually <10 kHz) releases the filtering requirements. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.

The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC output, working as a source of synchronization signal for other products connected to the same synchronization line. The SYNC pin of products being synchronized must be configured as SYNC Input. Default configuration is using the internal clock, independently of signal at the SYNC pin. Synchronization is configured using PMBus commands SYNC_CONFIG.

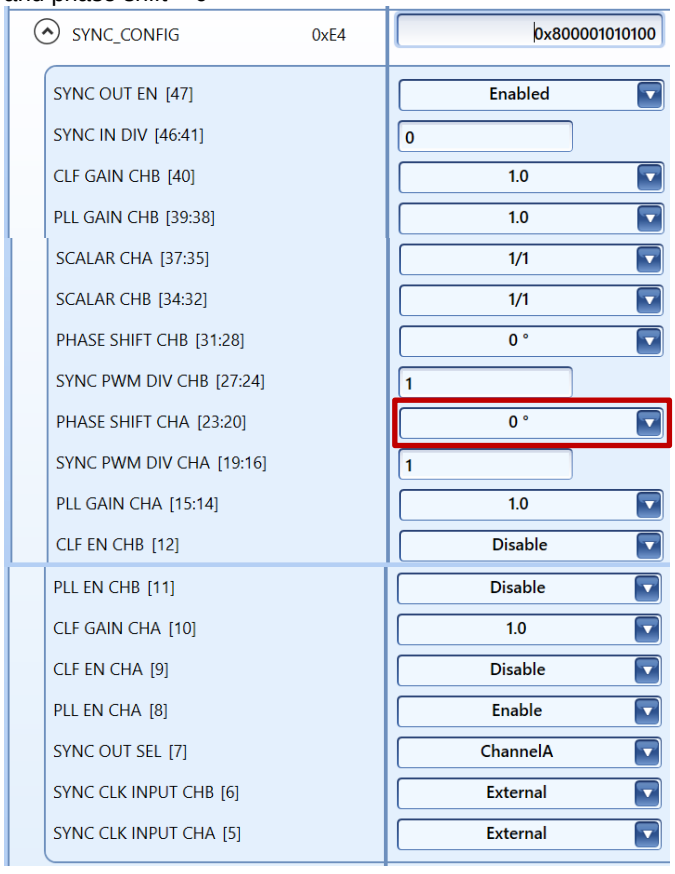
First, use the MULTIFUNCTION_PIN_CONFIG command to assign pin 19 as 'SYNC IN' or 'SYNC OUT'. Then use SYNC_CONFIG for detailed sync function configuration.

SYNC OUT configration:

1, MULTIFUNCTION_PIN_CONFIG: assign pin 19 as 'SYNC OUT'

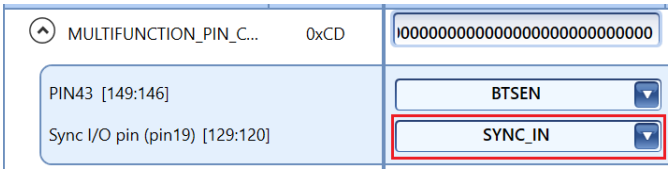


2, SYNC_CONFIG: configuration as below for 'SYNC OUT', and phase shift = 0°

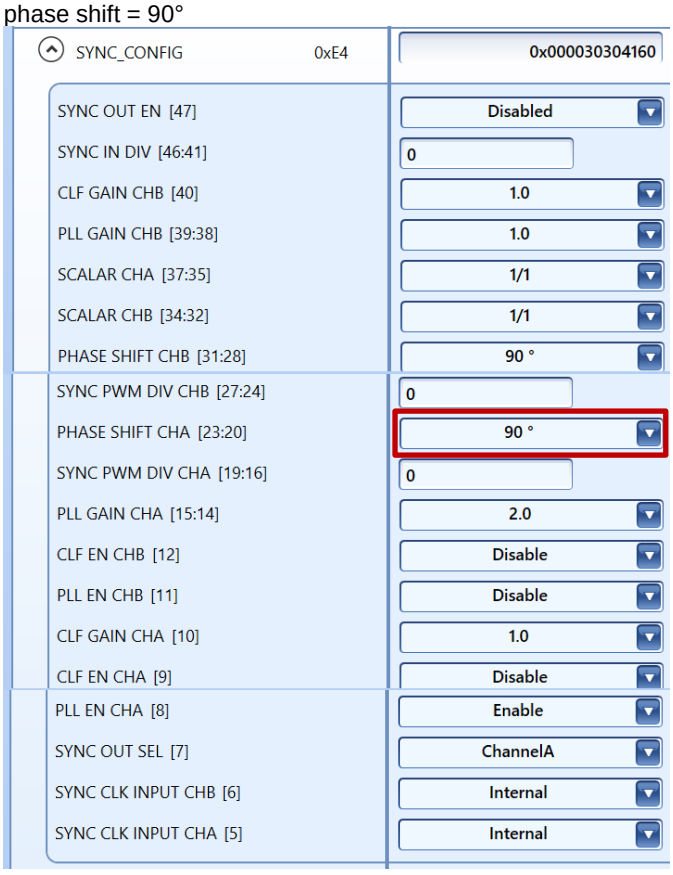


SYNC IN configration:

1, MULTIFUNCTION_PIN_CONFIG: assign pin 19 as 'SYNC IN'



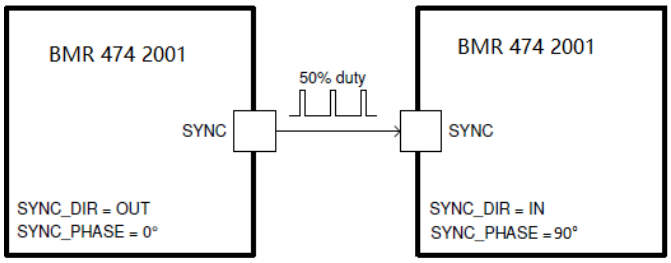
2, SYNC_CONFIG: configuration as below for 'SYNC IN', and phase shift = 90°



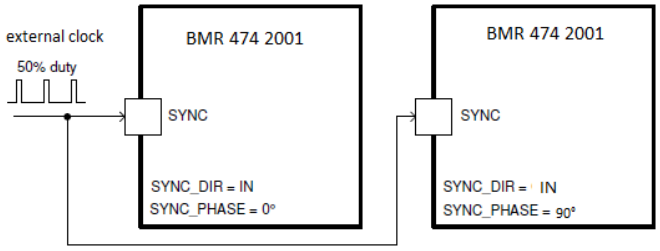
Note: SYNC modification is blocked while the output voltage is regulated. Please disable the module before SYNC configuration.

Phase Spreading

Below pictures illustrate 2 common methods of synchronizing multiple modules.



Clock master module drive a clock slave module



External clock drive 2 clock slave module

Use the 'Flex Power Designer' to config the 'phase shift' parameter in SYNC_CONFIG, will implement the phase spreading of multiple modules. to improve ripple cancellation and reduce beat frequencies on input supply.

BMR 474 2001 is a dual phase module, internally the PWM1 and PWM2 has 180° shift. So, for multiple module in sync group, use 360°/2n for phase shift configuration (n: the module number for synchronization), for example:

1 SYNC OUT, 1 SYNC IN	Phase shift configuration	PWM1	PWM2
SYNC OUT module	0°	0°	180°
SYNC IN module	90°	90°	270°

1 SYNC OUT, 2 SYNC IN	Phase shift configuration	PWM1	PWM2
SYNC OUT module	0°	0°	180°
SYNC IN module1	60°	60°	240°
SYNC IN module2	120°	120°	300°
.....	.....	.....	.....

Soft-start and Soft-stop

The soft-start and soft-stop control functionality allows the output voltage to ramp-up and ramp-down with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple controllers.
The rise time is the time taken for the output to ramp to its target voltage, while the fall time is the time taken for the output to ramp down from its regulation voltage to 0 V. The on-delay time sets a delay from when the output is enabled until the output voltage starts to ramp up. The off-delay time sets a delay from when the output is disabled until the output voltage starts to ramp down.

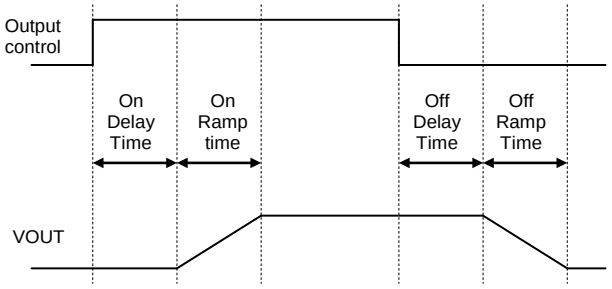


Illustration of Soft-Start and Soft-Stop.

In standard configuration soft-stop is disabled and the regulation of output voltage stops immediately when the output is disabled. Soft-stop can be enabled through the PMBus command ON_OFF_CONFIG. The delay and ramp times can be reconfigured using the PMBus commands TON_DELAY, TON_RISE, TOFF_DELAY and TOFF_FALL.

Output Voltage Sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs and ASICs that require one supply to reach its operating voltage prior to another.

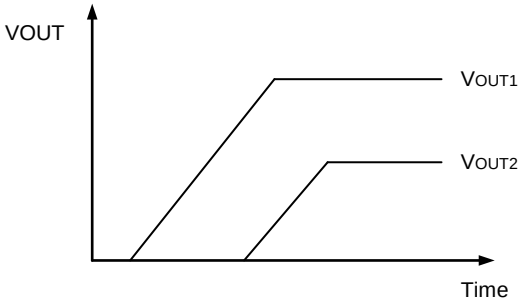


Illustration of Output Voltage Sequencing.

Different types of multi-product sequencing are supported:

1. Time based sequencing. Configuring the start delay and rise time of each module through the PMBus interface and by connecting the CTRL pin of each product to a common enable signal.

2. Event based sequencing. Routing the PG pin signal of one module to the CTRL pin of the next module in the sequence.

These sequencing options are easily configured using the Flex Power Designer software. See application note AN310 for further information.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. There could also be still charged output capacitors when starting up shortly after turn-off.
The product incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition.

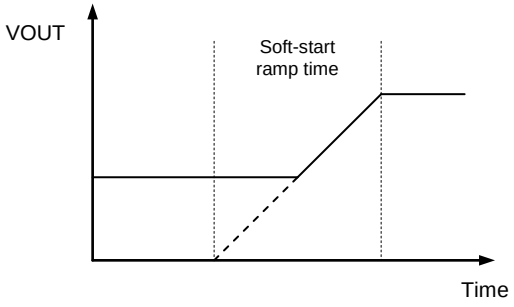


Illustration of Pre-Bias Startup.

Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Output section for each model provides the available output current versus ambient air temperature and air velocity at specified V_I.

The product is tested on a 254 x 254 mm, 35 µm (1 oz) test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 8 layers.

Note that the cooling via power pins does not only have to handle the power loss from the module. A low resistance between module and target device is of major importance to reduce additional power loss.

See Design Note 019 for further information.

Definition of Product Operating Temperature

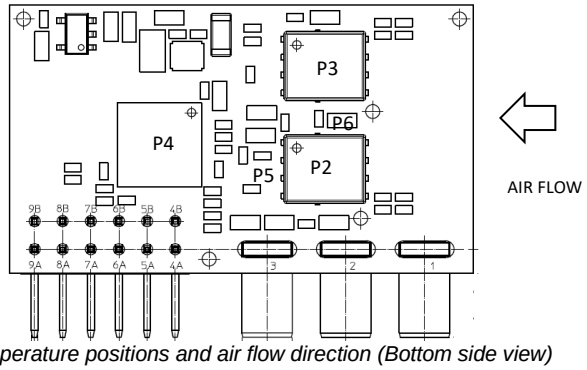
The temperature at positions P1, P2, P3, P4, P5 and P6 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above specified maximum measured at the specified positions are not allowed and may cause permanent damage.

Position	Description	Max Temperature
P1	Power inductor, Reference point	T_{P1} = 125 °C
P2, P3	Smart Power Stage Hot spot	T_{P2}, T_{P3}= 125 °C
P4	Controller	T_{P4} = 125°C
P5	PCB	T_{P5} = 125°C
P6	C19, ceramic capacitor	T_{P6} = 120°C

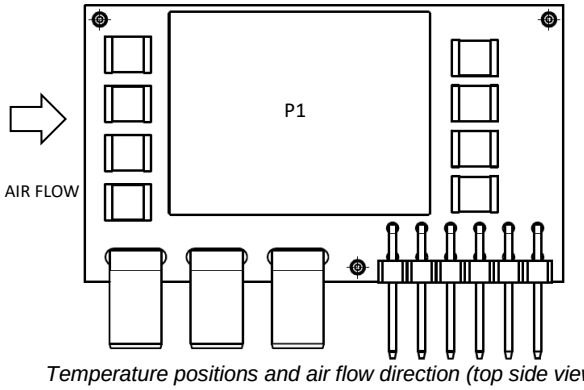
Since it is not easy to measure P6 (ceramic capacitor), and easier to measure P1, measuring the temperature at only position P1 is an alternative method to verify proper thermal conditions.

Using PMBus command READ_TEMPERATURE will get the highest temperature of TP2 or TP3.

Horizontal Direction



Temperature positions and air flow direction (Bottom side view)



Temperature positions and air flow direction (top side view)

Definition of Reference Temperature TP1

The temperature at position P1 has been used as a reference temperature for the Electrical Specification data provided.

Over Temperature Protection (OTP)

The products are protected from thermal overload by an internal over temperature shutdown function in the controller, which measure the temperature of the power stage.

The internal temperature of power stage is continuously monitored and when the temperature rises above the configured OTP threshold the product will respond as configured. The product can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage while the temperature is above the fault threshold. Operation resumes automatically and the output is enabled when the temperature has fallen below the warning threshold, i.e. there is a hysteresis defined by the difference between the fault threshold and the warning threshold.

Default configuration is option 1. The default OTP threshold and hysteresis are specified in Electrical Characteristics.

The OTP limit and response are configured using the PMBus commands OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE.

PCB Layout Consideration

The radiated EMI performance of the product will depend on the PCB layout and ground layer design. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.
A ground layer will increase the stray capacitance in the PCB and improve the high frequency EMC performance.

Further layout recommendations are listed below.

- The pin strap resistors, R_{SA}, and R_{VSET} divider should be placed as close to the product as possible to minimize loops that may pick up noise. Avoid capacitive load on these signals as it may result in false pin strap reading.
- In remote sense compensation application, care should be taken in the routing of the connections from the point of load to the S+ and S- terminals, preferably between ground planes which are not carrying high currents. The routing should avoid areas of high electric or magnetic fields. So in host board, it is strongly recommend that the sense traces should not be laid on the module's top side direction, but laid on the module's bottom side direction instead, and should be laid out as a differential pair and be shielded by the PCB ground layer to reduce noise susceptibility. In the layer above and below the sense trace, there are large area PGND copper laid which provide good shield for S+/S-. (see Figure 3 sense+/- layout example)

If the remote sense compensation is not used, please leave the sense+ and sense- open, needn't connect to power pin.

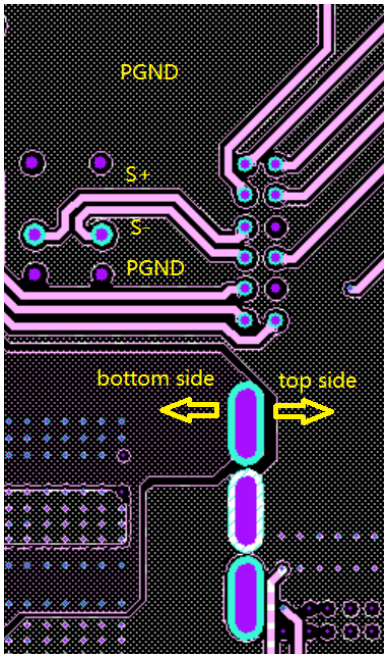


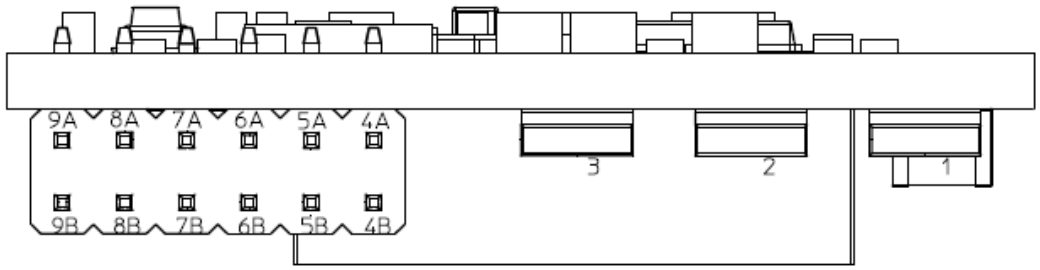
Figure 3 sense+/- layout example

- Avoid current carrying planes under the pin strap resistors and the PMBus signals.
- The capacitors C_{IN} should be placed as close to the input pins as possible and with low impedance connections, e.g. using via stitching around capacitors' terminals. See AN323 for more details.
- The capacitors C_{OUT} should in general be placed close to the load. However typically you would like to place larger ceramic output capacitors close to the module output in order to handle the output ripple current. See AN321 for more details. Low impedance connections must be used, e.g. via stitching around capacitors' terminals.
- The modules should be placed closely to the ASIC for better performance. Since the overshoot voltage during step is followed V=L*di/dt, the L is the PCB power trace inductance, if PCB impedance is high, the overshoot voltage may be high.
- If possibly use planes on several layers to carry V_I, V_O and GND, there should be a large number of vias close to the VIN, VOUT and GND pads in order to lower input and output impedances and improve heat spreading between the product and the host board. Minimum total copper thickness of VOUT and GND layers respectively need to be 140 µm (4 oz) in order to distribute maximum current without unacceptable losses.

Table 1 Output Voltage Adjust using Pin-strap Resistors

R_{LB} = 20.0 kΩ		R_{LB} = 27.4 kΩ		R_{LB} = 37.4 kΩ		R_{LB} = 49.9 kΩ		R_{LB} = 64.9 kΩ		R_{LB} = 86.6 kΩ		R_{LB} = 115.0 kΩ		R_{LB} = 154.0 kΩ	
V_{OUT} (V)	R_{HB}(kΩ)	V_{OUT} (V)	R_{HB}(kΩ)	V_{OUT} (V)	R_{HB}(kΩ)	V_{OUT} (V)	R_{HB}(kΩ)	V_{OUT} (V)	R_{HB}(kΩ)	V_{OUT} (V)	R_{HB}(kΩ)	V_{OUT} (V)	R_{HB}(kΩ)	V_{OUT} (V)	R_{HB}(kΩ)
Do not use								0.6	412	0.61	549	0.62	732	0.63	976
0.64	102	0.65	140	0.66	191	0.67	255	0.68	332	0.69	442	0.7	576	0.71	787
0.72	82.5	0.73	113	0.74	154	0.75	205	0.76	267	0.77	357	0.78	475	0.79	634
0.8	68.1	0.81	95.3	0.82	130	0.83	174	0.84	226	0.85	301	0.86	392	0.87	536
0.88	59	0.89	80.6	0.90	110	0.91	147	0.92	191	0.93	255	0.94	332	0.95	453
0.96	49.9	0.97	68.1	0.98	93.1	0.99	124	1	162	1.01	215	1.02	287	1.03	383
1.04	43.2	1.05	59	1.06	80.6	1.07	110	1.08	140	1.09	187	1.1	249	1.11	332
1.12	38.3	1.13	52.3	1.14	71.5	1.15	95.3	1.16	124	1.17	165	1.18	221	1.19	294
1.2	33.2	1.21	45.3	1.22	61.9	1.23	82.5	1.24	107	1.25	143	1.26	191	1.27	255
1.28	29.4	1.29	40.2	1.3	54.9	1.31	73.2	1.32	95.3	1.33	127	1.34	169	1.35	226
1.36	26.1	1.37	35.7	1.38	48.7	1.39	64.9	1.4	84.5	1.41	113	1.42	150	1.43	200
1.44	23.2	1.45	31.6	1.46	43.2	1.47	57.6	1.48	75	1.49	97.6	1.5	133	1.51	178
1.52	20.5	1.53	28	1.54	38.3	1.55	51.1	1.56	66.5	1.57	88.7	1.58	118	1.59	158
1. 6	18.2	1.61	24.9	1.62	34	1.63	45.3	1.64	59	1.65	78.7	1.66	105	1.67	140
1.68	16.2	1.69	22.1	1.7	30.1	1. 71	40.2	1.72	52.3	1.73	69.8	1.74	93.1	1.75	124
1.76	14.3	1.77	19.6	1.78	26.7	1.79	35.7	1.8	46.4	1.81	61.9	1.82	82.5	1.83	110
1.84	12.4	1.85	17.4	1.86	23.2	1.87	30.9	1.88	40.2	1.89	53.6	1.9	71.5	1.91	95.3
1.92	11	1.93	15	1.94	20.5	1.95	27.4	1.96	35.7	1.97	47.5	1.98	63.4	1.99	84.5
2	9.53	2.01	13.3	2.02	18.2	2.03	24.3	2.04	30.9	2.05	41.2	2.06	54.9	2.07	75
2.08	8.45	2.09	11.5	2.1	15.8	2.11	21	2.12	27.4	2.13	36.5	2.14	48.7	2.15	64.9
2.16	7.15	2.17	9. 76	2.18	13.3	2.19	17.8	2.2	23.2	2.21	30.9	2.22	41.2	2.23	54.9
2.24	6.19	2.25	8.45	2.26	11.5	2.27	15.4	2.28	20	2.29	26.7	2.30	35.7	2.31	47.5
2.32	5.11	2.33	7.15	2.34	9.53	2.35	13	2.36	16.9	2.37	22.1	2.38	29.4	2.39	40.2
2.4	4.22	2.41	5.76	2.42	7.87	2.43	10.5	2.44	13.7	2.45	18.2	2.46	24.3	2.47	32.4
2.48	3.4	2.49	4.64	2.50	6.34	2.51	8.45	2.52	11	2.53	14.7	2.54	19.6	2.55	26.1
2.56	2.61	2.57	3.57	2.58	4.87	2.59	6.49	2.60	8.45	2.61	11.3	2.62	15	2.63	20
2.64	1.87	2.65	2.55	2.66	3.48	2.67	4.64	2.68	6.04	2.69	8.06	2.70	10.7	2.71	14.3
2.72	1.15	2.73	1.58	2.74	2.15	2.75	2.87	2.76	3.74	2.77	4.99	3.3	6.65	Do not use	

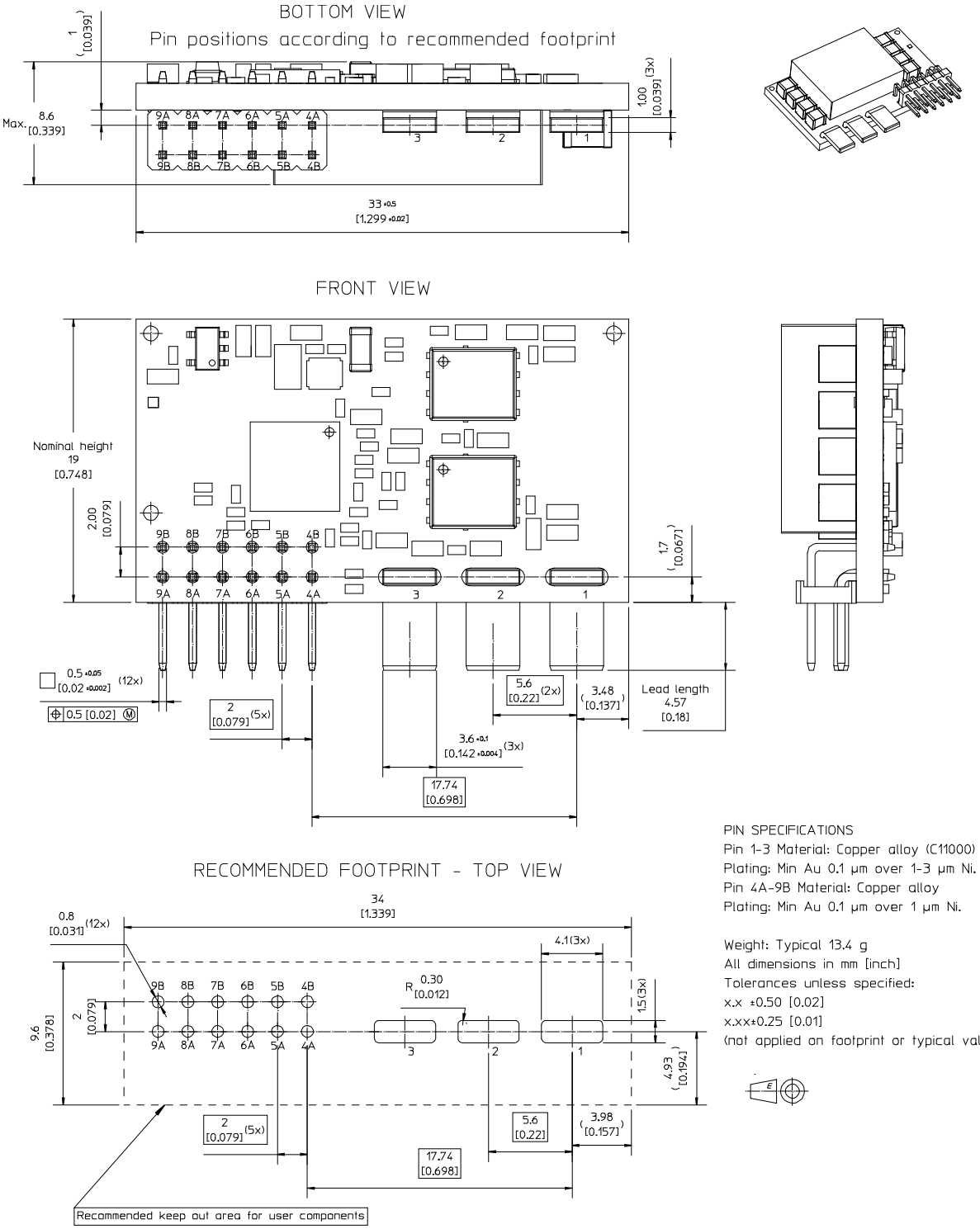
Pin Descriptions – SIP version



Pin layout, top view.

Pin	Designation	Type	Function
1	VIN	Power	Input Voltage
2	GND	Power	Power Ground
3	VOUT	Power	Output Voltage
4A	VREF	Power	Reference voltage for pin strap voltage
4B	SA	I	PMBus address pin strap. Used with external resistor to assign an unique PMBus address to the product.
5A	PREF	Power	Pin strap reference. Ground reference for pin-strap resistors.
5B	CTRL	I	Remote Control. Can be used to enable/disable the output voltage of the product. May be left open if it is unused due to internal pull-up.
6A	S-	I	Negative sense. Connect to power ground close to the load. Leave it open when it is unused.
6B	SYNC	I/O	External switching frequency synchronization input or output. Left open if it is unused.
7A	S+	I	Positive sense. Connect to output voltage close to the load. Leave it open when it is unused.
7B	VSET	I	Output voltage pin strap. Used with external resistor to set the nominal output voltage.
8A	SALERT	O Open-Drain	PMBus Alert. Asserted low when any of the configured protection mechanisms indicate a fault or a warning. Requires a pull-up resistor even when it is unused.
8B	PG	O Open-Drain	Power Good output. Asserted high when the product is ready to provide regulated output voltage to the load. It can be left open if it's unused.
9A	SDA	I/O	PMBus Data. Data signal for PMBus communication. Requires a pull-up resistor even when it is unused.
9B	SCL	I/O	PMBus Clock. Clock for PMBus communication. Requires a pull-up resistor even when it is unused.

Mechanical Information – SIP Mount Version

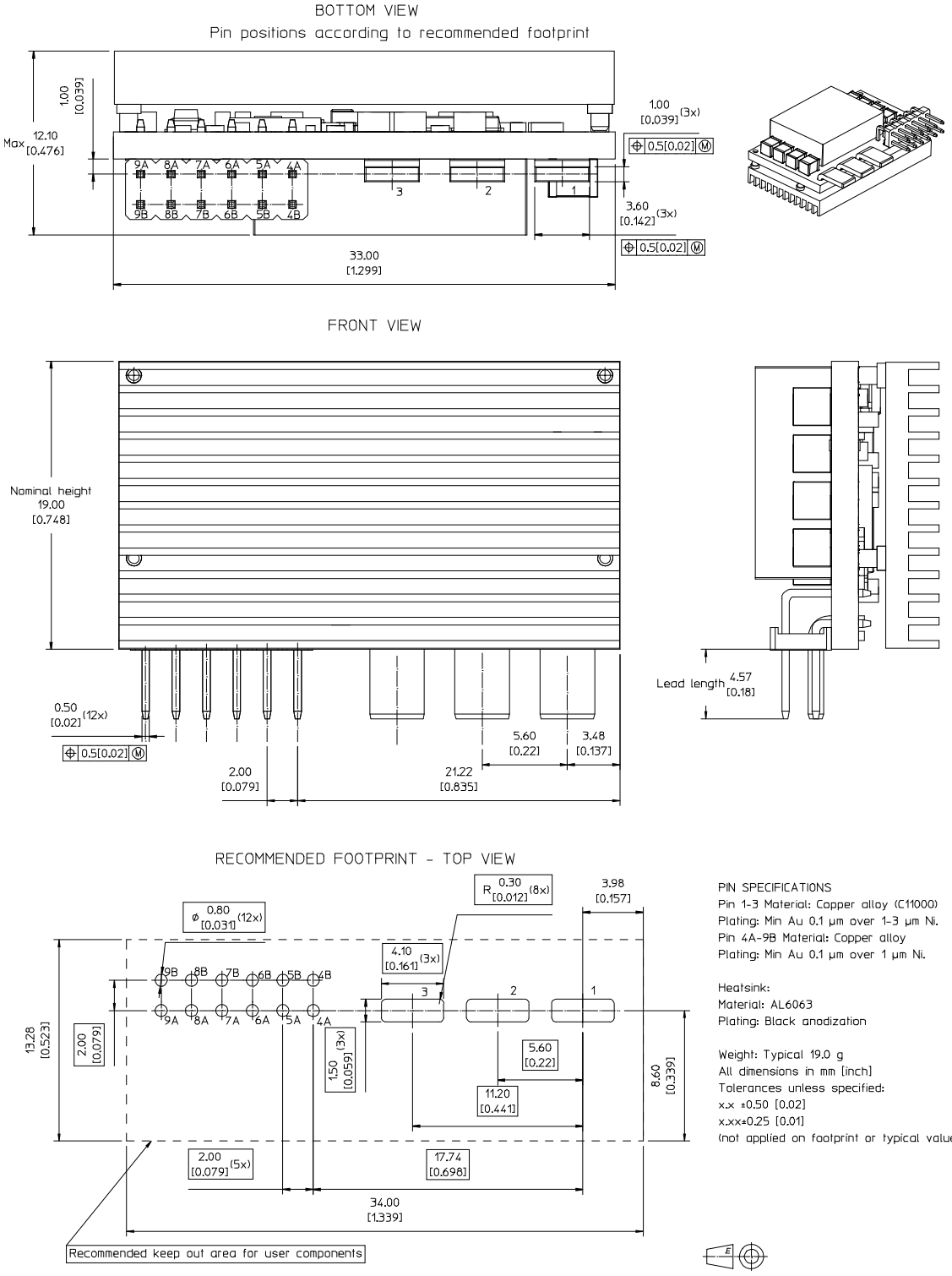


PIN SPECIFICATIONS
Pin 1-3 Material: Copper alloy (C11000)
Plating: Min Au 0.1 µm over 1-3 µm Ni.
Pin 4A-9B Material: Copper alloy
Plating: Min Au 0.1 µm over 1 µm Ni.

Weight: Typical 13.4 g
All dimensions in mm [inch]
Tolerances unless specified:
x.x ±0.50 [0.02]
x.xx±0.25 [0.01]
(not applied on footprint or typical values)

All component placements – whether shown as physical components or symbolical outline – are for reference only and are subject to change throughout the product's life cycle, unless explicitly described and dimensioned in this drawing.

Mechanical Information – Heatsink Version



All component placements – whether shown as physical components or symbolical outline – are for reference only and are subject to change throughout the product's life cycle, unless explicitly described and dimensioned in this drawing.

Soldering Information - Hole Mounting (SIP version)

The product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

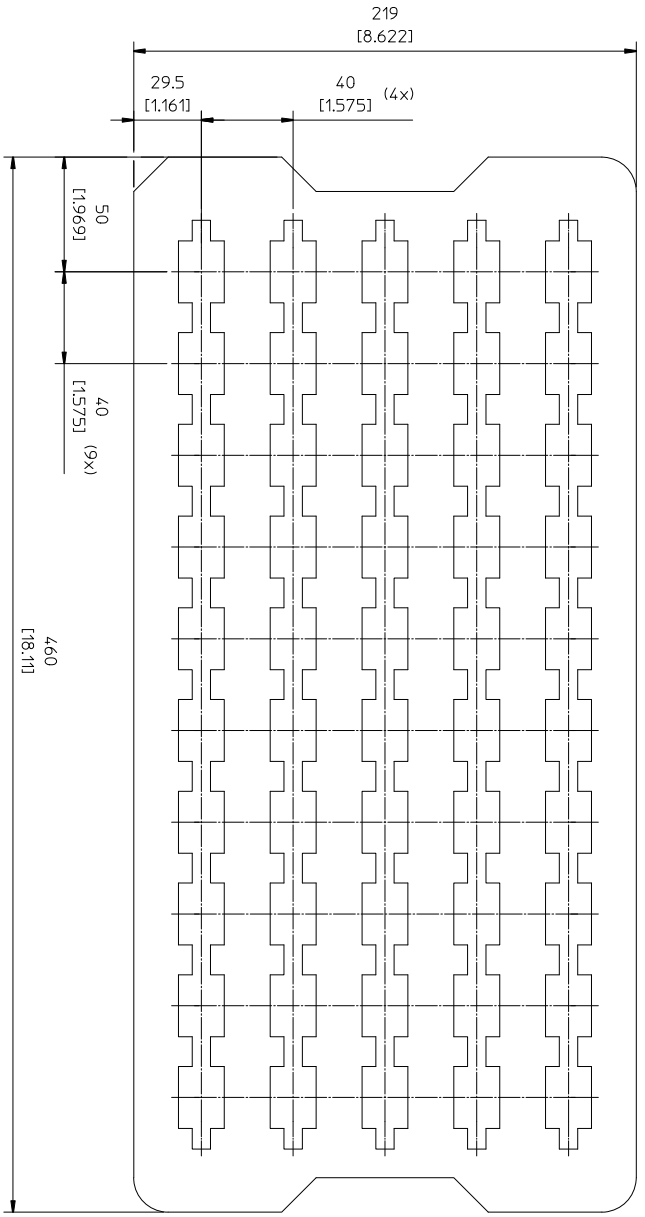
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

Delivery Package Information (SIP version)

The products are delivered in antistatic trays

Tray Specifications	
Material	Antistatic Polyethylene foam
Surface resistance	10^5< Ohms/square <10^{11}
Bakability	The trays are not bakeable
Tray thickness	18 mm [0.709 inch] for SIP version 23 mm [0.906 inch] for SIP with heatsink version
Box capacity	100 products, 2 full trays/box)
Tray weight	35 g empty tray, 705 g full tray (SIP version) 40 g empty tray, 990 g full tray (SIP with heatsink version)



Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T_A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether	55°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-20 test Ta	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g^2/Hz 10 min in each direction

PMBus Command Appendix

This appendix contains a detailed reference of the PMBus commands supported by the product.

Data Formats
The products make use of a few standardized numerical formats, along with custom data formats. A detailed walkthrough of the above formats is provided in AN304, as well as in sections 7 and 8 of the PMBus Specification Part II. The custom data formats vary depending on the command and are detailed in the command description.

Standard Commands
The functionality of commands with code 0x00 to 0xCF is usually based on the corresponding command specification provided in the PMBus Standard Specification Part II (see Power System Management Bus Protocol Documents below). However there might be different interpretations of the PMBus Standard Specification or only parts of the Standard Specification applied, thus the detailed command description below should always be consulted.

Forum Websites
The System Management Interface Forum (SMIF)
http://www.powersig.org/
The System Management Interface Forum (SMIF) supports the rapid advancement of an efficient and compatible technology base that promotes power management and systems technology implementations. The SMIF provides a membership path for any company or individual to be active participants in any or all of the various working groups established by the implementer forums.

Power Management Bus Implementers Forum
(PMBUS-IF)
http://pmbus.org/
The PMBus-IF supports the advancement and early adoption of the PMBus protocol for power management. This website offers recent PMBus specification documents, PMBus articles, as well as upcoming PMBus presentations and seminars, PMBus Document Review Board (DRB) meeting notes, and other PMBus related news.

PMBus – Power System Management Bus Protocol Documents
These specification documents may be obtained from the PMBus-IF website described above. These are required reading for complete understanding of the PMBus implementation. This appendix will not re-address all of the details contained within the two PMBus Specification documents.

Specification Part I – General Requirements Transport And Electrical Interface
Includes the general requirements, defines the transport and electrical interface and timing requirements of hard wired signals.

Specification Part II – Command Language
Describes the operation of commands, data formats, fault management and defines the command language used with the PMBus.

SMBus – System Management Bus Documents
System Management Bus Specification, Version 2.0, August 3, 2000
This specification specifies the version of the SMBus on which Revision 1.2 of the PMBus Specification is based. This specification is freely available from the System Management Interface Forum Web site at:
http://www.smbus.org/specs/

PMBus Command Summary and Factory Default Values of Standard Configuration

The factory default values provided in the table below are valid for the Standard configuration. Factory default values for other configurations can be found using the Flex Power Designer tool.

Code	Name	Data Format	Factory Default Value Standard Configuration BMR_474_2001/001 R1	
0x00	PAGE	R/W Byte	0x00	
0x01	OPERATION (Page 0)	R/W Byte	0x00	
0x01	OPERATION (Page 1)	R/W Byte	0x00	
0x02	ON_OFF_CONFIG (Page 0)	R/W Byte	0x17	
0x02	ON_OFF_CONFIG (Page 1)	R/W Byte	0x17	
0x03	CLEAR_FAULTS	Send Byte		
0x04	PHASE (Page 0)	R/W Byte	0xFF	
0x04	PHASE (Page 1)	R/W Byte	0xFF	
0x10	WRITE_PROTECT	R/W Byte	0x00	
0x11	STORE_DEFAULT_ALL	Send Byte		
0x12	RESTORE_DEFAULT_ALL	Send Byte		
0x15	STORE_USER_ALL	Send Byte		
0x16	RESTORE_USER_ALL	Send Byte		
0x1B	SMBALERT_MASK (STATUS_VOUT)	SMBAlert Mask	0x00	
0x1B	SMBALERT_MASK (STATUS_IOUT)	SMBAlert Mask	0x20	
0x1B	SMBALERT_MASK (STATUS_INPUT)	SMBAlert Mask	0x08	
0x1B	SMBALERT_MASK (STATUS_TEMPERATURE)	SMBAlert Mask	0x00	
0x1B	SMBALERT_MASK (STATUS_CML)	SMBAlert Mask	0x00	
0x1B	SMBALERT_MASK (STATUS_MFR_SPECIFIC)	SMBAlert Mask	0x26	
0x20	VOUT_MODE (Page 0)	Read Byte	0x16	
0x20	VOUT_MODE (Page 1)	Read Byte	0x16	
0x21	VOUT_COMMAND (Page 0)	R/W Word	1 x Vout by pin-strap	
0x21	VOUT_COMMAND (Page 1)	R/W Word	1 x Vout by pin-strap	
0x22	VOUT_TRIM (Page 0)	R/W Word	0x0000	0.0 V
0x22	VOUT_TRIM (Page 1)	R/W Word	0x0000	0.0 V
0x24	VOUT_MAX (Page 0)	R/W Word	1.15 x Vout by pin-strap	
0x24	VOUT_MAX (Page 1)	R/W Word	1.15 x Vout by pin-strap	
0x25	VOUT_MARGIN_HIGH (Page 0)	R/W Word	1.05 x Vout by pin-strap	
0x25	VOUT_MARGIN_HIGH (Page 1)	R/W Word	1.05 x Vout by pin-strap	
0x26	VOUT_MARGIN_LOW (Page 0)	R/W Word	0.95 x Vout by pin-strap	
0x26	VOUT_MARGIN_LOW (Page 1)	R/W Word	0.95 x Vout by pin-strap	
0x27	VOUT_TRANSITION_RATE (Page 0)	R/W Word	0xBA00	1.0 V/ms
0x27	VOUT_TRANSITION_RATE (Page 1)	R/W Word	0xBA00	1.0 V/ms
0x28	VOUT_DROOP (Page 0)	R/W Word		
0x28	VOUT_DROOP (Page 1)	R/W Word		
0x29	VOUT_SCALE_LOOP (Page 0)	R/W Word	Unit Specific	
0x29	VOUT_SCALE_LOOP (Page 1)	R/W Word	Unit Specific	
0x2B	VOUT_MIN (Page 0)	R/W Word	x Vout by pin-strap	
0x2B	VOUT_MIN (Page 1)	R/W Word	x Vout by pin-strap	
0x33	FREQUENCY_SWITCH (Page 0)	R/W Word		
0x33	FREQUENCY_SWITCH (Page 1)	R/W Word		
0x34	POWER_MODE (Page 0)	R/W Byte		
0x34	POWER_MODE (Page 1)	R/W Byte		
0x35	VIN_ON	R/W Word	0xF018	6.0 V
0x36	VIN_OFF	R/W Word	0xF016	5.5 V
0x38	IOUT_CAL_GAIN (Page 0)	R/W Word	Unit Specific	
0x38	IOUT_CAL_GAIN (Page 1)	R/W Word	Unit Specific	
0x39	IOUT_CAL_OFFSET (Page 0)	R/W Word	Unit Specific	
0x39	IOUT_CAL_OFFSET (Page 1)	R/W Word	Unit Specific	
0x40	VOUT_OV_FAULT_LIMIT (Page 0)	R/W Word		
0x40	VOUT_OV_FAULT_LIMIT (Page 1)	R/W Word		
0x41	VOUT_OV_FAULT_RESPONSE (Page 0)	R/W Byte	0x80	

Code	Name	Data Format	Factory Default Value Standard Configuration BMR_474_2001/001 R1	
0x41	VOUT_OV_FAULT_RESPONSE (Page 1)	R/W Byte	0x80	
0x42	VOUT_OV_WARN_LIMIT (Page 0)	R/W Word		
0x42	VOUT_OV_WARN_LIMIT (Page 1)	R/W Word		
0x43	VOUT_UV_WARN_LIMIT (Page 0)	R/W Word		
0x43	VOUT_UV_WARN_LIMIT (Page 1)	R/W Word		
0x44	VOUT_UV_FAULT_LIMIT (Page 0)	R/W Word		
0x44	VOUT_UV_FAULT_LIMIT (Page 1)	R/W Word		
0x45	VOUT_UV_FAULT_RESPONSE (Page 0)	R/W Byte	0x80	
0x45	VOUT_UV_FAULT_RESPONSE (Page 1)	R/W Byte	0x80	
0x46	IOUT_OC_FAULT_LIMIT	R/W Word	0x0035	53 A
0x47	IOUT_OC_FAULT_RESPONSE (Page 0)	R/W Byte	0xC0	
0x47	IOUT_OC_FAULT_RESPONSE (Page 1)	R/W Byte	0xC0	
0x4A	IOUT_OC_WARN_LIMIT (Page 0)	R/W Word	0x0078	120.0 A
0x4A	IOUT_OC_WARN_LIMIT (Page 1)	R/W Word	0x0078	120.0 A
0x4B	IOUT_UC_FAULT_LIMIT (Page 0)	R/W Word	0x07A6	1958 A
0x4B	IOUT_UC_FAULT_LIMIT (Page 1)	R/W Word	0x07A6	1958 A
0x4C	IOUT_UC_FAULT_RESPONSE (Page 0)	R/W Byte	0xC0	
0x4C	IOUT_UC_FAULT_RESPONSE (Page 1)	R/W Byte	0xC0	
0x4F	OT_FAULT_LIMIT (Page 0)	R/W Word	0x0078	120.0 °C
0x4F	OT_FAULT_LIMIT (Page 1)	R/W Word	0x0078	120.0 °C
0x50	OT_FAULT_RESPONSE (Page 0)	R/W Byte	0x80	
0x50	OT_FAULT_RESPONSE (Page 1)	R/W Byte	0x80	
0x51	OT_WARN_LIMIT (Page 0)	R/W Word	0x006E	110.0 °C
0x51	OT_WARN_LIMIT (Page 1)	R/W Word	0x006E	110.0 °C
0x55	VIN_OV_FAULT_LIMIT	R/W Word	0x0010	16.0 V
0x56	VIN_OV_FAULT_RESPONSE	R/W Byte	0x80	
0x57	VIN_OV_WARN_LIMIT	R/W Word	0x000F	15.0 V
0x58	VIN_UV_WARN_LIMIT	R/W Word	0xF016	5.5 V
0x59	VIN_UV_FAULT_LIMIT	R/W Word	0xF014	5.0 V
0x5A	VIN_UV_FAULT_RESPONSE	R/W Byte	0xB8	
0x60	TON_DELAY (Page 0)	R/W Word	0xF800	0.0 ms
0x60	TON_DELAY (Page 1)	R/W Word	0xF800	0.0 ms
0x61	TON_RISE (Page 0)	R/W Word	0xF800	0.0 ms
0x61	TON_RISE (Page 1)	R/W Word	0xF800	0.0 ms
0x62	TON_MAX_FAULT_LIMIT (Page 0)	R/W Word	0xF008	2.0 ms
0x62	TON_MAX_FAULT_LIMIT (Page 1)	R/W Word	0xF008	2.0 ms
0x63	TON_MAX_FAULT_RESPONSE (Page 0)	R/W Byte	0x80	
0x63	TON_MAX_FAULT_RESPONSE (Page 1)	R/W Byte	0x80	
0x64	TOFF_DELAY (Page 0)	R/W Word	0x8000	0.0 ms
0x64	TOFF_DELAY (Page 1)	R/W Word	0x8000	0.0 ms
0x65	TOFF_FALL (Page 0)	R/W Word		
0x65	TOFF_FALL (Page 1)	R/W Word		
0x78	STATUS_BYTE (Page 0)	Read Byte		
0x78	STATUS_BYTE (Page 1)	Read Byte		
0x79	STATUS_WORD (Page 0)	Read Word		
0x79	STATUS_WORD (Page 1)	Read Word		
0x7A	STATUS_VOUT (Page 0)	Read Byte		
0x7A	STATUS_VOUT (Page 1)	Read Byte		
0x7B	STATUS_IOUT (Page 0)	Read Byte		
0x7B	STATUS_IOUT (Page 1)	Read Byte		
0x7C	STATUS_INPUT	Read Byte		
0x7D	STATUS_TEMPERATURE (Page 0)	Read Byte		
0x7D	STATUS_TEMPERATURE (Page 1)	Read Byte		
0x7E	STATUS_CML	Read Byte		
0x7F	STATUS_OTHER	Read Byte		
0x80	STATUS_MFR_SPECIFIC (Page 0)	Read Byte		
0x80	STATUS_MFR_SPECIFIC (Page 1)	Read Byte		
0x88	READ_VIN	Read Word		
0x89	READ_IIN	Read Word		

Code	Name	Data Format	Factory Default Value Standard Configuration BMR_474_2001/001 R1	
0x8B	READ_VOUT (Page 0)	Read Word		
0x8B	READ_VOUT (Page 1)	Read Word		
0x8C	READ_IOUT (Page 0)	Read Word		
0x8C	READ_IOUT (Page 1)	Read Word		
0x8D	READ_TEMPERATURE_1 (Page 0)	Read Word		
0x8D	READ_TEMPERATURE_1 (Page 1)	Read Word		
0x96	READ_POUT (Page 0)	Read Word		
0x96	READ_POUT (Page 1)	Read Word		
0x97	READ_PIN	Read Word		
0x98	PMBUS_REVISION	Read Byte		
0x99	MFR_ID	R/W Block22	Unit Specific	
0x9A	MFR_MODEL	R/W Block14	Unit Specific	
0x9B	MFR_REVISION	R/W Block3	Unit Specific	
0x9D	MFR_DATE	Read Block4	Unit Specific	
0xAD	IC_DEVICE_ID	Read Block6	0x544953676000	
0xAE	IC_DEVICE_REV	Read Block2		
0xB1	USER_DATA_01 (page 0)	R/W Block8		
0xB1	USER_DATA_01 (Page 1)	R/W Block8		
0xB2	USER_DATA_02 (Page 0)	R/W Block5		
0xB2	USER_DATA_02 (Page 1)	R/W Block5		
0xB4	USER_DATA_04 (page 0)	R/W Block6	0x036008080000	
0xB4	USER_DATA_04 (Page 1)	R/W Block6	0x036008080000	
0xBA	USER_DATA_10 (Page 0)	R/W Block1		
0xBA	USER_DATA_10 (Page 1)	R/W Block1		
0xBB	USER_DATA_11	R/W Block10		
0xBD	USER_DATA_13	R/W Block15		
0xCD	MULTIFUNCTION_PIN_CONFIG_1	R/W Block32		
0xCE	MULTIFUNCTION_PIN_CONFIG_2	R/W Block31		
0xCF	SMBALERT_MASK_EXTENDED	R/W Block7		
0xD1	READ_VOUT_MIN_MAX (Page 0)	Read Block4		
0xD1	READ_VOUT_MIN_MAX (Page 1)	Read Block4		
0xD2	READ_IOUT_MIN_MAX (Page 0)	Read Block4		
0xD2	READ_IOUT_MIN_MAX (Page 1)	Read Block4		
0xD3	READ_TEMPERATURE_MIN_MAX (Page 0)	Read Block4		
0xD3	READ_TEMPERATURE_MIN_MAX (Page 1)	Read Block4		
0xD4	READ_MFR_VOUT (Page 0)	Read Word		
0xD4	READ_MFR_VOUT (Page 1)	Read Word		
0xD5	READ_VIN_MIN_MAX	Read Block4		
0xD6	READ_IIN_MIN_MAX	Read Block4		
0xD7	READ_PIN_MIN_MAX	Read Block4		
0xD8	READ_POUT_MIN_MAX (Page 0)	Read Block4		
0xD8	READ_POUT_MIN_MAX (Page 1)	Read Block4		
0xDC	STATUS_PHASES (Page 0)	Read Word		
0xDC	STATUS_PHASES (Page 1)	Read Word		
0xDD	STATUS_EXTENDED	Read Block7		
0xE4	SYNC_CONFIG	R/W Block6		
0xEE	PIN_DETECT_OVERRIDE	R/W Byte		
0xEF	SLAVE_ADDRESS	R/W Byte		
0xFB	MFR_SPECIFIC_WRITE_PROTECT	R/W Word		
0xFE02	MFR_PMBUSCFG_TIMESTAMP	Read Block8	Unit Specific	

PMBus Command Details

PAGE (0x00)
Description:

Bit	Description	Format
7:0	Page 1 is not used in 2-phase mode.	Integer Unsigned

OPERATION (0x01)
Status Registers: Page 0 (0), Page 1 (1)
Description: Controls enable and margin operations.

Bit	Function	Description	Value	Function	Description
7:6	Enable	Make the device enable or disable if PMBus Enable has been activated in ON_OFF_CONFIG.	00	Immediate Off	Disable immediately without controlled ramp-down or sequencing.
			01	Soft Off	Disable by controlled ramp-down timings or sequencing.
			10	Enable	Enable device to the set voltage or margin state, using ramp up timings / sequencing.
5:4	Margin	Select between margin high/low states or nominal output.	00	Nominal	Operate at nominal output voltage.
			01	Margin Low	Operate at voltage set by command VOUT_MARGIN_LOW.
			10	Margin High	Operate at voltage set by command VOUT_MARGIN_HIGH.
3:2	Margin fault action		01	Ignore fault	Output voltage target is VOUT_MARGIN_HIGH/VOUT_MARGIN_LOW, OV/UV faults are masked.
			10	Act on fault	Output voltage target is VOUT_MARGIN_HIGH/VOUT_MARGIN_LOW, OV/UV faults trigger per their respective fault response settings.

ON_OFF_CONFIG (0x02)
Status Registers: Page 0 (0), Page 1 (1)
Description: Configures how the device is controlled by the CTRL pin and the PMBus.

Bit	Function	Description	Value	Function	Description
4	Powerup Operation		0	Ignore CTRL pin or PMBus	Unit starts power conversion any time the input power is present regardless of the state of the CTRL pin.
			1	CTRL pin or PMBus	Device does not power up until commanded by the CTRL pin or OPERATION command.
3	PMBus Enable Mode	Controls how the device responds to the PMBus command OPERATION.	0	Ignore PMBus command	Ignores the on/off portion of the OPERATION command.
			1	Use PMBus command	Device requires on by OPERATION command to enable the output voltage.
2	Enable Pin Mode	Controls how the device responds to the CTRL pin.	0	Ignore CTRL pin	Device ignores the CTRL pin.
			1	Use CTRL pin	Device requires the CTRL pin to be asserted to enable the output voltage.

Bit	Function	Description	Value	Function	Description
1	Enable Pin Polarity	Polarity of the CTRL pin.	0	Active Low	CTRL pin will cause device to enable when driven low.
			1	Active High	CTRL pin will cause device to enable when driven high.
0	Disable Action	CTRL pin action when commanding the output to turn off.	0	Soft Off	Use the configured turn off delay and fall time.
			1	Immediate Off	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

CLEAR_FAULTS (0x03)
Description: Clears all fault status bits

PHASE (0x04)
Status Registers: Page 0 (0), Page 1 (1)
Description: Used to configure, control, and monitor multiple phases on one page. Need to be established before any phase-dependent command can be successfully excuted.

Bit	Description	Format
7:0	Only phase 1 and phase 2 are applied in 2-phase mode. Listed values for phase selection: 0x00 PHASE, 0X01 PHASE, 2 0XFF TOTAL PHASE.	Integer Unsigned

WRITE_PROTECT (0x10)
Description: The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation.

Bit	Description	Value	Function	Description
7:0		0x80	Disable all writes	Disable all writes except to the WRITE_PROTECT command.
		0x40	Enable operation	Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands.
		0x20	Enable control and Vout commands	Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands.
		0x00	Enable all commands	Enable writes to all commands.

STORE_DEFAULT_ALL (0x11)
Description: Commands the device to store its configuration into the Default Store.

RESTORE_DEFAULT_ALL (0x12)
Description: Commands the device to restore its configuration from the Default Store.

STORE_USER_ALL (0x15)
Description: Commands the device to copy the entire contents of the operating memory to the matching locations in the non-volatile user store memory.

RESTORE_USER_ALL (0x16)
Description: Commands the device to copy the entire cotents of the non-volatile User Store Memory to the matching lications in the operating memory.

SMBALERT_MASK (0x1B)
Status Registers: STATUS_VOUT (0x7A), STATUS_IOUT (0x7B), STATUS_INPUT (0x7C), STATUS_TEMPERATURE (0x7D), STATUS_CML (0x7E), STATUS_MFR_SPECIFIC (0x80)
Description: The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Mask Bit 7		0	Pull SALERT	
			1	Ignore	
6	Mask Bit 6		0	Pull SALERT	
			1	Ignore	
5	Mask Bit 5		0	Pull SALERT	
			1	Ignore	
4	Mask Bit 4		0	Pull SALERT	
			1	Ignore	
3	Mask Bit 3		0	Pull SALERT	
			1	Ignore	
2	Mask Bit 2		0	Pull SALERT	
			1	Ignore	
1	Mask Bit 1		0	Pull SALERT	
			1	Ignore	
0	Mask Bit 0		0	Pull SALERT	
			1	Ignore	

VOUT_MODE (0x20)
Status Registers: Page 0 (0), Page 1 (1)
Description: Controls how future VOUT-related commands parameters will be interpreted.

Bit	Function	Description	Format
4:0	Parameter	Five bit two's complement EXPONENT for the MANTISSA delivered as the data bytes for VOUT_COMMAND in VOUT_LINEAR Mode.	Integer Signed

Bit	Function	Description	Value	Function	Description
7:5	Mode	Selection of mode for representation of output voltage parameters.	000	Linear	Linear Mode Format.
			001	VID	VID Mode.

VOUT_COMMAND (0x21)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the nominal value of the output voltage from 0.6V to 3.3V.

Bit	Description	Format	Unit
15:0	Sets the nominal value of the output voltage.	Vout Mode Unsigned	V

VOUT_TRIM (0x22)
Status Registers: Page 0 (0), Page 1 (1)
Description: Configures a fixed offset to be applied to the output voltage when enabled.

Bit	Description	Format	Unit
15:0	Sets VOUT trim value. The range is limited to +/-150 mV.	Vout Mode Signed	V

VOUT_MAX (0x24)
Status Registers: Page 0 (0), Page 1 (1)
Description: Configures the maximum allowed output voltage.

Bit	Description	Format	Unit
15:0	If the device is commanded to a Vout value higher than this level, the output voltage will be clamped to this level. The max VOUT_MAX setting is 115% of the VSET pin-strap setting.	Vout Mode Unsigned	V

VOUT_MARGIN_HIGH (0x25)
Status Registers: Page 0 (0), Page 1 (1)
Description: Configures the target for margin-up commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin high.	Vout Mode Unsigned	V

VOUT_MARGIN_LOW (0x26)
Status Registers: Page 0 (0), Page 1 (1)
Description: Configures the target for margin-down commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin low.	Vout Mode Unsigned	V

VOUT_TRANSITION_RATE (0x27)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the transition rate when changing output voltage.

Bit	Description	Format	Unit
15:0	Configures the transition time for margining and on-the-fly VOUT_COMMAND changes.	Linear	V/ms

VOUT_DROOP (0x28)
Status Registers: Page 0 (0), Page 1 (1)
Description: Configures a droop of output voltage.

Bit	Description	Format	Unit
15:0	Sets the effective load line (V/I slope) for the rail in which the device is used. When the device is part of a current sharing rail, this value must be non-zero and the same for all devices in the rail.	Linear	mV/A

VOUT_SCALE_LOOP (0x29)
Status Registers: Page 0 (0), Page 1 (1)
Description: Allows PMBus devices to map between the commanded voltage, and the voltage at the control circuit.

Bit	Description	Format
15:0	Choose scaling factor.Values less than 0.5 and greater than 1.0 are unaccepted.	Linear

VOUT_MIN (0x2B)
Status Registers: Page 0 (0), Page 1 (1)
Description: Configures the minimum allowed output voltage.

Bit	Description	Format	Unit
15:0	If the device is commanded to a Vout value lower than this level, the output voltage will be clamped to this level.	Vout Mode Unsigned	V

FREQUENCY_SWITCH (0x33)
Status Registers: Page 0 (0), Page 1 (1)
Description: Controls the switching frequency.

Bit	Description	Format	Unit
15:0	Sets the switching frequency in 50 kHz steps. The specified range is 300 - 2000 kHz.	Linear	kHz

POWER_MODE (0x34)
Status Registers: Page 0 (0), Page 1 (1)
Description: Changes the operating power state of the device.

Bit	Description	Value	Function	Description
2:0	Choose operating mode of the device.	000	Maximum Efficiency	Enable phase shedding and allow DCM for all phases.
		011	Maximum Power	Disable phase shedding and all phases run in FCCM mode.
		100	Manufacturer Defined	Enable phase shedding and allow DCM for only the 1 phase operation, otherwise CCM.

VIN_ON (0x35)
Description: Input voltage must be above this level before the output can be enabled.

Bit	Description	Format	Unit
15:0	0.25V per step	Linear	V

VIN_OFF (0x36)
Description: Input voltage must be lower this level before the output can be disabled.

Bit	Description	Format	Unit
15:0	0.25V per step	Linear	V

IOUT_CAL_GAIN (0x38)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the current sense resistance.

Bit	Description	Format	Unit
15:0	Sets the effective impedance for current sensing at +25°C.	Linear	mΩ

IOUT_CAL_OFFSET (0x39)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the current-sense offset.

Bit	Description	Format	Unit
15:0	Sets an offset to IOUT readings. Use to compensate for delayed measurements of current ramp.	Linear	A

VOUT_OV_FAULT_LIMIT (0x40)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the VOUT overvoltage fault threshold. When VBOOT=0V, the device automatically selects the widest threshold (+448mV) regardless if the value stored in NVM.

Bit	Description	Format	Unit
15:0	Sets the VOUT overvoltage fault threshold, which is VOUT_COMMAND + Vout OV Fault Limit	Vout Mode Unsigned	mV

VOUT_OV_FAULT_RESPONSE (0x41)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the VOUT OV fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch Off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.

Bit	Function	Description	Value	Function	Description
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.

VOUT_OV_WARN_LIMIT (0x42)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the VOUT overvoltage warning threshold. When VBOOT=0V, the device automatically selects the widest threshold (+448mV) regardless if the value stored in NVM.

Bit	Description	Format	Unit
15:0	Sets the VOUT overvoltage warning threshold, which is VOUT_COMMAND + Vout OV Warn Limit	Vout Mode Unsigned	mV

VOUT_UV_WARN_LIMIT (0x43)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the VOUT undervoltage warning threshold.When VBOOT=0V, the device automatically selects the widest threshold (-448mV) regardless if the value stored in NVM.

Bit	Description	Format	Unit
15:0	Sets the VOUT undervoltage warning threshold, which is VOUT_COMMAND - Vout UV Warn Limit.	Vout Mode Unsigned	mV

VOUT_UV_FAULT_LIMIT (0x44)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the VOUT undervoltage fault threshold.When VBOOT=0V, the device automatically selects the widest threshold (-448mV) regardless if the value stored in NVM.

Bit	Description	Format	Unit
15:0	Sets the VOUT undervoltage fault threshold, which is VOUT_COMMAND - Vout UV Fault Limit.	Vout Mode Unsigned	mV

VOUT_UV_FAULT_RESPONSE (0x45)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the VOUT UV fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	01	Shutdown After Delay	Disable the output with delay time according to the setting in bits [2:0].
			10	Shutdown Immediately	Shutdown and do not restart. The output remains disabled until the fault is cleared.
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Latch off	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Hiccup	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Delay Time	Delay will be ignored for when VO UV RESP bits instruct the device to shutdown immediately.	000	4	
			001	8	
			010	12	

Bit	Function	Description	Value	Function	Description
			011	16	

IOUT_OC_FAULT_LIMIT (0x46)
Description: Sets the output over-current peak limit for per phase/page.

Bit	Description	Format	Unit
15:0	Sets the IOUT overcurrent peak fault threshold for each phase with PHASE command set to 00h. Sets the IOUT overcurrent peak fault threshold for each page with PHASE command set to FFh. Adjustable range from 0-1023A. Linear format with LSB=1A. Note that only when per-page over_current protection is triggered, the device responds according to IOUT_OC_FAULT_LIMIT_RESPONSE.	Integer Unsigned	A

IOUT_OC_FAULT_RESPONSE (0x47)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the output total-PAGE over-current fault response.

Bit	Description	Value	Function	Description
7:3	Describes the device interruption operation. For all modes set by bits [7:3], the device pulls SALERT low and sets the related fault bit in the status registers.	11000	Latch Off Immediately	Shutdown and do not restart.
		11111	Hiccup Immediately	Shutdown and attempt to restart after 1 hittcup time and repeat, until either the unit is commanded OFF, or a successful start-up retrial.

IOUT_OC_WARN_LIMIT (0x4A)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the output over-current warn limit for per page.

Bit	Description	Format	Unit
15:0	Sets the IOUT overcurrent peak warning threshold for each page. Adjustable range from 0-1023A. Linear format with LSB=1A.	Linear	A

IOUT_UC_FAULT_LIMIT (0x4B)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the output sink-current peak limit for per page.

Bit	Description	Format	Unit
10:0		Integer Signed	A

IOUT_UC_FAULT_RESPONSE (0x4C)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the output total-PAGE under-current fault response.

Bit	Function	Description	Value	Function	Description
7:3	Response	Describes the device interruption operation. For all modes set by bits [7:3], the device pulls SALERT low and sets the related fault bit in the status registers.	10000	Latch Off After Delay	Continue operating after for the CYCLE SETTING number of cycles. If the fault persists，shutdown and do not restart.
0	Cycling Setting	Respond after set cycles.	0	8 Cycles	Respond after 8 consecutive cycles with negative current exceeding IOUT_UC_FAULT_LIMIT.
			1	16 Cycles	Respond after 16 consecutive cycles with negative current exceeding IOUT_UC_FAULT_LIMIT.

OT_FAULT_LIMIT (0x4F)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the over-temperature fault limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature fault threshold.	Linear	°C

OT_FAULT_RESPONSE (0x50)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the over-temperature fault response.

Bit	Description	Value	Function	Description
7:3	Describes the device interruption operation. For all modes set by bits [7:3], the device pulls SALERT low and sets the related fault bit in the status registers.	10000	Latch Off Immediately	Shutdown and do not restart.
		10111	Hiccup Immediately	Shutdown and attempt to restart after 1 hittcup time and repeat, until either the unit is commanded OFF, or a successful start-up retrial.
		11111	Hysteresis Only	Power conversion is disabled when the sensed temperature exceeds the over temperature fault limit. The unit attempts to restart power conversion once the sensed temperature falls below the overtemperature fault limit.

OT_WARN_LIMIT (0x51)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the over-temperature warn limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature warn threshold.	Linear	°C

VIN_OV_FAULT_LIMIT (0x55)
Description: Sets the input over-voltage fault limit.

Bit	Description	Format	Unit
15:0	Sets the VIN overvoltage fault threshold.	Linear	V

VIN_OV_FAULT_RESPONSE (0x56)
Description: Sets the input over-voltage fault response.

Bit	Description	Value	Function	Description
7:3	Describes the device interruption operation. For all modes set by bits [7:3], the device pulls SALERT low and sets the related fault bit in the status registers.	10000	Latch Off Immediately	Shutdown and do not restart.
		10111	Hiccup Immediately	Shutdown and attempt to restart after 1 hittcup time and repeat, until either the unit is commanded OFF, or a successful start-up retrial.

VIN_OV_WARN_LIMIT (0x57)
Description: Sets the input over-voltage warning limit.

Bit	Description	Format	Unit
15:0	Sets the VIN overvoltage warning threshold.	Linear	V

VIN_UV_WARN_LIMIT (0x58)
Description: Sets the input under-voltage warning limit.

Bit	Description	Format	Unit
15:0	Sets the VIN undervoltage warning threshold.	Linear	V

VIN_UV_FAULT_LIMIT (0x59)
Description: Sets the input under-voltage fault limit.

Bit	Description	Format	Unit
15:0	Sets the VIN undervoltage fault threshold.	Linear	V

VIN_UV_FAULT_RESPONSE (0x5A)
Description: Sets the input under-voltage fault response.

Bit	Description	Value	Function	Description
7:3	Describes the device interruption operation. For all modes set by bits [7:3], the device pulls SALERT low and sets the related fault bit in the status registers.	10000	Latch Off Immediately	Shutdown and do not restart.
		10111	Hiccup Immediately	Shutdown and attempt to restart after 1 hittcup time and repeat, until either the unit is commanded OFF, or a successful start-up retrial.

TON_DELAY (0x60)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the turn-on delay time

Bit	Description	Format	Unit
15:0	Sets the time, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Note that device requires approximately 500 µs from the moment it is commanded to enable power conversion, to the beginning of switching activity. Delay added by TON_DELAY is in addition to this.	Linear	ms

TON_RISE (0x61)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the turn-on ramp-up time.

Bit	Description	Format	Unit
15:0	Sets the rise time of VOUT after ENABLE and On Delay. The time can range from 0 ms to 31.75 ms.	Linear	ms

TON_MAX_FAULT_LIMIT (0x62)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets an upper limit on how long the unit can attempt to power up the output without reaching the target voltage.

Bit	Description	Format	Unit
15:0	Sets the upper limit time. The time can range from 0 ms to 31.75 ms.	Linear	ms

TON_MAX_FAULT_RESPONSE (0x63)
Status Registers: Page 0 (0), Page 1 (1)
Description: Instructs the device on what action to take in response to TON_MAX fault.

Bit	Description	Value	Function	Description
7:3	Describes the device interruption operation. For all modes set by bits [7:3], the device pulls SALERT low and sets the related fault bit in the status registers.	10000	Latch Off Immediately	Shutdown and do not restart.
		10111	Hiccup Immediately	Shutdown and attempt to restart after 1 hittcup time and repeat, until either the unit is commanded OFF, or a successful start-up retrial.

TOFF_DELAY (0x64)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the turn-off delay.

Bit	Description	Format	Unit
15:0	Sets the delay time from DISABLE to start of the fall of the output voltage. Normally the time can range from 0.5 ms up to 127.5 ms.	Linear	ms

TOFF_FALL (0x65)
Status Registers: Page 0 (0), Page 1 (1)
Description: Sets the turn-off ramp-down time.

Bit	Description	Format	Unit
15:0	Sets the fall time for VOUT after DISABLE and Off Delay. The time can range from 0 ms to 31.75 ms.	Linear	ms

STATUS_BYTE (0x78)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns a brief fault/warning status byte.

Bit	Function	Description	Value	Description
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No fault
			1	Fault
6	Off	This bit is asserted if the unit is not providing power to the output due to not being enabled, i.e. not set when output shut down due to fault.	0	No fault
			1	Fault
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No fault
			1	Fault
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No fault
			1	Fault
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No fault
			1	Fault
2	Temperature	A temperature fault or warning has occurred.	0	No fault
			1	Fault
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault
			1	Fault

STATUS_WORD (0x79)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns an extended fault/warning status byte.

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has occurred.	0	No fault
			1	Fault
14	Iout	An output current fault or warning has occurred.	0	No Fault.
			1	Fault.
13	Input	An input voltage, input current, or input power fault or warning has occurred.	0	No Fault.
			1	Fault.
12	Mfr	A manufacturer specific fault or warning has occurred.	0	No Fault.
			1	Fault.
11	Power-Good	The Power-Good signal, if present, is negated.	0	No Fault.
			1	Fault.
9	Other	An other fault has occurred.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No Fault.
			1	Fault.
6	Off	This bit is asserted if the unit is not providing power to the output due to not being enabled, i.e. not set when output shut down due to fault.	0	No Fault.
			1	Fault.
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No Fault.
			1	Fault.
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No Fault.

Bit	Function	Description	Value	Description
			1	Fault.
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No Fault.
			1	Fault.
2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault.
			1	Fault.

STATUS_VOUT (0x7A)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns Vout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vout OV Fault	Latched flag of Vout over-voltage fault has occurred .	0	No Fault.
			1	Fault.
6	Vout OV Warn	Latched flag of Vout over-voltage warning has occurred .	0	No Fault.
			1	Fault.
5	Vout UV Warn	Latched flag of Vout under-voltage warning has occurred .	0	No Fault.
			1	Fault.
4	Vout UV Fault	Latched flag of Vout under-voltage fault has occurred .	0	No Fault.
			1	Fault.
3	Vout Min/Max Fault	Latched flag of Vout min/max fault or warning has occurred .	0	No Fault.
			1	Fault.
2	Ton Max Fault	Latched flag of Ton max fault or warning has occurred .	0	No Fault.
			1	Fault.

STATUS_IOUT (0x7B)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns Iout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Iout OC Fault	Latched flag of Iout over-current fault has occurred.	0	No Fault.
			1	Fault.
5	Iout OC Warn	Latched flag of Iout over-current warning has occurred.	0	No Fault.
			1	Fault.
4	Iout UC Fault	Latched flag of Iout under-current fault has occurred.	0	No Fault.
			1	Fault.
3	Current Share Fault	Latched flag of current share fault has occurred.	0	No Fault.
			1	Fault.

STATUS_INPUT (0x7C)
Description: Returns VIN/IIN-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vin Overvoltage Fault	Latched flag of input over-voltage fault has occurred.	0	No Fault.
			1	Fault.
6	Vin OV Warn	Latched flag of input over-voltage warning has occurred.	0	No Fault.
			1	Fault.
5	Vin UV Warn	Latched flag of input under-voltage warning has occurred.	0	No Fault.
			1	Fault.
4	Vin UV Fault	Latched flag of input under-voltage fault has occurred.	0	No Fault.
			1	Fault.
3	Low Vin Fault	Latched flag of shutdown unit due to insufficient VIN .	0	No Fault.
			1	Fault.
2	Iin Oc Fault	Latched flag of input over-current fault has occurred.	0	No Fault.
			1	Fault.
1	Iin Oc Warn	Latched flag of input over-current warning has occurred.	0	No Fault.
			1	Fault.
0	Pin Op Warn	Latched flag of input over-power warning has occurred.	0	No Fault.
			1	Fault.

STATUS_TEMPERATURE (0x7D)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the temperature-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Overtemperature Fault	Latched flag of over-temperature fault has occurred.	0	No Fault.
			1	Fault.
6	Overtemperature Warn	Latched flag of over-temperature warn has occurred.	0	No Fault.
			1	Fault.

STATUS_CML (0x7E)
Description: Returns Communication/Logic/Memory-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Invalid Or Unsupported Command Received	Invalid Or Unsupported Command Received.	0	No Invalid Command Received.
			1	Invalid Command Received.
6	Invalid Or Unsupported Data Received	Invalid Or Unsupported Data Received.	0	No Invalid Data Received.
			1	Invalid Data Received.
5	Packet Error Check Failed	Packet Error Check (PEC) Failed.	0	No Failure.
			1	Failure.
4	Memory Error	A memory error was detected.	0	No Fault.
			1	Fault.
1	Other Communication Fault	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.	0	No Fault.
			1	Fault.

STATUS_OTHER (0x7F)
Description: Returns one data byte with information not specified in the other STATUS_BYTE.

Bit	Description	Value	Description
0	The device was the first to assert SMBALERT.	1	First to assert SMBALERT.
		0	The device was not the first to assert SMBALERT. This could mean either that the SMBALERT signal is not asserted (or has since been cleared), or that it is asserted, but this device was not the first on the bus to assert it.

STATUS_MFR_SPECIFIC (0x80)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns manufacturer specific status information.

Bit	Function	Description	Value	Description
7	Power On Self Check	Power on self check failed and device will permanently latch off.	0	Condition occurred.
			1	Condition did not occur.
6	Ext	More information is available in the STATUS_EXTENDED block command.	0	Cndition occurred.
			1	Condition did not occur.
5	VR Settle	The output voltage has settled to its new target.	0	Condition occurred.
			1	Condition did not occur.
4	Phase Error	Phase error.	0	No Fault.
			1	Fault.
3	Reset	A reset pin event has occurred.	0	No Fault.
			1	Fault.

Bit	Function	Description	Value	Description
0	Power Stage fault	Power Stage fault has occurred for the currently selected PAGE.	0	No Fault.
			1	Fault.

READ_VIN (0x88)
Description: Returns the measured input voltage.

Bit	Description	Format	Unit
15:0	Returns the input voltage reading.	Linear	V

READ_IIN (0x89)
Description: Returns the measured input current.

Bit	Description	Format	Unit
15:0	Returns the input current reading.	Linear	V

READ_VOUT (0x8B)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the measured output voltage.

Bit	Description	Format	Unit
15:0	Returns the output voltage reading.	Vout Mode Unsigned	V

READ_IOUT (0x8C)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the measured output current.

Bit	Description	Format	Unit
15:0	Returns the output current reading.	Linear	A

READ_TEMPERATURE_1 (0x8D)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the maximum power stage temperature.

Bit	Description	Format	Unit
15:0	When PAGE=00h or FFh, the command returns the maximum power stage temperature of channel A.	Linear	°C

READ_POUT (0x96)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the calculated output power.

Bit	Description	Format	Unit
15:0		Linear	W

READ_PIN (0x97)
Description: Returns the calculated input power.

Bit	Description	Format	Unit
15:0		Linear	W

PMBUS_REVISION (0x98)
Description: Returns the PMBus revision number for this device.

Bit	Function	Description	Value	Function	Description
7:4	Part I Revision	Part I Revision.	0011	1.3	Part I Revision 1.3.
3:0	Part II Revision	Part II Revision.	0011	1.3	Part II Revision 1.3.

MFR_ID (0x99)
Description: Sets the manufacturer ID String.

Bit	Description	Format
23:0	Maximum of 3 bytes.	ASCII

MFR_MODEL (0x9A)
Description: Sets the manufacturer model string.

Bit	Description	Format
23:0	Maximum of 3 bytes.	ASCII

MFR_REVISION (0x9B)
Description: Sets the manufacturer revision string.

Bit	Description	Format
23:0	Maximum of 3 bytes.	ASCII

MFR_DATE (0x9D)
Description: Sets the manufacturing data.

Bit	Description	Format
23:0		ASCII

IC_DEVICE_ID (0xAD)
Description: Reports identification information (not used)

Bit	Description	Format
47:0	Reports identification information (not used)	Byte Array

IC_DEVICE_REV (0xAE)
Description: Reports revision information (not used)

Bit	Description	Format
15:0	Reports revision information (not used)	Byte Array

USER_DATA_01 (0xB1)
Status Registers: page 0 (0), Page 1 (1)
Description: Defined as COMPENSATION_CONFIG. Configure the control loop compensation settings.

Bit	Function	Description	Format	Unit
63:48	Vout Droop	Shadow register for VOUT_DROOP.	Linear	mV/A
47:32	Acll	AC load line setting.Range from 0.0156 mOhm to 8 mOhm.	Linear	mOhm

Bit	Function	Description	Value	Function	Description
31:28	Dcm Int TC	Integrator time constant in DCM mode.	0000	1	
			0001	2	
			0010	3	
			0011	4	
			0100	5	
			0101	6	
			0110	7	
			0111	8	
			1000	9	
			1001	10	
			1010	11	
			1011	12	
			1100	13	
			1101	14	

Bit	Function	Description	Value	Function	Description
			1110	15	
			1111	16	
27:24	Dyn Int TC	Dynamic integration time constant.	0000	1	
			0001	2	
			0010	3	
			0011	4	
			0100	5	
			0101	6	
			0110	7	
			0111	8	
			1000	9	
			1001	10	
			1010	11	
			1011	12	
			1100	13	
			1101	14	
			1110	15	
			1111	16	
23:20	Int TC	Integration time constant.	0000	1	
			0001	2	
			0010	3	
			0011	4	
			0100	5	
			0101	6	
			0110	7	
			0111	8	
			1000	9	
			1001	10	
			1010	11	
			1011	12	
			1100	13	
			1101	14	
			1110	15	
			1111	16	
19:17	Ramp	Ramp amplitude.	000	80	
			001	120	
			010	160	
			011	200	
			100	240	
			101	280	
			110	320	
			111	360	
15:14	INT Gain	Integration path gain.	00	0.5	
			01	1.0	
			10	1.5	
			11	2.0	
13:12	AC Gain	AC path gain.	00	0.5	
			01	1.0	
			10	1.5	
			11	2.0	
11:8	Vdint	Dynamic integration voltage setting.	0000	60	
			0001	80	
			0010	100	
			0011	120	
			0100	140	
			0101	160	
			0110	180	
			0111	Disabled	
4	Gint	Scaling factor for Static and Dynamic Integration Time Constant.	0	1.0 x DYN INT TC;1.0 x INT TC	

Bit	Function	Description	Value	Function	Description
			1	6.0 x DYN INT TC;6.0 x INT TC	

USER_DATA_02 (0xB2)
Status Registers: Page 0 (0), Page 1 (1)
Description: Defined as NONLINEAR_CONFIG. Configure the device behavior during severe load transient events which saturate the control loop.

Bit	Function	Description	Format	Unit
31:24	Tblank	Select the leading edge blanking time.LSB=5ns and do not use settings below 20ns nominal.	Integer Unsigned	ns

Bit	Function	Description	Value	Function	Description
39:38	Minton	Select the controller minimum on-time.	00	30	
			01	40	
			10	50	
			11	60	
36:32	USR2	Undershoot reduction level 2 (USR2) threshold.	00000	15	
			00001	17.5	
			00010	20	
			00011	22.5	
			00100	25	
			00101	27.5	
			00110	30	
			00111	32.5	
			01000	35	
			01001	37.5	
			01010	40	
			01011	42.5	
			01100	45	
			01101	47.5	
			01110	50	
			01111	52.5	
			10000	55	
			10001	57.5	
			10010	60	
			10011	62.5	
			10100	65	
			10101	67.5	
			10110	70	
			10111	72.5	
			11000	75	
			11001	77.5	
			11111	Disabled	
23:20	Minoff	Sets controller minimum off time.	00000	30	
			0001	45	
			0010	60	
			0011	75	
			0100	90	
			0101	105	
			0110	120	
			0111	135	
19:16	OSR	Overshoot reduction threshold.	0000	20	
			0001	30	
			0010	40	
			0011	50	
			0100	60	
			0101	70	
			0110	80	
			0111	90	

Bit	Function	Description	Value	Function	Description
			1000	100	
			1001	110	
			1010	120	
			1011	130	
			1100	140	
			1101	150	
			1110	160	
			1111	Disabled	
15:14	OCL INT	Sets loop integration during OCL conditions.	00	Continue	Loop integration continues during OCL conditions.
			10	Open integration all phases	Open integration when all phases enter OCL, resume when any phase exits OCL.
			11	Open integration any phase	Open integration when any phases enter OCL, resume when any phase exits OCL.
12:8	USR1	Undershoot reduction level 1(USR1) threshold.	00000	10	
			00001	12.5	
			00010	15	
			00011	17.5	
			00100	20	
			00101	22.5	
			00110	25	
			00111	27.5	
			01000	30	
			01001	32.5	
			01010	35	
			01011	37.5	
			01100	40	
			01101	42.5	
			01110	45	
			01111	47.5	
			10000	50	
			10001	52.5	
			10010	55	
			10011	57.5	
			10100	60	
			10101	62.5	
			10110	65	
			10111	67.5	
			11000	70	
			11001	72.5	
			11111	Disabled	
7	OSR TRUNC	Pulse truncation is disabled/enabled during OSR.	0	Disabled	
			1	Enabled	
5	OSR BB	Body braking is disabled/enabled.	0	Disabled	
			1	Enabled	
4:2	TBB OSR	Osr body braking time duration.	000	0.4	
			001	0.5	
			010	0.6	
			011	0.9	
			100	1.0	
			101	1.1	
			110	1.9	
			111	2.2	
1:0	USR1 PH	Phases enabled duting USR1.	00	3 phases	
			01	4 phases	
			10	5 phases	
			11	All phases	

USER_DATA_04 (0xB4)
Status Registers: page 0 (0), Page 1 (1)
Description: Defined as DVID_CONFIG. Configure dynamic options to output voltage slewing.

Bit	Function	Description	Value	Function	Description
44:40	Acll Dacwn	DC loadline during downward moving DAC transitions.	00000	0	
			00010	0.5	
			00100	1.0	
			00110	1.5	
			01000	2.0	
			01010	2.5	
			01100	3.0	
			01110	3.5	
			10000	4.0	
			10010	4.5	
			10100	5.0	
			10110	5.5	
			11000	6.0	
			11010	6.5	
			11100	7.0	
			11110	7.5	
36:32	Dcll Dacup	DC loadline during upward moving DAC transitions.	00000	0	
			00010	0.5	
			00100	1.0	
			00110	1.5	
			01000	2.0	
			01010	2.5	
			01100	3.0	
			01110	3.5	
			10000	4.0	
			10010	4.5	
			10100	5.0	
			10110	5.5	
			11000	6.0	
			11010	6.5	
			11100	7.0	
			11110	7.5	
31:30	Dacdwn Dly	DAC down recovery delay in cycles.	00	1 cycle	
			01	2 cycles	
			10	4 cycles	
			11	8 cycles	
27:24	Acll Dacwn	AC loadline during downward moving DAC transitions.	0000	0	
			0001	0.5	
			0010	1.0	
			0011	1.5	
			0100	2.0	
			0101	2.5	
			0110	3.0	
			0111	3.5	
			1000	4.0	
			1001	4.5	
			1010	5.0	
			1011	5.5	
			1100	6.0	
			1101	6.5	
			1110	7.0	
			1111	7.5	
23:22	Dacup Dly	DAC UP recovery delay in PWN1 cycles.	00	1 cycle	
			01	2 cycles	
			10	4 cycles	
			11	8 cycles	
19:16	Acll Dacup	AC loadline during upward moving	0000	0	

Bit	Function	Description	Value	Function	Description
		DAC transitions.	0001	0.5	
			0010	1.0	
			0011	1.5	
			0100	2.0	
			0101	2.5	
			0110	3.0	
			0111	3.5	
			1000	4.0	
			1001	4.5	
			1010	5.0	
			1011	5.5	
			1100	6.0	
			1101	6.5	
			1110	7.0	
			1111	7.5	
14	Dac OV Det		0	0V	DAC ramps to 0V during soft-off or DVID down to zero.
			1	100mV	Tri-state PWMs when DAC reaches 100 mV during soft-off or DVID down to zero. Intended to prevent negative excursion on output voltage.
13	Bump Red	Disable/Enable soft-start bump reduction feature.	0	Disable	Disable soft-start bump reduction feature.
			1	Enable	Enable soft-start bump reduction feature. Enable fast PWM tri-state if output voltage exceeds DAC during soft-start.
11:10	Ofs Dacup	Sets DAC offset during upward moving DAC transitions.	00	0	
			01	10	
			10	20	
			11	30	
9:8	Ofs Dacdwn	Sets DAC offset during downward moving DAC transitions.	00	0	
			01	10	
			10	20	
			11	30	
1:0	Ofs Wake	Sets DAC offset during startup.	00	0	
			01	30	
			10	60	
			11	90	

USER_DATA_10 (0xBA)
Status Registers: Page 0 (0), Page 1 (1)
Description: Defined as ISHARE_CONFIG. Adjusts the ISHARE loop to adjust current balancing.

Bit	Description	Value	Function	Description
3:0	Sets the thermal sharing gain for the current phase.	0000	0.8	
		0001	0.85	
		0010	0.9	
		0011	0.95	
		0100	1.0	
		0101	1.05	
		0110	1.1	
		0111	1.15	
		1000	1.2	

USER_DATA_11 (0xBB)
Description: Defined as MFR_PROTECTION_CONFIG. Configure any protection features not included in the PMBus spec.

Bit	Function	Description	Value	Function	Description
47:46	Ishare	Ishare warning threshold	00	5	

Bit	Function	Description	Value	Function	Description
	Warning		01	10	
			10	20	
44:40	OV fixed threshold ChannelB	Fixed OVP threshold for channel B.	00000	3.7	
			00001	3.6	
			00010	3.5	
			00011	3.4	
			00100	3.3	
			00101	3.2	
			00110	3.1	
			00111	3.0	
			01000	2.9	
			01001	2.8	
			01010	2.7	
			1011	2.6	
			01100	2.5	
			01101	2.4	
			01110	2.3	
			01111	2.2	
			10000	2.1	
			10001	2.0	
			10010	1.9	
			10011	1.8	
			10100	1.7	
			10101	1.6	
			10110	1.5	
			10111	1.4	
			11000	1.3	
			11001	1.2	
			11010	1.1	
			11011	1.0	
			11100	0.9	
			11101	0.8	
			11110	0.7	
			11111	0.6	
33:32	Psflt Resp	Fault response setting for PS fault (TAO HIGH).	00	Continue uninterrupted	
			01	Hiccup Immediately	
			10	Latch off Immediately	
15:14	Hiccup	Selects the hiccup wait time for all hiccup faults in cycles.	00	5	
			01	10	
			10	25	
			11	50	
12:8	Ov fixed threshold ChannelA	Fixed OV threshold for channel A.	00000	3.7	
			00001	3.6	
			00010	3.5	
			00011	3.4	
			00100	3.3	
			00101	3.2	
			00110	3.1	
			00111	3.0	
			01000	2.9	
			01001	2.8	
			01010	2.7	
			1011	2.6	
			01100	2.5	
			01101	2.4	
			01110	2.3	
			01111	2.2	
			10000	2.1	

Bit	Function	Description	Value	Function	Description
			10001	2.0	
			10010	1.9	
			10011	1.8	
			10100	1.7	
			10101	1.6	
			10110	1.5	
			10111	1.4	
			11000	1.3	
			11001	1.2	
			11010	1.1	
			11011	1.0	
			11100	0.9	
			11101	0.8	
			11110	0.7	
			11111	0.6	
1:0	OCL Cycl	Cycle counter for phase OCL warning condition.	00	1	
			01	2	
			10	4	
			11	6	

USER_DATA_13 (0xBD)
Description: Defined as MFR_CALIBRATION_CONFIG. Contains any non-pmBus standard calibration factors which may be applied to the device.

Bit	Function	Description	Format
47:40	Iinofs	Offset calibration for input current measurement. LSB=0.0625A.	Integer Unsigned
39:31	Giinmax	Digital gain adjustment for input current measurement. LSB=0.5.	Integer Unsigned
23:20	Iout TC TH ChannelB	Dual-slope IMON gain calibration temoerature threshold for channel B. LSB=5°C	Integer Unsigned
19:16	Iout TC TH ChannelA	Dual-slope IMON gain calibration temperature threshold for channel A. LSB=5°C.	Integer Unsigned

Bit	Function	Description	Value	Function	Description
26:24	Giinshunt	Analog gain adjustment for input current measurement.	000	20	
			001	30	
			010	40	
			011	50	
			100	60	
			101	70	
			110	80	
			111	100	
15:12	Calculated Iin Efficiency ChannelB	Calculated Iin efficiency assumption for channelB.	0000	89	
			0001	89.5	
			0010	90	
			0011	90.5	
			0100	91	
			0101	91.5	
			0110	92.0	
			0111	92.5	
			1000	93.0	
			1001	93.5	
			1010	94.0	
			1011	94.5	
			1100	95.0	
			1101	95.5	
			1110	96.0	
			1111	96.5	
11:8	Calculated Iin Efficiency ChannelA	Calculated Iin efficiency assumption for channelA.	0000	89	
			0001	89.5	
			0010	90	
			0011	90.5	

Bit	Function	Description	Value	Function	Description
			0100	91	
			0101	91.5	
			0110	92.0	
			0111	92.5	
			1000	93.0	
			1001	93.5	
			1010	94.0	
			1011	94.5	
			1100	95.0	
			1101	95.5	
			1110	96.0	
			1111	96.5	
7:4	Iout Tgain ChannelB	Dual-slope IMON gain calibration value for channel B. #IOUT TGAIN CHA = IOUT_CAL_GAIN x k, k is lisetd below.	0000	0.984	
			0001	0.986	
			0010	0.988	
			0011	0.990	
			0100	0.992	
			0101	0.994	
			0110	0.996	
			0111	0.998	
			1000	1.0	
			1001	1.002	
			1010	1.004	
			1011	1.006	
			1100	1.008	
			1101	1.010	
			1110	1.012	
			1111	1.014	
3:0	Iout Tgain ChannelA	Dual-slope IMON gain calibration value for channel A. #IOUT TGAIN CHA = IOUT_CAL_GAIN x k, k is lisetd below.	0000	0.984	
			0001	0.986	
			0010	0.988	
			0011	0.990	
			0100	0.992	
			0101	0.994	
			0110	0.996	
			0111	0.998	
			1000	1.0	
			1001	1.002	
			1010	1.004	
			1011	1.006	
			1100	1.008	
			1101	1.010	
			1110	1.012	
			1111	1.014	

MULTIFUNCTION_PIN_CONFIG_1 (0xCD)
Description: Configures multi-function pins.

Bit	Function	Description	Value	Function	Description
149:146	PIN43	Configures pin43 as ATSEN, BTSEN or TSEN.	0010	ATSEN	Temperature sense for channel A.
			0100	BTSEN	Temperature sense for channel B.
			0110	TSEN	Temperature sense for channels A and B.
129:120	PIN19	Configures pin19 as BVR_EN, SYNC_IN, SYNC_OUT or RESET#.			

MULTIFUNCTION_PIN_CONFIG_2 (0xCE)
Description: Configures multi-function pins.

Bit	Description	Value	Function	Description
5:2	Configures pin44 as ATSEN or BTSEN.	0010	ATSEN	
		0100	BTSEN	

SMBALERT_MASK_EXTENDED (0xCF)
Description: SMBALERT_MASK bits for bits in the STATUS_EXTENDED command block.

Bit	Function	Description	Value	Function	Description
55	Invalid Access	Invalid PMBus Access (attempt to write read-only command).	0	Invalid	
			1	Not Invalid	
54	Bad Group	Bad Group Command transaction occurred.	0	Fault	
			1	No Fault	
53	RD Group	Group command with READ transaction occurred.	0	Fault	
			1	No Fault	
52	CML Other	A CML error other than those explicitly listed occurred.	0	Fault	
			1	No Fault	
51	PMBus Transaction Aborted by Mater		0	Fault	
			1	No Fault	
50	PMBus Data Arbitration Lost		0	Fault	
			1	No Fault	
49	Master NACK'd Block Size Byte		0	Fault	
			1	No Fault	
45	Too Few Bytes Received		0	Fault	
			1	No Fault	
44	Too Many Bytes Received		0	Fault	
			1	No Fault	
43	Block Size too Small for Command		0	Fault	
			1	No Fault	
42	Block Size too Big for Command		0	Fault	
			1	No Fault	
41	Locked	Attempted to write to write-protected register.	0	Fault	
			1	No Fault	
39	VSP OPEN ChannelB		0	Fault	
			1	No Fault	
38	VSP OPEN ChannelA		0	Fault	
			1	No Fault	
37	VSN OPEN ChannelB		0	Fault	
			1	No Fault	
36	VSN OPEN ChannelA		0	Fault	
			1	No Fault	
28	Sync Fault		0	Fault	
			1	No Fault	
26	No Update	Update not allowed.	0	Fault	
			1	No Fault	
24	Invalid ADDR	Invalid ADDR pin detection.	0	Invalid	
			1	Not Invalid	
19	Invalid PHASE_CONFIG		0	Invalid	
			1	Not Invalid	
18	Config File Error	Invalid configuration file.	0	Invalid	
			1	Not Invalid	
15	Flt High (ChannelB)	SPS over temperature, over current or phase fault condition of channelB.	0	Fault	
			1	No Fault	
14	Flt High	SPS over temperature, over	0	Fault	

Bit	Function	Description	Value	Function	Description
	(ChannelA)	current or phase fault condition of channelA.	1	No Fault	
5	Pre-biased Over-voltage Fault (ChannelB)		0	Fault	
			1	No Fault	
4	Pre-biased Over-voltage Fault (ChannelA)		0	Fault	
			1	No Fault	
3	Tracking Over-voltage Fault (ChannelB)		0	Fault	
			1	No Fault	
2	Tracking Over-voltage Fault (ChannelA)		0	Fault	
			1	No Fault	
1	Fixed Over-voltage Fault (ChannelB)		0	Fault	
			1	No Fault	
0	Fixed Over-voltage Fault (ChannelA)		0	Fault	
			1	No Fault	

READ_VOUT_MIN_MAX (0xD1)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the highest and lowest READ_VOUT values recorded.

Bit	Function	Description	Format
31:16	Read Vout Min	Minimum recorded READ_VOUT.	Linear
15:0	Read Vout Max	Maximum recorded READ_VOUT.	Linear

READ_IOUT_MIN_MAX (0xD2)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the highest and lowest READ_IOUT values recorded.

Bit	Function	Description	Format
31:16	Read Iout Min	Minimum recorded READ_IOUT.	Linear
15:0	Read Iout Max	Maximum recorded READ_IOUT.	Linear

READ_TEMPERATURE_MIN_MAX (0xD3)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the highest and lowest READ_TEMPERATURE_1 values recorded.

Bit	Function	Description	Format
31:16	Read Temp Min	Minimum recorded READ_TEMPERATURE_1.	Linear
15:0	Read Temp Max	Maximum recorded READ_TEMPERATURE_1.	Linear

READ_MFR_VOUT (0xD4)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the actual, measured output voltage.

Bit	Description	Format
15:0		Linear

READ_VIN_MIN_MAX (0xD5)
Description: Returns the highest and lowest READ_VIN values recorded.

Bit	Function	Description	Format
31:16	Read Vin Min	Minimum recorded READ_VIN.	Linear
15:0	Read Vin Max	Maximum recorded READ_VIN.	Linear

READ_IIN_MIN_MAX (0xD6)
Description: Returns the highest and lowest READ_IIN values recorded.

Bit	Function	Description	Format
31:16	Read Iin Min	Minimum recorded READ_IIN.	Linear
15:0	Read Iin Max	Maximum recorded READ_IIN.	Linear

READ_PIN_MIN_MAX (0xD7)
Description: Returns the highest and lowest READ_PIN values recorded.

Bit	Function	Description	Format
31:16	Read Pin Min	Minimum recorded READ_PIN.	Linear
15:0	Read Pin Max	Maximum recorded READ_PIN.	Linear

READ_POUT_MIN_MAX (0xD8)
Status Registers: Page 0 (0), Page 1 (1)
Description: Returns the highest and lowest READ_POUT values recorded.

Bit	Function	Description	Format
31:16	Read Pout Min	Minimum recorded READ_POUT.	Linear
15:0	Read Pout Max	Maximum recorded READ_POUT.	Linear

STATUS_PHASES (0xDC)
Status Registers: Page 0 (0), Page 1 (1)
Description: When PHASE = FFh or 80h, reads to this command return a data word detailing which phases have experienced fault conditions. When PHASE != FFh, reads to this command return a data word detailing which fault(s) the current PHASE has experienced. PHASE number assignment is per PHASE_CONFIG .

Bit	Description	Format
15:0		Integer Unsigned

STATUS_EXTENDED (0xDD)
Description: STATUS_EXTENDED provides a data block indicating the failure of one or more of the devices non standard fault detection features. All supported bits may be cleared either by CLEAR_FAULTS , or individually by writing 1b to the STATUS_EXTENDED register in their position.

Bit	Function	Description	Value	Function	Description
55	Invalid Access	Invalid PMBus Access (attempt to write read-only command).	0		
			1		
54	Bad Group	Bad Group Command transaction occurred.	0		
			1		
53	RD Group	Group command with READ transaction occurred.	0		
			1		
52	CML Other	A CML error other than those explicitly listed occurred.	0		
			1		
51	PMBus Transaction Aborted by Mater		0		
			1		
50	PMBus Data Arbitration Lost		0	No Fault	
			1	Fault	
49	Master NACK'd Block Size Byte		0		
			1		
45	Too Few Bytes		0		

Bit	Function	Description	Value	Function	Description
	Received		1		
44	Too Many Bytes Received		0		
			1		
43	Block Size too Small for Command		0		
			1		
42	Block Size too Big for Command		0		
			1		
41	Locked	Attempted to write to write-protected register.	0		
			1		
39	VSP OPEN ChannelB		0		
			1		
38	VSP OPEN ChannelA		0		
			1		
37	VSN OPEN ChannelB		0		
			1		
36	VSN OPEN ChannelA		0		
			1		
28	Sync Fault		0		
			1		
26	No Update	Update not allowed.	0		
			1		
24	Invalid ADDR	Invalid ADDR pin detection.	0		
			1		
19	Invalid PHASE_CONFIG		0		
			1		
18	Config File Error	Invalid configuration file.	0		
			1		
15	Flt High (ChannelB)	SPS over temperature, over current or phase fault condition of channelB.	0		
			1		
14	Flt High (ChannelA)	SPS over temperature, over current or phase fault condition of channelA.	0		
			1		
5	Pre-biased Over-voltage Fault (ChannelB)		0		
			1		
4	Pre-biased Over-voltage Fault (ChannelA)		0		
			1		
3	Tracking Over-voltage Fault (ChannelB)		0		
			1		
2	Tracking Over-voltage Fault (ChannelA)		0		
			1		
1	Fixed Over-voltage Fault (ChannelB)		0		
			1		
0	Fixed Over-voltage Fault (ChannelA)		0		
			1		

SYNC_CONFIG (0xE4)
Description: Configures options to input synchronization.

Bit	Function	Description	Format
46:41	SYNC IN DIV	SYNC indivision ratio. Value ranges from 0-15d.	Integer Unsigned
27:24	SYNC PWM DIV CHB	SYNC PWM frequency divider channelB.PWN and SYNC divided by 2^(N).	Integer Unsigned
19:16	SYNC PWM DIV CHA	SYNC PWM frequency divider channelA.PWN and SYNC divided by 2^(N).	Integer Unsigned

Bit	Function	Description	Value	Function	Description
47	SYNC OUT EN	Enable SYNC output.	0	Disabled	
			1	Enabled	
40	CLF GAIN CHB	CLF loop gain channelB.	0	1.0	
			1	0.5	
39:38	PLL GAIN CHB	PLL loop gain channelB.	00	1.0	
			01	2.0	
			10	4.0	
			11	8.0	
37:35	SCALAR CHA	Scalar selection for channelA.	000	1/1	
			001	5/4	
			010	9/8	
			011	17/16	
			101	3/4	
			110	7/8	
			111	15/16	
34:32	SCALAR CHB	Scalar selection for channelB.	000	1/1	
			001	5/4	
			010	9/8	
			011	17/16	
			101	3/4	
			110	7/8	
			111	15/16	
31:28	PHASE SHIFT CHB	Phase shift selection for channelB.	0000	0	
			0001	30	
			0010	60	
			0011	90	
			0100	120	
			0101	150	
			0110	180	
			0111	210	
			1000	240	
			1001	270	
			1010	300	
			1011	330	
			1100	360	
23:20	PHASE SHIFT CHA	Phase shift selection for channelA.	0000	0	
			0001	30	
			0010	60	
			0011	90	
			0100	120	
			0101	150	
			0110	180	
			0111	210	
			1000	240	
			1001	270	
			1010	300	
			1011	330	
			1100	360	
15:14	PLL GAIN CHA	PLL loop gain channelA.	00	1.0	
			01	2.0	
			10	4.0	
			11	8.0	
12	CLF EN CHB	CLF loop enable channelB.	0	Disable	
			1	Enable	

Bit	Function	Description	Value	Function	Description
11	PLL EN CHB	PLL loop enable channelB.	0	Disable	
			1	Enable	
10	CLF GAIN CHA	CLF loop gain channelA.	0	1.0	
			1	0.5	
9	CLF EN CHA	CLF loop enable channelA.	0	Disable	
			1	Enable	
8	PLL EN CHA	PLL loop enable channelA.	0	Disable	
			1	Enable	
7	SYNC OUT SEL	SYNC out synchronized to channelA/B.	0	ChannelA	
			1	ChannelB	
6	SYNC CLK INPUT CHB	Synchronize to external or interal clock channelB.	0	External	
			1	Internal	
5	SYNC CLK INPUT CHA	Synchronize to external or interal clock channelA.	0	External	
			1	Internal	

PIN_DETECT_OVERRIDE (0xEE)
Description: Prevent DEFAULT or USER STORE values from over-writing the Pin-Programmed Value.

Bit	Function	Description	Value	Function	Description
1	PD ADDR	Decides SLAVE_ADDRESS command will be restored from NVM/pin ADDR_CONFIG detection.	0	NVM	
			1	VBOOT CHA PIN	
0	PD BOOT	Decides channelA Vboot command will be restored from VOUT_COMMAND NVM/pin VBOOT CHA detection.	0	NVM	
			1	VBOOT CHA PIN	

SLAVE_ADDRESS (0xEF)
Description: Used to program or read-back the slave address of digital communication. When a slave address is updated, the device does not start responding to the new address immediately.

Bit	Description	Format
6:0	PMBus slave address.	Integer Unsigned

MFR_SPECIFIC_WRITE_PROTECT (0xFB)
Description: Provides the user with greater resolution to Write Protect features than the Standard PMBus Functions.

Bit	Function	Description	Value	Function	Description
15	WP ALL		0	No Change	
			1	All writes are rejected	All writes are rejected, except those needed to read certain parameters, or clear faults.Include: PAGE, CLEAR_FAULTS, PHASE, SMBALERT_MASK, STATUS_BYTE, STATUS_WORD, STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML, STATUS_MFR_SPECIFIC, SMBALERT_MASK_EXTENDED and STATUS_EXTENDED.
14	WP WP		0	No Change	

Bit	Function	Description	Value	Function	Description
			1	The PMBus standard WRITE_PROTECT is read-only	
13	WP VOUT		0	No Change	
			1	VOUT_COMMAND, VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW are read-only	
12	WP CAL		0	No Change	
			1	Calibration related commands are read-only	Calibration related commands include: VOUT_TRIM, IOUT_CAL_GAIN, IOUT_CAL_OFFSET and MFR_CALIBRATION_CONFIG.
11	WP OUTFLT		0	No Change	
			1	Output related faults are read-only	Output related faults include: VOUT_MAX, VOUT_MIN, VOUT_OV_FAULT_LIMIT, VOUT_OV_FAULT_RESPONSE, VOUT_OV_WARN_LIMIT, VOUT_UV_WARN_LIMIT, VOUT_UV_FAULT_LIMIT, VOUT_UV_FAULT_RESPONSE, IOUT_OC_FAULT_LIMIT, IOUT_OC_FAULT_RESPONSE, IOUT_OC_WARN_LIMIT, IOUT_UC_FAULT_LIMIT, IOUT_UC_FAULT_RESPONSE, TON_MAX_FAULT_LIMIT and TON_MAX_FAULT_RESPONSE.
10	WP INFLT		0	No Change	
			1	Input related faults are read-only	Input related faults include: VIN_ON, VIN_OFF, VIN_OV_FAULT_LIMIT, VIN_OV_FAULT_RESPONSE, VIN_OV_WARN_LIMIT, VIN_UV_WARN_LIMIT, VIN_UV_FAULT_LIMIT, VIN_UV_FAULT_RESPONSE, IIN_OC_FAULT_LIMIT, IIN_OC_FAULT_RESPONSE, IIN_OC_WARN_LIMIT and PIN_OP_WARN_LIMIT.
9	WP OTHFLT		0	No Change	
			1	Other fault related commands are read-only	Other fault related commands include: OT_FAULT_LIMIT, OT_FAULT_RESPONSE, OT_WARN_LIMIT and MFR_PROTECTION_CONFIG.
8	WP CFG		0	No Change	

Bit	Function	Description	Value	Function	Description
			1	Configuration related commands are read-only	Configuration related commands include: VOUT_MODE, VOUT_TRANSITION_RATE, VOUT_DROOP, VOUT_SCALE_LOOP, FREQUENCY_SWITCH, COMPENSATION_CONFIG, NONLINEAR_CONFIG, PHASE_CONFIG, DVID_CONFIG, PHASE_SHED_CONFIG, ISHARE_CONFIG, SYNC_CONFIG, MISC_OPTIONS, PIN_DETECT_OVERRIDE, SLAVE_ADDRESS and MULTIFUNCTION_PIN_CONFIG.
7	WP SEQ		0	No Change	
			1	Sequencing commands are read-only	Sequencing commands include: TON_DELAY, TON_RISE, TOFF_DELAY and TOFF_FALL.
6	WP ONOFF		0	No Change	
			1	OPERATION and ON_OFF_CONFIG are read-only	
5	WP MFR		0	No Change	
			1	End-manufactuer related commands are read-only	End-manufacturer related commands include: MFR_ID, MFR_MODEL, MFR_REVISION, MFR_DATE.
3	WP DBG		0	No Change	
			1	Test/Debug related commands are read-only	
1	Write Protection NVM		0	No Change	
			1	NVM related commands are rejected	NVM related commands include: STORE_DEFAULT_ALL, RESTORE_DEFAULT_ALL, STORE_USER_ALL and RESTORE_USER_ALL.

MFR_PMBUSCFG_TIMESTAMP (0xFE02)
Description: Contains product number and revision information. Example: For product number BMR 474 2100/001 R1A the fields will be: BMR number = 4742100001. Preliminary revision = Not = 0. Product revision number = 1. Product revision letter = A.

Bit	Function	Description	Format
63:24	BMR number	Number 1-999 9999 999.	Integer Unsigned
22:17	Preliminary revision number	Number 1-63.	Integer Unsigned
16:12	Product revision letter	Number 1-26 respresent A-Z.	ASCII
11	Configuration revision letter	Letter ASCII coded	ASCII

Bit	Function	Description	Value	Description
23	Preliminary revision	0=Non-preliminary revision (e.g. R1A), 1=Preliminary revision (e.g. P1A)	0	Non-preliminary revision (e.g. R1A)
			1	Preliminary revision (e.g. P1A)