TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

OPERATING INFORMATION: COMMON FEATURES

The features listed in the following pages are common to DC/DC converters.

Turn on and off input voltage

The product monitors the input voltage and will turn on and turn off at configured thresholds (see Technical *Specification: part 1 - Electrical Specification*). The turn-on input voltage threshold is set higher than the corresponding turn-off threshold. Hence, there is a hysteresis between turn-on and turn-off input voltage levels.

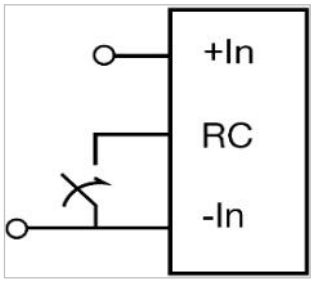
Input voltage transient

The end-user must secure that the transient voltage will not exceed the value stated in the Technical Specification under Absolute maximum ratings of each product. ETSI TR 100 283 examines the parameters of DC distribution networks and provides guidelines for controlling the transient and reduce its harmful effect.

Remote control (RC)

The products are fitted with a remote control function referenced to the primary negative input connection (-In), with negative logic options available. The RC function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. The RC pin has an internal pull up resistor.

The external device must provide a minimum required sink current > 0.5 mA to guarantee a voltage not higher than maximum voltage on the RC pin (see Electrical characteristics table). To turn off the product the RC pin should be left open for a minimum time of 300 µs, the same time requirement applies when the product shall turn on. When the RC pin is left open, the voltage generated on the RC pin is max 1.7 V. The standard product is provided with "negative logic" RC and will be off until the RC pin is connected to the –In. To turn off the product the RC pin should be left open. In situations where it is desired to have the product to power up automatically without the need for control signals or a switch, the RC pin shall be wired directly to –In.



Remote control

Input and output impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. Minimum recommended external input capacitance is given in the *Technical Specification*. Electrolytic capacitors will be degraded in low temperature. The needed input capacitance in low temperature should be equivalent to the value stated in the Technical Specification at 25°C. The performance in some applications can be enhanced by addition of external capacitance as described under External decoupling capacitors (next paragraph). If the input voltage source contains significant inductance, the addition of a low ESR ceramic capacitor of 22 – 100 µF capacitor across the input of the product will ensure stable operation. The minimum required capacitance value depends on the output power and the input voltage. The higher output power the higher input capacitance is needed.

External decoupling capacitors

When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load.

The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several parallel capacitors to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. It is equally important to use low resistance and low inductance PWB layouts and cabling.

External decoupling capacitors will become part of the product's control loop. The control loop is optimized for a wide range of external capacitance and the maximum recommended value that could be used without any additional analysis is found in the Technical Specification under Electrical specifications. Output filter can be configured and simulated based on the needed control loop and transient response.

For further information please contact your local Flex Power Modules' representative or email us at pm.info@flex.com.

Output voltage adjust using PMBus

The output voltage of the product can be reconfigured via PMBus command VOUT_COMMAND (0x21) or VOUT_TRIM (0x22). This can be used when adjusting the output voltage above or below output voltage initial setting up to a certain level, see Electrical specification for adjustment range.
When changing the output voltage, the voltage at the output pins must be kept within Vtrim max and Vtrim min. Output voltage setting must be kept below the threshold of the over voltage protection (OVP) to prevent the product from shutting down. At increased output voltages the maximum power rating of the product remains the same, and the max output current must be decreased correspondingly.

Margin up and down control

These controls allow the output voltage to be momentarily adjusted, either up or down, by a nominal 10%. The margin high and margin low shall be limited to max and min output voltage, if the nominal output voltage is changed. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors.

The margin up and down levels of the product can easily be re-configured using Flex Power Designer software.

Soft start power up and soft stop

The default rise time for a single product is 10 ms. When starting by applying input voltage the control circuit boot-up time adds approximately an additional 15 ms delay. The soft-start and soft-stop control functionality allows the output voltage to ramp-up and ramp-down with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple controllers.

The rise time is the time taken for the output to ramp to its target voltage, while the fall time is the time taken for the output to ramp down from its regulation voltage to 0 V. The TON_DELAY (0x60) time sets a delay from when the output is enabled until the output voltage starts to ramp up. The TOFF_DELAY (0x64) delay time sets a delay from when the output is disabled until the output voltage starts to ramp down.
By default, soft-stop is disabled, and the regulation of output voltage stops immediately when the output is disabled. Soft-stop can be enabled through the PMBus command ON_OFF_CONFIG (0x02). The delay and ramp times can be reconfigured using the PMBus commands TON_DELAY (0x60), TON_RISE (0x61), TOFF_DELAY (0x64) and TOFF_FALL (0x65).

Pre-bias start-up

The product has a pre-bias start up functionality and will not sink current during start up if a pre-bias source is present at the output terminals. If the pre-bias voltage is lower than the target value set in VOUT_COMMAND (0x21), the product will ramp up to the target value. If the pre-bias voltage is higher than the target value set in VOUT_COMMAND (0x21), the product will ramp down to the target value and in this case sink current. It is recommended to keep TON_RISE below 100ms.

Over/under temperature protection (OTP/UTP)

The products are protected from thermal overload by an internal over temperature sensor.
The product will make continuous attempts to start up (non-latching mode) and resume normal operation automatically when the temperature has dropped below the temperature threshold set in command OT_WARN_LIMIT (0x51). The OTP and hysteresis of the product can be re-configured using the PMBus interface. The product also has an under-temperature protection. The OTP and UTP fault limit and fault response can be configured via the PMBus.
Note: using the fault response "continue without interruption" may cause permanent damage to the product.

Input over/under voltage protection

The product can be protected from high input voltage and low input voltage by a pre-configured value with a response time of 30µs. The over/under-voltage fault level and fault response is easily configured using Flex Power Designer software.
For more information, see *Technical Reference Document: PMBus*.

Output Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 30% above the nominal output voltage. If the output voltage exceeds the OVP limit, the product can respond in different ways.
The default response from an over voltage fault is to immediately shut down, with a response time of ~70us. The device will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled.
The OVP fault level and fault response can be configured via the PMBus interface
For more information, see *Technical Reference Document: PMBus*.

Over current protection (OCP)

The products include current limiting circuitry for protection at continuous overload. For standard configuration the output voltage will decrease towards 0.25×Vout, set in command IOUT_OC_LV_FAULT_LIMIT (0x48), then shutdown and automatic restart (hiccup mode) for output currents in excess of max output current (max IO). The product will resume normal operation after removal of the overload. The load distribution should be designed for the maximum output short circuit current specified.
For more information, see *Technical Reference Document: PMBus.*

Switching frequency

The product is optimized at the frequency given in the Technical Specification under part 1- Electrical Specification , but can run at lower and higher frequencies through PMBus configuration. The electrical performance can be affected at different frequencies. Please contact your local Flex Power Modules FAE for more details.

Address offset

The command FW_CONFIG_PMBUS (0xC9) can be configured to utilize different address offset option. There are 2 different address setting options.

1. The bit 16 in command 0xC9 must be set to 1 to enable PMBus address offset via resistors.
2. The resistor address offset in combination with a value set by PMBus base address offset, [31:24] in command FW_CONFIG_PMBUS (0xC9). This can be chosen when 1 address resistor is used.
3. A pre-configured PMBus address, [23:17] in FW_CONFIG_PMBUS (0xC9). The bit 16 in command 0xC9 must be set to 0 to enable digital PMBus address offset. The digital PMBus address offset in combination with a digital PMBus base address offset, [31:24] in command FW_CONFIG_PMBUS (0xC9) adds a larger range of address possibilities. This combination can be chosen if no address resistors are used.

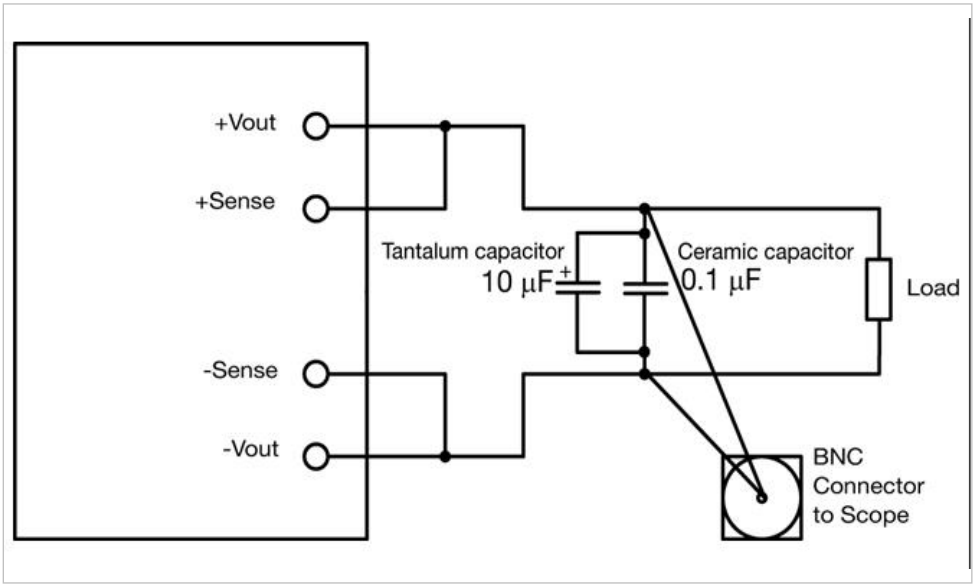
The PMBus-address offset's with resistor value increments the address value following the formula in the PMBus Addressing section of documentation.

Feed Forward Capability

The BMR492 products has a Feed Forward function implemented that can handle sudden input voltage changes. The output voltage will be regulated during an input transient and will typically stay within 3% when an input transient is applied. The Feed Forward acts on both positive and negative input voltage transients.

Output ripple and noise

Output ripple and noise measured according to figure below.
See Design Note 022 for detailed information



Output ripple and noise test set-up

Non-Volatile Memory (NVM)

The product incorporates two Non-Volatile Memory areas for storage of the PMBus command values; the Default NVM and the User NVM. The Default NVM is pre-loaded with Flex factory default values. The Default NVM is write-protected and can be used to restore the Flex factory default values through the command RESTORE_DEFAULT_ALL (0x12).

The User NVM is pre-loaded with Flex factory default values. The User NVM is writable and open for customization. The values in NVM are loaded during initialization according to section Initialization Procedure, where after commands can be changed through the PMBus Interface.

The module contains a one-time programmable memory (OTP) used to store configuration settings, which will not be programmed into the device OTP automatically. The STORE_USER_ALL(0x15) commands must be used to commit the current settings are transferred from RAM to OTP as device defaults.

Power good

The power good pin (PG) indicates when the product is ready to provide regulated output voltage to the load. During ramp-up and during a fault condition, PG is held high. By default, PG is asserted low after the output has ramped to setting according to POWER_GOOD_ON (0x5E), and de-asserted if the output voltage falls below the setting according to POWER_GOOD_OFF (0x5F). These thresholds may be changed using the PMBus commands POWER_GOOD_ON (0x5E) and POWER_GOOD_OFF (0x5F).

By default, the PG pin is configured as Push/pull output.

The polarity is by default configured to active low, the polarity of PG can be set to active high using bit [39] in the command FW_CONFIG_PMBUS (0xC9):

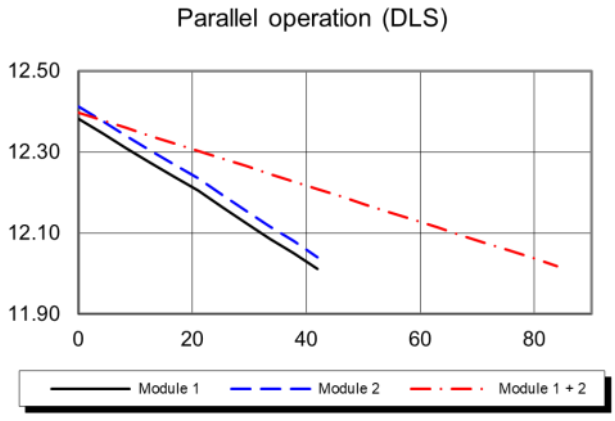
bit[39] = 0 (active low)
bit[39] = 1 (active high)

The product provides a Power Good flag in the Status Word register that indicates the output voltage is within a specified tolerance of its target level and no-fault condition exists.

For more information, see *Technical Reference Document: PMBus*.

Parallel operation Droop Load Sharing (DLS)

Two or more products may be paralleled for redundancy if the total power is equal or less than P_O max. The products provide output voltage droop corresponding to pre-configured artificial resistance in the output circuit to enable direct paralleling. The stated output voltage set point is at no load. The output voltage will decrease when the load current is increased. This feature allows the products to be connected in parallel and share the current. This feature allows the products to be connected in parallel and share the current with 10% accuracy at max output power . This means that up to 90% of max rated current from each module can be utilized. The product measures reversed current, and will compensate the output voltage in these situations. At reversed current > 40A the product will shut down immediately, to avoid this protection, it is recommend to load on after output is established . Note that continuous restarts after a fault (“hiccup mode”) are not recommended for parallel operation. Droop Load Share variants (DLS) will have a default response from an OCP fault consisting of a response delay of 2ms then immediately shut down. To prevent unnecessary current stress, changes of the output voltage must be done with the output disabled. This must be considered for all commands that affect the output voltage.



POWER MANAGEMENT

PMBus overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin. The following product parameters can continuously be monitored by a host: Input voltage, output voltage/current, duty cycle and internal temperature.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface.

Throughout this document, different PMBus commands are referenced. The Flex Power Designer software suite can be used to configure and monitor this product via the PMBus interface. More information is found on our website.

SMBus interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I²C (master must allow for clock stretching) or SMBus host device. In addition, the product is compatible with PMBus version 1.3 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports 100 kHz and 400 kHz bus clock frequency only. The PMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

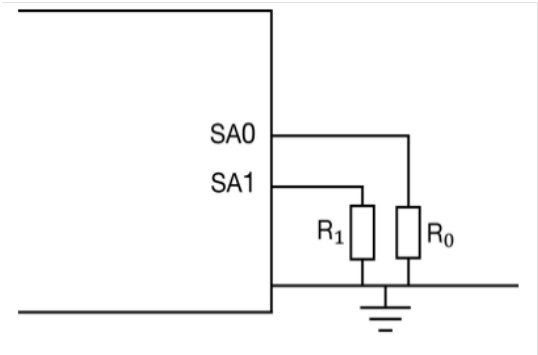
$$\tau = R_P C_p \leq 1us \qquad \text{Eq. 7}$$

where R_P is the pull-up resistor value and C_P is the bus load. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply between 2.7 to 3.8 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

It is recommended to always use PEC (Packet Error Check) when communicating via PMBus.

PMBus addressing

The following figure and table show recommended resistor values with min and max voltage range for hard-wiring PMBus addresses (series E96, 1% tolerance resistors suggested):



Schematic of connection address resistor

R_{SA0} [kΩ]	SA0/SA1	R_{SA0} [kΩ]	SA0/SA1
10	0	54.9	4
15.4	1	84.5	5
23.7	2	130	6
36.5	3	200	7

The SA0 and SA1 pins can be configured with a resistor to GND according to the following equation.

PMBus Address = 8 x (SA1 index) + (SA0 index)

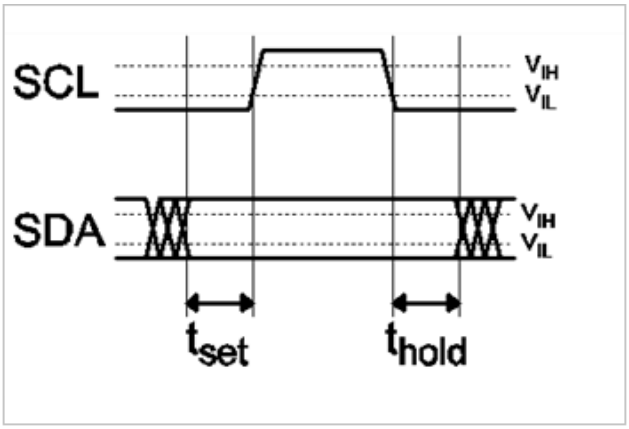
PMBus base address value is configured via PMBus command 0xC9. The default base address is 0x00.

The allowed range of the PMBus address is: 1-126 excluding 12 and 16. When the calculated PMBus address falls outside the allowed range address 126 is assigned instead. It is not recommended to keep the SA0/SA1 pins left open.

I2C/SMBus timing

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the rising edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. This product supports the BUSY flag in the status commands to indicate product being too busy for SMBus response. A bus-free time delay between every SMBus transmission (between every stop & start condition) must occur. Refer to the SMBus specification, for SMBus electrical and timing requirements.

Note that an additional delay of 5 ms has to be inserted in case of storing the RAM content into the internal non-volatile memory.



Set-up and hold timing diagramm

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Output current	READ_IOUT
Temperature*	READ_TEMPERATURE_1
Switching frequency	READ_FREQUENCY
Duty cycle	READ_DUTY_CYCLE

* reports the temperture from temperature sensor set in command 0xDC, internal (controller IC)/external (temp. sensor)

Monitoring faults

Fault conditions can be detected using the SALERT pin, which will be asserted low when any number of pre-configured fault or warning conditions occurs. The SALERT pin will be held low until faults and/or warnings are cleared by the CLEAR_FAULTS command, or until the output voltage has been re-enabled. It is possible to mask which fault conditions should not assert the SALERT pin by the command SMBALERT_MASK. In response to the SALERT signal, the user may read a number of status commands to find out what fault or warning condition occurred, see table below.

Fault and warning	PMBus command
Overview, Power Good	STATUS_BYTE STATUS_WORD
Output voltage level	STATUS _VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

General PMBus command summary

PMBus signal interfaces characteristics

Characteristic	conditions	minimum	typical	maximum	unit
PMBus signal interface characteristics					
Input clock frequency drift	External sync.	-5		5	%
Initialization time	From VI > 27 V to ready to		15		ms
Output voltage total on delay time	Enable by input voltage		T_{INIT} + T_{ONdel}		
	Enable by RC or CTRL pin		T_{ONdel}		
Logic output low signal	SCL, DA, SYNC, GCB, SALERT, PG, sink/source current = 4 mA			0.25	V
Logic output high signal		2.7			V
Logic output low sink				4	mA
Logic output high source				4	mA
Logic input low threshold	SCL, SDA, CTRL, SYNC			0.6	V
Logic input high threshold		2.1			V
Logic pin input	SCL, SDA, CTRL, SYNC		10		pF
Supported SMBus		100		400	kHz
SMBus bus free time	STOP bit to START bit		1.3		µs
SMBus SDA setup time from SCL			100		µs
SMDBus SDA hold time			0		ns
SMBus START/STOP condition setup/hold time			600		ns
SCL low period		1.3			µs
SCL high period			0.6	50	µs