TECHNICAL REFERENCE DOCUMENT: DESIGN & APPLICATION GUIDELINES

Operating Information

BMR 510 is a two-phase non-isolated high-efficiency small footprint step-down power block. It includes drivers, MOSFETs, output inductors and sensing circuitry for output currents and junction temperatures. Further, it includes over-current and over-temperature protection functions with fault reporting. The product has two independent outputs, which can be used separately (dual rail) or in parallel (single rail dual phase). Several products can be paralleled for multiphase operation.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. If the input voltage source contains significant inductance, the addition of a capacitor with low ESR at the input of the product will ensure stable operation.

External Input Capacitors

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage during large load transients.

It is recommended to use at least 70 µF ceramic external input capacitors for each module, placed closed to input pins and with low impedance connections to the VIN and GND pins to be effective. See application note AN323 for further guidelines on how to choose and apply input capacitors.

External Output Capacitors

The output capacitor requirement depends on two considerations: output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to minimize output voltage deviation.

It is recommended to place at least 140 µF ceramic capacitors close to each product, since it has no internal output capacitance. In addition, low ESR ceramic and low ESR electrolytic/polymer capacitors shall be placed as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts for capacitance to be effective.

See application note AN321 for further guidelines on how to choose and apply output capacitors.

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Enable

When the voltages at VIN and VCC pins are sufficiently high and the EN pin is high, operation begins. The EN pins are connected together in the product and common to both phases.

Pulse-Width Modulation (PWM)

The pulse-width modulation input pins are capable of tri-state input. When the PWM input is high, the high-side MOSFET is turned on and the low-side MOSFET is turned off. When the PWM input is low, the high-side MOSFET is turned off and the low-side MOSFET is turned on. If the PWM input is floated, it will force the PWM into tri-state.

When the PWM input signal is within the tri-state threshold window for a typical 40 ns, the high-side MOSFET turns off immediately, and the low-side MOSFET enters diode emulation mode, which is on until zero-current detection.

The tri-state PWM input can come from a forced mid-voltage PWM signal or made by floating the PWM input. The internal current source charges the signal to a middle voltage.

When operating both phases of the product, PWM1 and PWM2 pulses shall be 180° shifted.

Diode Emulation Mode

In diode emulation mode, when PWM is in a tri-state input, the low side MOSFET is turned on whenever the inductor current is positive. The low side MOSFET turns off if the inductor current is negative or after the inductor current crosses the zero current.

Current Sense

The ISEN pins are bidirectional current source outputs proportional to the inductor current of each phase. The gain is 5 µA/A. An external resistor must be used to program the voltage gain proportional to the inductor current, if needed.

The ISEN outputs have two states. In disable mode (EN = low), the current sense circuit is disabled and the ISEN outputs are in the high impedance state.

EN	ISEN
High	Active
Low	Hi-Z

The voltage of the ISEN pins must be within the specified voltage range to achieve an accurate current reporting. In general, there is a resistor, RIOUT, connected from ISEN to a reference voltage, VCM, that can sink small currents to provide enough voltage level to meet the required operating voltage range. Proper VCM and RIOUT values can be determined by the equation:

$0.7\ V < (I_{ISEN} \times R_{IOUT}) + V_{CM} < 2.1\ V$

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The current sense outputs can be used by the controller to monitor the output current accurately. The cycle -by-cycle current information from the ISEN pins can be used for phase- current balancing, over-current protection, and voltage positioning (output voltage droop).

Current Limit

When high side over-current is detected, the high side MOSFET turns off for that PWM cycle. If there are ten consecutive cycles of a high side current limit event, the high side MOSFET latches off, TSEN pulls high to VCC, and the low side MOSFET turns on until zero current detection. Toggle EN or recycle VIN or VCC to release the latch and restart operation.

When the low side under-current is detected (negative current) the low side MOSFET is turned off and the high side MOSFET is turned on for 200 ns to limit the negative current cycle by cycle. The low side negative current limit will not trigger a fault report.

Temperature Sense with Fault Indicator

The TSEN pins have two functions:
1. Junction temperature sense.
2. Fault detection.
The voltage at the TSEN pin is proportional to the junction temperature whenever VIN and VCC is higher than their UVLO thresholds. The gain is 8 mV/°C and has an 800 mV offset at 25 °C. Examples:
V_{TSEN} = 0.8 V @ TJ = 25 °C
V_{TSEN} = 1.6 V @ TJ = 125 °C
When any fault occurs, TSEN is pulled to the VCC voltage to report the fault event, regardless of the current junction temperature. 200 ns after the fault has occurred, the PWM impedance changes accordingly to indicate the fault type:

Fault Type	PWM Impedance
Over-current limit protection	10 kΩ to GND
Over-temperature limit protection	20 kΩ to GND
Internal short protection	1 kΩ to VCC

For multiphase operation, connect TSEN of each phase together to report the highest junction temperature. It is recommended to add a filter to the TSEN signal. See Application Example for typical component values to use.

Temperature Limit

When the over-temperature threshold is exceeded, the high side MOSFET latches off, TSEN pulls high to VCC, and the low side MOSFET turns on until zero current detection. Toggle EN or recycle VIN or VCC to release the latch and restart operation.