Technical Specification

BMR520 series DC-DC Converters Input 42.5-75 V, Output up to 25 A / 300 W	28701-BMR520 Rev A March 2022
	© Flex

Key Features

- Vertical mounting DC-DC converter
- Board-space efficient solution
- One control assembly supports 3 power blades
- 12 Vout, 300W max power per power blade
- High efficiency, typical 94% at 53 Vin, half load
- Small footprint
  - Control assembly – 17mm x 17mm x 11.6mm (0.67” x 0.67” x 0.46”)
  - Power blade – 40mm x 20mm x 17mm (1.58” x 0.67” x 0.79”)
- 1500V input to output isolation
- Meets safety requirements per IEC/EN/UL 62368-1
- PMBus 1.3 Compliant
- MTBF 19.6 million hours

General Characteristics

- Configurable with PMBus
- Full configuration support with Flex Power Designer
- Full featured input/output telemetry
- Configurable protections
  - Input UVP
  - Output UVP/OVP/OCP/OTP
- Differential remote sense
- ISO 9001/14001 certified supplier
- Highly automated manufacturing ensures quality

Safety Approvals

Design for Environment

Meets requirements in high-temperature lead-free soldering processes.

Contents

flex

Technical Specification

BMR520 series DC-DC Converters Input 42.5-75 V, Output up to 25 A / 300 W	28701-BMR520 Rev A March 2022 © Flex

Ordering Information

Product program	Function	Output
BMR5201000	Power blade	12V / 25A
BMR5202000/001	Controller assembly	

Product number and Packaging

BMR520 $n_1n_2n_3n_4/n_5n_6n_7n_8$									
Options	n_1	n_2	n_3	n_4	/	n_5	n_6	n_7	n_8
Module type	o	o			/				
Variant info			o	o	/				
Configuration file					/	o	o	o	
Packaging					/				o

Options	Description	
n_1n_2	10 20	Power blade – baseplated, LGA Controller assembly – Open Frame, Box Pin
n_3n_4	00	Reserved for options
$n_5n_6n_7$	001	Default config for one controller assembly with three power blades (only applied for controller assembly)
n_8	C	Antistatic tape and reel packaging

Example: A completed power solution for one controller assembly plus three power blades with baseplate and LGA foot print would be 3 x BMR5201000 + 1 x BMR5202000/001

Note: Power blade does not support special configurations in the part number suffix n5n6n7; those positions are left blank.

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF= 1/λ) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Flex Power uses Telcordia SR-332 Issue 4 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 4 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state	Std. deviation, σ
51 nFailures/h	6.0 nFailures/h

MTBF (mean value) for BMR520 series = 19.6 Mh
MTBF at 90% confidence level = 17 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2011/65/EU and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Flex Power Modules products are found in the Statement of Compliance document.

Flex Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Flex Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Flex Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

flex

Technical Specification

BMR520 series DC-DC Converters Input 42.5-75 V, Output up to 25 A / 300 W	28701-BMR520 Rev A March 2022
	© Flex

Safety Specification

General information

Flex Power DC/DC converters and DC/DC regulators are designed in accordance with the safety standards IEC 62368-1, EN 62368-1 and UL 62368-1 *Audio/video, information and communication technology equipment - Part 1: Safety requirements*

IEC/EN/UL 62368-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Electrically-caused fire
- Injury caused by hazardous substances
- Mechanically-caused injury
- Skin burn
- Radiation-caused injury

On-board DC/DC converters, Power interface modules and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without “conditions of acceptability”. Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use shall comply with the requirements in IEC/EN/UL 62368-1. Product related standards, e.g. IEEE 802.3af *Power over Ethernet*, and ETS-300132-2 *Power interface at the input to telecom equipment, operated by direct current (dc)* are based on IEC/EN/UL 60950-1 with regards to safety.

Flex Power DC/DC converters, Power interface modules and DC/DC regulators are UL 62368-1 recognized and certified in accordance with EN 62368-1. The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

Isolated DC/DC converters & Power interface modules

The product may provide basic or functional insulation between input and output according to IEC/EN/UL 62368-1 (see Safety Certificate), different conditions shall be met if the output of a basic or a functional insulated product shall be considered as ES1 energy source.

For basic insulated products (see Safety Certificate) the output is considered as ES1 energy source if one of the following conditions is met:

- The input source provides supplementary or double or reinforced insulation from the AC mains according to IEC/EN/UL 62368-1.
- The input source provides functional or basic insulation from the AC mains and the product’s output is reliably connected to protective earth according to IEC/EN/UL 62368-1.

For functional insulated products (see Safety Certificate) the output is considered as ES1 energy source if one of the following conditions is met:

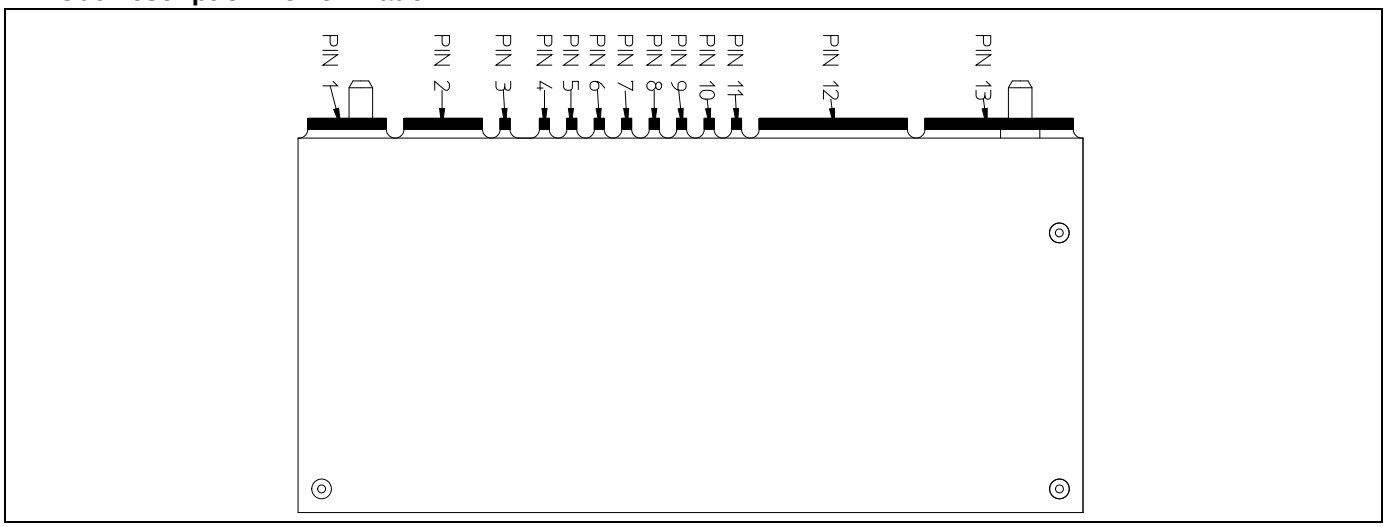
- The input source provides double or reinforced insulation from the AC mains according to IEC/EN/UL 62368-1.
- The input source provides basic or supplementary insulation from the AC mains and the product’s output is reliably connected to protective earth according to IEC/EN/UL 62368-1.
- The input source is reliably connected to protective earth and provides basic or supplementary insulation according to IEC/EN/UL 62368-1 and the maximum input source voltage is 60 Vdc.

Galvanic isolation between input and output is verified in an electric strength test and the isolation voltage (V_{iso}) meets the voltage strength requirement for basic insulation according to IEC/EN/UL 62368-1.

It is recommended to use a slow blow fuse at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter. In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating

Pin-Out Description Power Blade

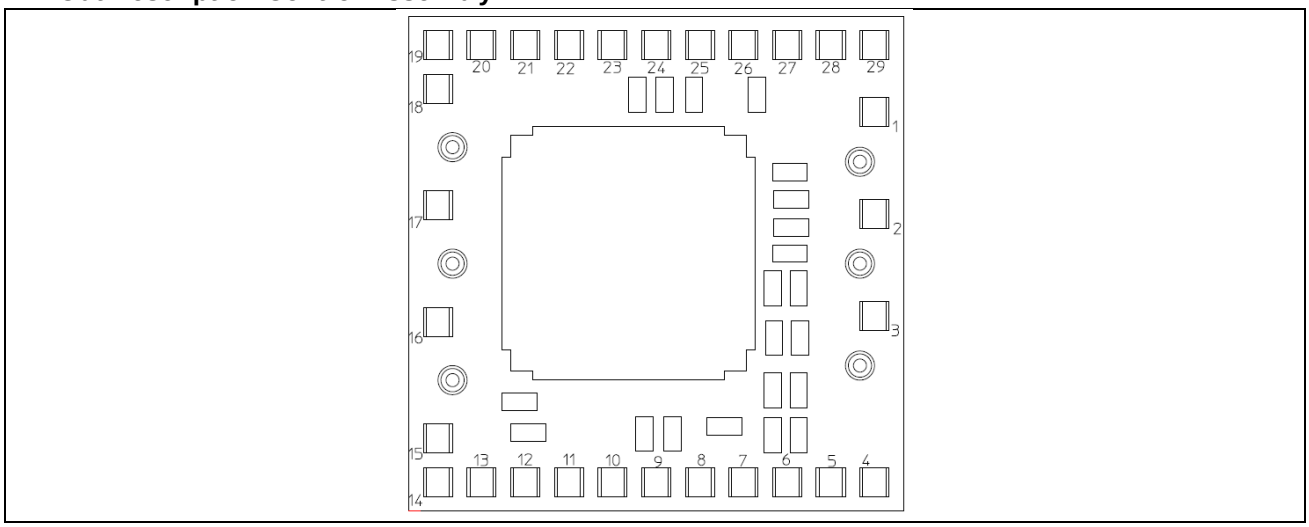


Pin layout, side view from baseplate.

Pin	Designation	Type	Function
1	+IN	Power	Input voltage positive.
2	-IN	Power	Input voltage negative.
3	VP	Auxiliary Power Input	Primary side driver voltage supply. Should be connected to VP output pin of Control Assembly.
4	PWMX	Input	Primary side PWM signal. Connect to PWMXx* output of Control Assembly.
5	PWMY	Input	Primary side PWM signal. Connect to PWMYx* output of Control Assembly.
6	VCC5	Auxiliary Power Input	Secondary side power supply for IC and driver.
7	VCC1V8	Power	Secondary side offset voltage for current sense circuit referenced to GND
8	VS	Auxiliary Power Input	Secondary side voltage supply referenced to GND
9	Io_sense	Output	Output current sense signal. Should be connected to VCC1V8 by a jumper if not used.
10	START	Input	Secondary side synchronization input. Connect to STARTx* output of Control Assembly.
11	TM	Input	Temperature sense output. Connect to TMx* input of Control Assembly.
12	GND	Power	Power ground (-OUT)
13	+OUT	Power	+ Output voltage.

* x = 1, 2, 3, is the Blade number in application.

Pin-Out Description Control Assembly

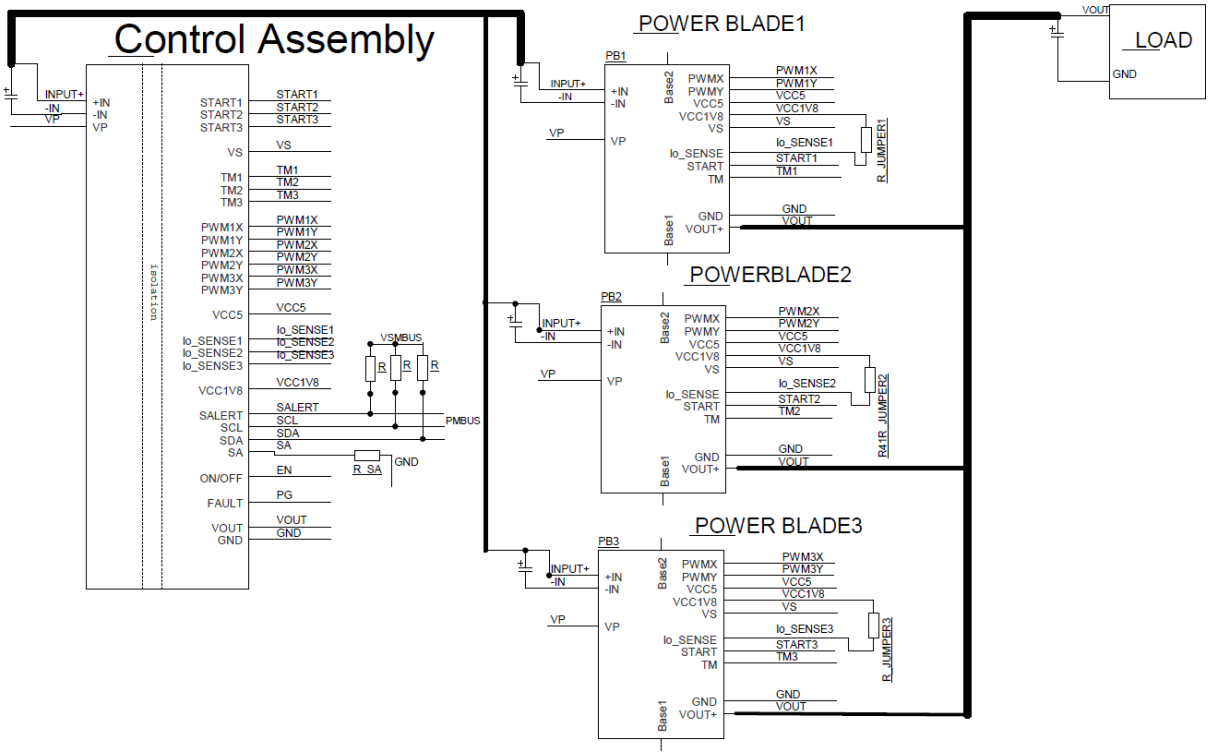


Pin layout, bottom view .

Pin	Designation	Type	Function
1	+IN	Power Input	Input voltage positive.
2	VP	Auxiliary Power Output	Primary side driver voltage supply. Connect to VP pin of cell x.
3	-IN	Power Input	Input voltage negative.
4	Io_SENSE3	Input	Current sensing cell3. Connect to VCC1V8 if not used.
5	Io_SENSE2	Input	Current sensing cell2. Connect to VCC1V8 if not used.
6	Io_SENSE1	Input	Current sensing cell1.
7	PG	Output Open drain	Power good . Can be left open due to internal pull-up.
8	EN	Input	Output voltage enable /CTRL pin. Can be left open if unused due to internal pull-up. Referenced for GND, positive logic, left open will let the module operate.
9	SA	Input	Address setting. Connect a resistor divider to GND in order to define PMBus addresses. See section PMBus Interface.
10	SCL	Input	PMBus Clock. Clock for PMBus communication. Requires a pull-up resistor, also when unused. See section PMBus Interface.
11	SDA	Input/ Output Open drain	PMBus Data. Data signal for PMBus communication. Requires a pull-up resistor, also when unused. See section PMBus Interface.
12	SALERT	Output Open drain	PMBus Alert. Asserted low when any of the configured protection mechanisms indicate a fault.
13	VOUT	Input	Vout sensing pin, connect to positive out common point.
14	START3	Output	Secondary side synchronization output for cell 3. If no cell 3 leave floating.
15	START2	Output	Secondary side synchronization output for cell 2. If no cell 2 leave floating.
16	VS	Auxiliary Power Output	Secondary side voltage supply output. Connect to VS of all blades.

Pin	Designation	Type	Function
17	GND	Reference	Auxiliary power reference and digital ground.
18	START1	Output	Secondary side synchronization output for cell 1. If no cell 1 leave floating.
19	PWM3Y	Output	Primary side PWMY output to cell 3. Connect to PWMY pin of cell 3.If no cell 3 leave floating.
20	PWM3X	Output	Primary side PWMX output to cell 3. Connect to PWMX pin of cell 3. If no cell 3 leave floating.
21	PWM2Y	Output	Primary side PWMY output to cell 2. Connect to PWMY pin of cell 3. If no cell 2 leave floating.
22	PWM2X	Output	Primary side PWMX output to cell 2. Connect to PWMX pin of cell 3. If no cell 2 leave floating.
23	PWM1Y	Output	Primary side PWMY output to cell 1. Connect to PWMY pin of cell 3. If no cell 1 leave floating.
24	PWM1X	Output	Primary side PWMX output to cell 1. Connect to PWMX pin of cell 3. If no cell 1 leave floating.
25	VCC5	Auxiliary Power Output	Secondary side Power supply for IC and driver. Connect to VCC5 pin of cell x
26	VCC1V8	Auxiliary Voltage Output	Secondary side offset voltage for current sense circuit. Connect to VCC1V8 pin of cell x.
27	TM3	Input	Temperature sense input for cell 3. Connect to TM output of cell 3. If no cell 3, leave unconnected.
28	TM2	Input	Temperature sense input for cell 2. Connect to TM output of cell 2. If no cell 2, leave unconnected.
29	TM1	Input	Temperature sense input for cell 1. Connect to TM output of cell 1. If no cell 1, leave unconnected.

Application Example



flex

Technical Specification

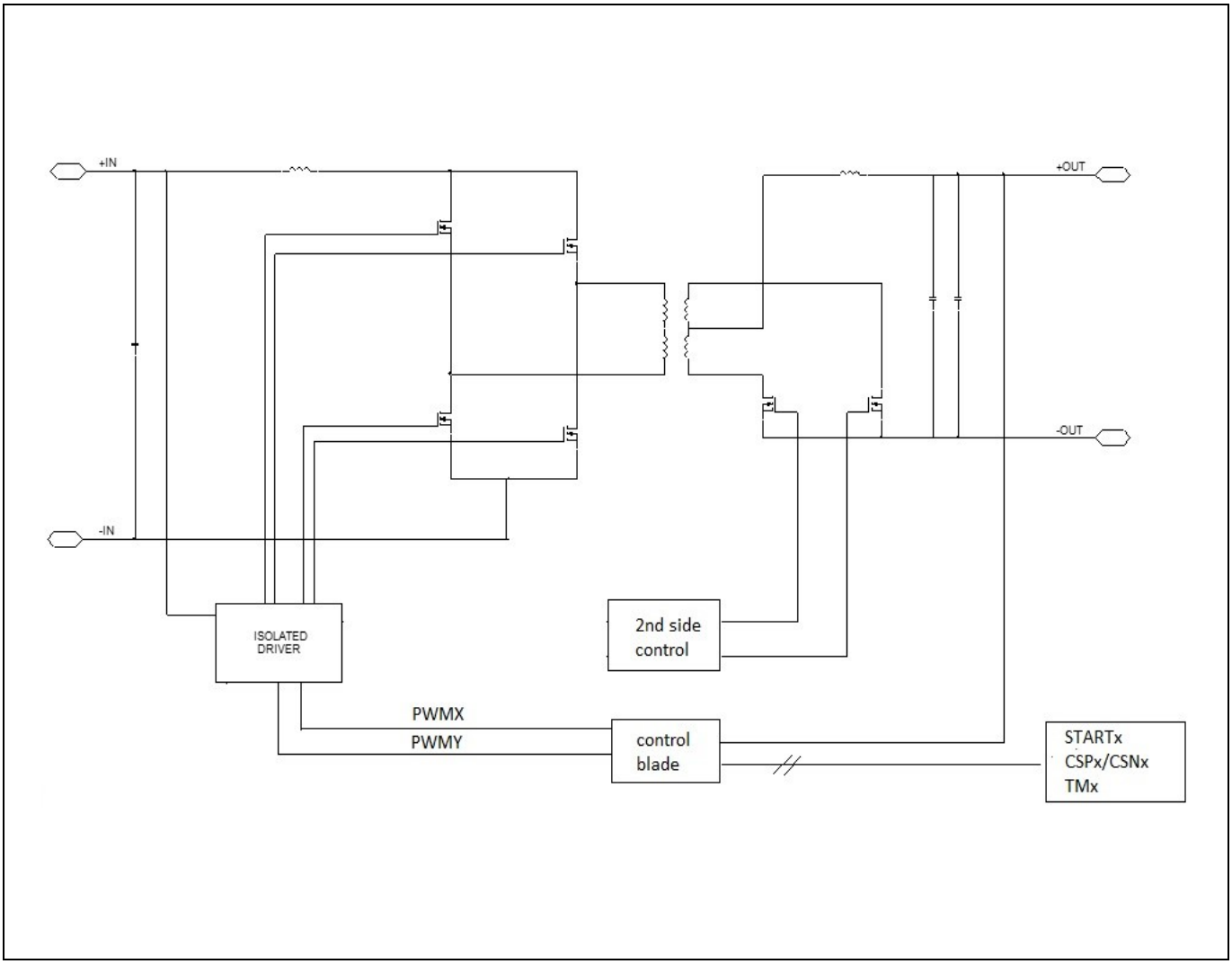
BMR520 series DC-DC Converters Input 42.5-75 V, Output up to 25 A / 300 W	28701-BMR520 Rev A March 2022 © Flex

Absolute Maximum Ratings

Characteristics			min	typ	max	Unit
T_{P1}	Operating Temperature (see Thermal Consideration section)		-40		125	°C
T_S	Storage temperature		-55		125	°C
V_I	Input voltage		42.5		75	V
C_{out}	Output capacitance		200	470	2500	µF
V_{iso}	Isolation voltage (input to output test voltage)				1500	Vdc
V_{iso}	Isolation voltage (input to baseplate qualification test voltage)				750	Vdc
V_{iso}	Isolation voltage (baseplate to output qualification test voltage)				750	Vdc
V_{RC}	Remote Control pin voltage (see Operating Information section)	Positive logic option	-0.5		5	V
		Negative logic option	-0.5		5	V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the Electrical Specification section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fundamental Circuit Diagram



Common Electrical Specification

This section includes parameter specifications common to all product versions within the product series. Typically these are parameters defined by the digital controller of the products. In the table below PMBus commands for configurable parameters are written in capital letters.

T_{P1} = -40 to +90 °C, V_I = 42.5 to 75 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 53 V, max I_O, unless otherwise specified under Conditions:
BMR520XXXX/XXX (Stand alone)

Characteristics		Conditions	min	typ	max	Unit
f_{SW} = $1/T_{SW}$	Switching Frequency			250		kHz
	Switching Frequency Range, Note 1	PMBus configurable FREQUENCY_SWITCH				kHz

T_{INIT}	Initialization Time	From V_I > ~27 V to ready to be enabled	12		ms
T_{ONdel_tot}	Output voltage Total On Delay Time	Enable by input voltage	T_{INIT} + T_{ONdel}		
		Enable by RC or CTRL pin	T_{ONdel}		
T_{ONdel}	Output voltage On Delay Time	PMBus configurable Turn on delay duration	0		ms
		Range TON_DELAY	0	127	ms
T_{OFFdel}	Output voltage Off Delay Time	PMBus configurable Turn off delay duration, Note 2	0		ms
T_{ONrise} / $T_{OFFfall}$	Output voltage On/Off Ramp Time (0-100%-0 of V_O)	Turn on ramp duration -Stand alone	10		ms
		Turn off ramp duration	Disabled in standard configuration. Turn off immediately upon expiration of Turn off delay.		ms
		Ramp time accuracy for standalone operation (actual ramp time vs set value)	±1		%
V_{Ioff}	Input turn off range	States the level where the output voltage is disabled, PMBus configurable	40		V
V_{Ion}	Input turn on range	States the level where the output voltage is enabled, PMBus configurable.	42		V

flex

Technical Specification

BMR520 series DC-DC Converters Input 42.5-75 V, Output up to 25 A / 300 W	28701-BMR520 Rev A March 2022
	© Flex

Characteristics		Conditions	min	typ	max	Unit
Power Good , PG	PG threshold VR_RDY pin	PMBus configurable Rising		100		% V_O
		PMBus configurable Falling		When output voltage disabled		V_O
Input Under Voltage Protection, IUVP	threshold	PMBus configurable		40		V
	threshold range	VIN_UV_FAULT_LIMIT		0-100		%V_{IN}
	Set point accuracy			1		%
	response delay			100		µs
	Fault response	PMBus configurable VIN_UV_FAULT_RESPONSE		Latch (0x80)		
Input Over Voltage Protection, IOVP	threshold	PMBus configurable		NA		V
	threshold range	VIN_OV_FAULT_LIMIT		0-100		%V_{IN}
	Set point accuracy			±1		%
	response delay			100		µs
	Fault response	PMBus configurable VIN_OV_FAULT_RESPONSE		Latch (0x80)		
Output Voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold	PMBus configurable		10		V_O
	OVP threshold	PMBus configurable		14		V_O
	UVP/OVP response time			100/50		µs
	Fault response	PMBus configurable VOUT_UV_FAULT_RESPONSE		Latch (0x80)		
		PMBus configurable VOUT_OV_FAULT_RESPONSE		Latch (0x80)		
Over Current Protection, OCP ,Note 9	Peak OCP threshold	Set value			50	A
	Peak OCP threshold range	PMBus configurable MFR_IMON, TEL_IOUT_FSR		0		
	Peak OCP response time			150		ns
	Average OCP threshold	Set value		32		A
	Average OCP threshold range	PMBus configurable IOUT_OC_FAULT_LIMIT	0	32	40	A
	Average OCP warning threshold	Set value		30		A
	Average OCP warning threshold range	PMBus configurable IOUT_OC_WARN_LIMIT	0		40	A
	Response time				400	us
	Fault response	IOUT_OC_FAULT_RESPONSE		Latch (0x80)		
Over Temperature Protection, OTP, Note 7	Threshold			135		°C
	Threshold range	PMBus configurable OT_FAULT_LIMIT	25		146	°C
	Warning threshold	PMBus configurable		115		°C
	Response time				400	us
	Fault response	OT_FAULT_RESPONSE		Latch (0x80)		

Characteristics			Conditions	min	typ	max	Unit
Monitoring Accuracy		Input voltage READ_VIN	READ_VIN, V_I = 53 V		±0.25		V
		Output voltage READ_VOUT	READ_VOUT, V_O = 12 V		±10		mV
		Output current READ_IOUT	T_{P1} = 25°C, V_O = 12.0 V		±1		A
V_{OL}	Logic output low signal level		SCL, SDA, SYNC, SALERT, PG Sink/source current = 4 mA			0.25	V
V_{OH}	Logic output high signal level			2.7			V
I_{OL}	Logic output low sink current					4	mA
I_{OH}	Logic output high source current					4	mA
V_{IL}	Logic input low threshold		SCL, SDA, CTRL, SYNC			1.1	V
V_{IH}	Logic input high threshold			2.1			V
C_{I_PIN}	Logic pin input capacitance		SCL, SDA, CTRL, SYNC		10		pF
RC_{S_PU}	Secondary Remote Control logic pin internal pull-up resistance		SCL, SDA, SALERT		No internal pull-up		
			CTRL to +3.3V Note 8		47		kΩ
f_{SMB}	Supported SMBus Operating frequency			100		400	kHz
T_{BUF}	SMBus Bus free time		STOP bit to START bit See section SMBus – Timing		1.3		µs
t_{set}	SMBus SDA setup time from SCL		See section SMBus – Timing		100		ns
t_{hold}	SMBus SDA hold time from SCL		See section SMBus – Timing		0		ns
	SMBus START/STOP condition setup/hold time from SCL				600		ns
T_{low}	SCL low period			1.3			µs
T_{high}	SCL high period				0.6	50	µs

Note 1. There are configuration changes to consider when changing the switching frequency, see section Switching Frequency.
Note 2. A default value of 0 ms forces the device to Immediate Off behavior with TOFF_FALL ramp-down setting being ignored.
Note 3. The specified accuracy applies for off delay times larger than 4 ms. When setting 0 ms the actual delay will be 0 ms.
Note 4. According to the combination of command MFR_RESPONSE_UNIT_CFG and delay time set in IOUT_OC_FAULT_RESPONSE, see Appendix – PMBus commands.
Note 5. Note that higher OCP threshold than specified may result in damage of the module at OC fault conditions.
Note 6. For current setting see Appendix – PMBus commands
Note 7. See section Over Temperature Protection (OTP).
Note 8. If configure the CTRL pin with internal Pull-up with command MFR_MULTI_PIN_CONFIG, see Appendix – PMBus commands.
Note 9. This is the value given by single cell Power Blade. For 3 phase system, peak OCP=138A, average OCP=105A, average OCW=90A

flex

Technical Specification

BMR520 series DC-DC Converters Input 42.5-75 V, Output up to 25 A / 300 W	28701-BMR520 Rev A March 2022 © Flex

Electrical Specification
12 V, 25 A / 300 W

Blade single phase with Control Assembly

T_{P1} = -40 to +90ºC, V_I = 42.5V to 75 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25°C, V_i= 53 V_I max I_O, unless otherwise specified under Conditions.
Additional C_{in} = 100 µF E-cap+ 2x 4.7uF MLCC, C_{out} = 470 µF Oscon +4x47 uF MLCC . See Operating Information section for selection of capacitor types.

Characteristics		Conditions	min	typ	max	Unit
V_I	Input voltage range		42.5		75	V
V_{Ioff}	Turn-off input voltage	Decreasing input voltage, Note 1		40		V
V_{Ion}	Turn-on input voltage	Increasing input voltage		42		V
C_I	Internal input capacitance	V_I = 53 V		4.4		µF
P_O	Output power		0		300	W
η	Efficiency	50% of max I_O, V_I = 48 V		94.5		%
		max I_O		95		
		50% of max I_O, V_I = 53 V		93.8		
		max I_O, V_I = 53 V		94.9		
P_d	Power Dissipation	max I_O		16	23	W
P_{li}	Input idling power	I_O = 0 A, V_I = 53 V		5.5		W
P_{RC}	Input standby power	V_I = 53 V (turned off with RC)		1.2		W
f_s	Switching frequency	0-100 % of max I_O		250		kHz

V_{Oi}	Output voltage initial setting and accuracy	T_{P1} = +25°C, V_I = 53 V, I_O = 25 A	11.95	12	12.05	V
V_O	Output adjust range	See operating information	10.8		13.2	V
	Output voltage tolerance band	0-100% of max I_O	11.76		12.24	V
	Idling voltage	I_O = 0 A, V_I = 42.5-75 V		12		V
	Line regulation	V_I = 42.5-75 V, max I_O		10	20	mV
	Load regulation	V_I = 53 V, 0-100% of max I_O		10	20	mV
V_{tr}	Load transient voltage deviation	V_I = 53 V, Load step 25-75-25% of max I_O, di/dt = 2 A/µs, C_O = 2.5mF		±200	±300	mV
t_{tr}	Load transient recovery time				0.5	ms
t_r	Ramp-up time (from 10−90% of V_{Oi})	10-100% of max I_O		11		ms
t_s	Start-up time (from V_I connection to 90% of V_{Oi})			25		ms
t_{RC}	RC start-up time (from V_{RC} connection to 90% of V_{Oi})	max I_O		13		ms
RC	Sink current.	See operating information	0.5			mA
	Trigger level	Decreasing / Increasing RC-voltage		0.4/0.7		V
	Response time		0.4		1.1	ms
I_O	Output current		0		25	A
I_{lim}	Current limit threshold	T_{P1} < max T_{P1}	30	32	34	A
I_{sc}	Short circuit current	T_{P1} = 25ºC, see Note 2		/		A
C_{out}	Recommended Capacitive Load	T_{P1} = 25ºC, see Note 3	200	470	2500	µF
V_{Oac}	Output ripple & noise	See ripple & noise section, V_{Oi}		80	200	mVp-p
OVP	Over voltage protection	T_{P1} = +25°C, V_I = 53 V, 50% of max I_O		14.5		V

Note 1: when input voltage is lower than 40V, the module duty cycle saturates, idling power is much higher, the module is turned off to avoid this situation.

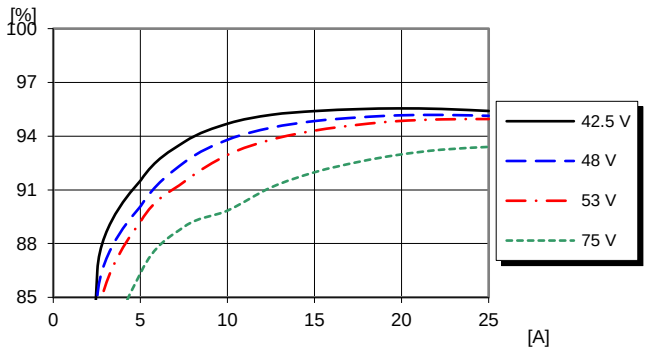
Note 2: RMS output current is the presented. OCP response is Latch mode

Note 3: Low ESR value, OSCON; Max. Capacitive Load is 7500 µF for three Power Blades

Typical Characteristics
12 V, 25 A / 300 W

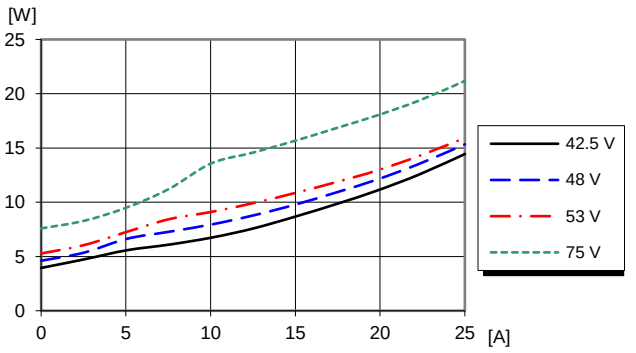
Blade single phase

Efficiency



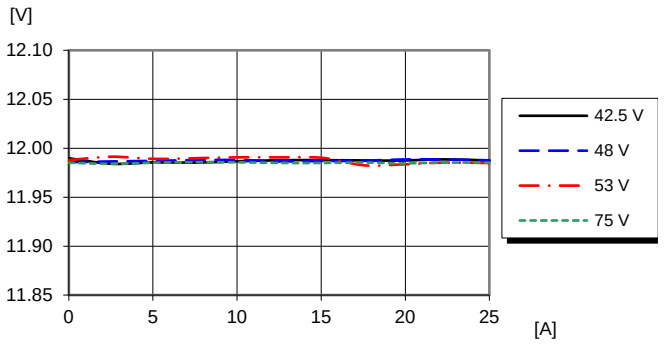
Efficiency vs. load current and input voltage at T_{P1} = +25°C.

Power Dissipation



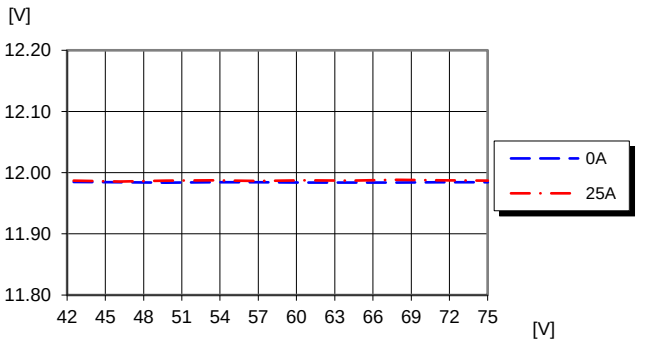
Dissipated power vs. load current and input voltage at T_{P1} = +25°C.

Output Characteristics



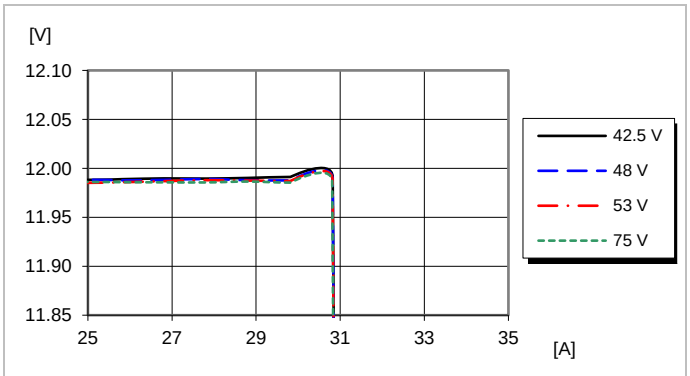
Output voltage vs. load current at T_{P1} = +25°C.

Output Characteristics



Output voltage vs. load current at I_O > max I_O, T_{P1} = +25°C.

Current Limit Characteristics



Output voltage vs. load current at I_O > max I_O, T_{P1} = +25°C.

flex

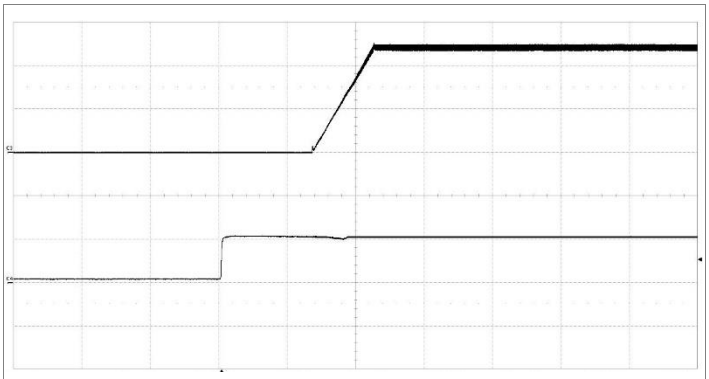
Technical Specification

BMR520 series DC-DC Converters Input 42.5-75 V, Output up to 25 A / 300 W	28701-BMR520 Rev A March 2022
	© Flex

Typical Characteristics
12 V, 25 A / 300 W

Blade single phase

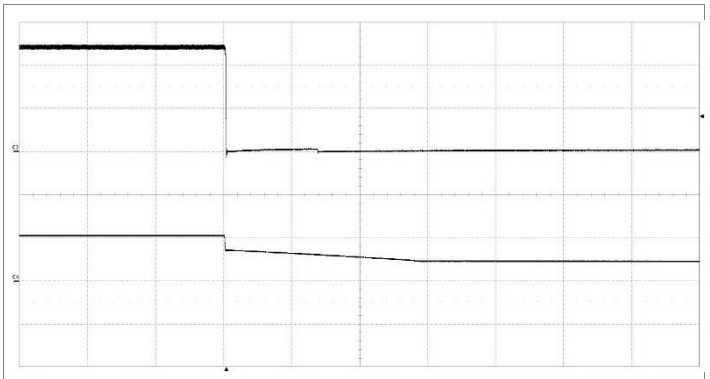
Start-up



Start-up enabled by connecting V_I at:
T_{P1} = +25°C, V_I = 53 V,
I_O = 25 A load.(E-load)

Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (50 V/div.).
Time scale: (10 ms/div.).

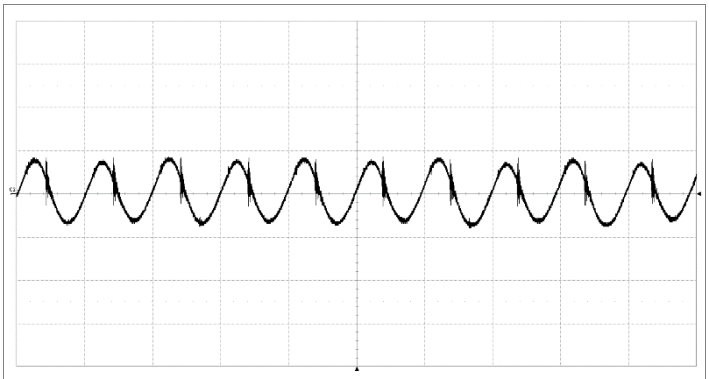
Shut-down



Shut-down enabled by disconnecting V_I at:
T_{P1} = +25°C, V_I = 53 V,
I_O = 25 A load.(E-load)

Top trace: output voltage (5 V/div.).
Bottom trace: input voltage (50 V/div.).
Time scale: (20 ms/div.).

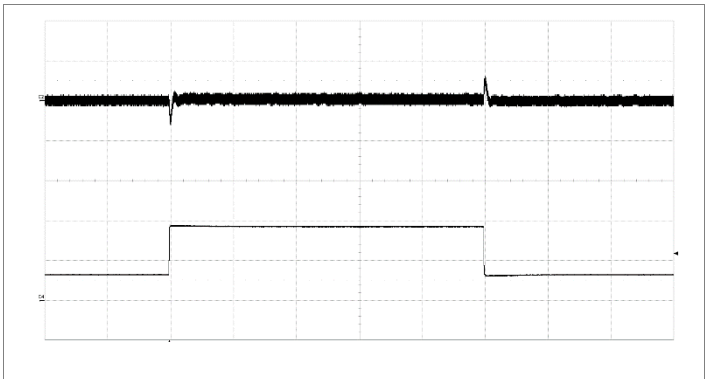
Output Ripple & Noise



Output voltage ripple at:
T_{P1} = +25°C, V_I = 53 V,
I_O = 25 A load.(E-load)

Trace: output voltage (50 mV/div.).
Time scale: (2 µs/div.).
Cout=470uF OSCON+4x47uF MLCC

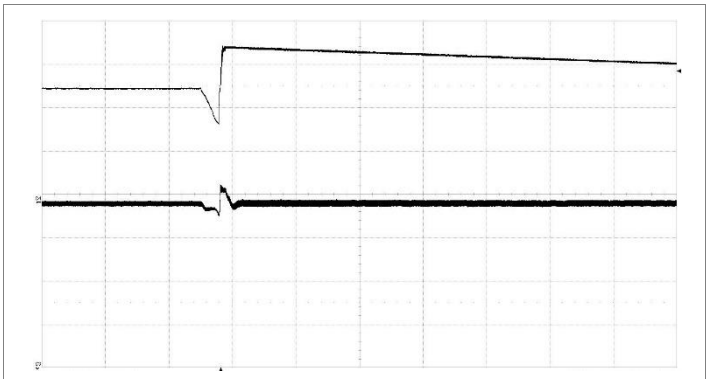
Output Load Transient Response



Output voltage response to load current step-change (6.25 – 18.75 – 6.25 A) at:
T_{P1} =+25°C, V_I = 53 V.
Cout=470uF OSCON+4x47uF MLCC

Top trace: Output voltage (0.5 V/div.).
Bottom trace: Output current (10 A/div.).
Time scale: (1 ms/div.).

Input Voltage Transient Response



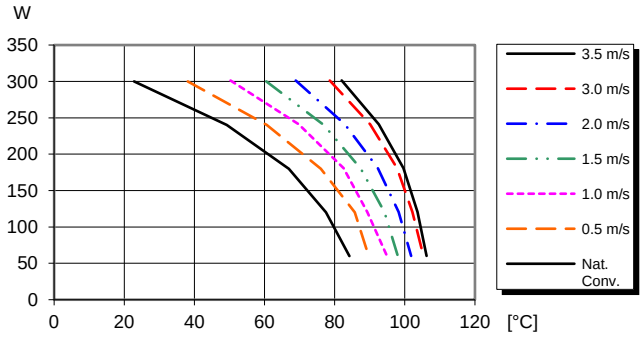
Output voltage response to input voltage transient at: T_{P1}= +25°C, V_I = 42-75 V,
slew rate = 0.1V/µs, I_O = 25 A, C_O = 1.94 mF

Top trace: input voltage (20 V/div.).
Bottom trace: output voltage (2 V/div.).
Time scale: (1 ms/div.).

Typical Characteristics
12 V, 25 A / 300 W

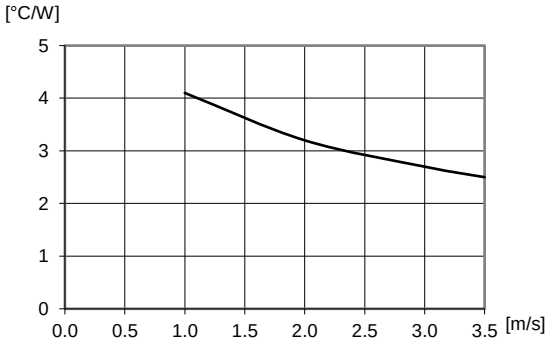
Blade single phase

Output Current Derating – Base Plate & Heat Sink



Available load current vs. ambient air temperature and airflow at V_I = 48 V. See Thermal Consideration section.

Thermal Resistance – Base Plate & Heat Sink

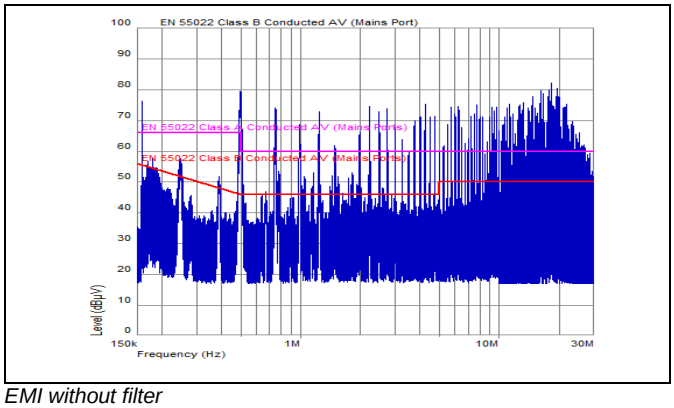


Thermal resistance vs. airspeed measured at the converter. Tested in wind tunnel with airflow and test conditions as per the Thermal consideration section. V_I = 48 V.Io=25A

EMC Specification

Conducted EMI measured according to EN55022, CISPR 22 and FCC part 15J (see test set-up). See Design Note 029 for further information. The fundamental switching frequency is 250 kHz for BMR520. The EMI characteristics below is measured at V_I = 53 V and max I_O.

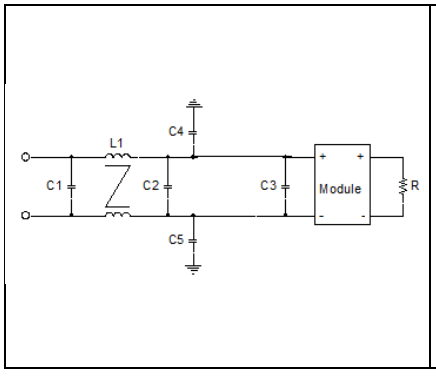
Conducted EMI Input terminal value (typ)



EMI without filter

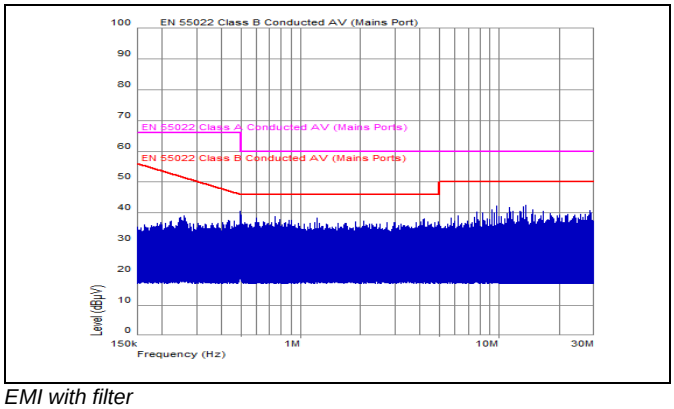
Optional external filter for class B

Suggested external input filter in order to meet class B in EN 55022, CISPR 22 and FCC part 15J.

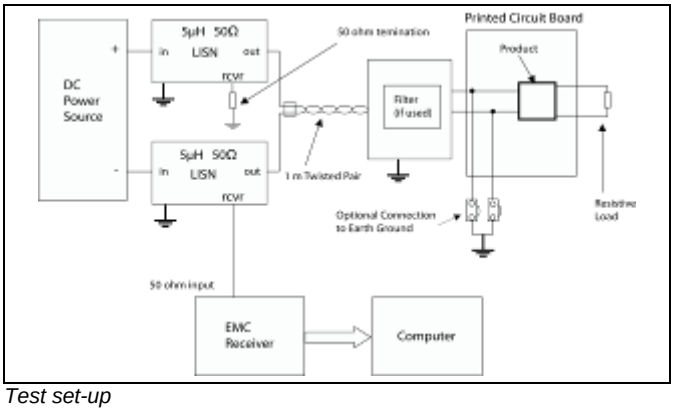


Filter components:
C1 = 2x2.2 µF
C2 = 2x2.2 µF
C3 = 2x4.7 µF + 220 µF (e-lyt)
C4, C5 = 22 nF
L1 = 0.81 mH (P0429)

Note: a ferrite core added on input cable to get ~1.4uH CM chock



EMI with filter



Test set-up

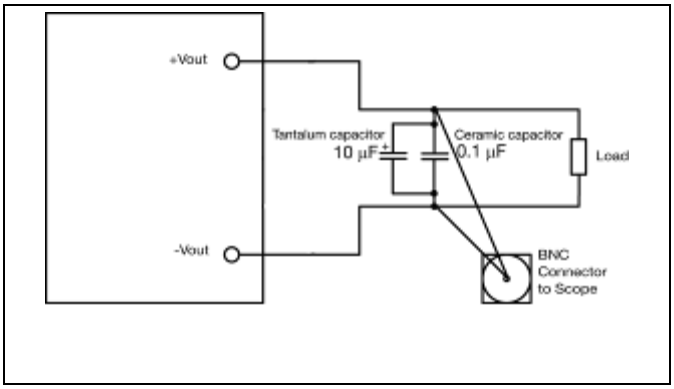
Layout recommendations

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and to the equipment ground or chassis.

A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

Output ripple and noise

Output ripple and noise is measured according to figure below. See Design Note 022 for detailed information.



Output ripple and noise test setup

Power Management Overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin. The following product parameters can continuously be monitored by a host: Input voltage, output voltage/current, and internal temperature.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface

Throughout this document, different PMBus commands are referenced. A detailed description of each command is provided in the appendix at the end of this specification.

The Flex Power Designer software suite can be used to configure and monitor this product via the PMBus interface. For more information please contact your local Flex sales representative.

SMBus Interface

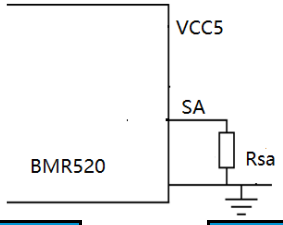
This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire I²C (master must allow for clock stretching) or SMBus host device. In addition, the product is compatible with PMBus version 1.3 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports 100 kHz and 400 kHz bus clock frequency only. The PMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors are required to guarantee the rise time as follows:

Eq. 7 $$\tau = R_P C_p \leq 1us$$

where R_p is the pull-up resistor value and C_p is the bus load. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply between 2.7 to 3.8 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.

PMBus Addressing

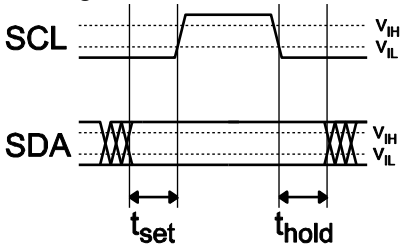
The PMBus address is configured with a resistor, R_{SA}, connected between the SA pin and GND, as shown in the Typical Application Circuit. Recommended resistor values are shown in the table below. 1% tolerance resistors are required



R_{SA} [kΩ]	Address
10.5	0x60
12	0x61
14	0x62
15.4	0x64
18	0x68
20.5	0x69
24	0x6A
27	0x6C

R_{SA} [kΩ]	Address
33	0x70
39	0x71
47	0x72
62	0x74
82	0x58
120	0x59
220	0x5A
Infinite (open)	0x5C

I²C/SMBus – Timing



Setup and hold times timing diagram

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the falling edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. Refer to the SMBus 2.0 specification, for SMBus electrical and timing requirements.

This product supports the BUSY flag in the status commands to indicate product being too busy for SMBus response. A bus-free time delay according to this specification must occur between every SMBus transmission (between every stop & start condition).
The product supports PEC (Packet Error Checking) according to the SMBus specification.

After sending commands that involve writing to the NVM a delay according to the table below is required before V_{CTRL} is powered off. If sending a subsequent command the user may insert these delays or the BUSY flag in STATUS_BYTE can be polled to detect when the device is ready to receive a new

command.

After sending PMBus command	Required delay before additional command
STORE_DEFAULT_ALL	100 ms
MFR_STORE_MAP	
MFR_SECT_WR	20ms

Monitoring via PMBus
It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus Command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Output current	READ_IOUT
Temperature	READ_TEMPERATURE

Monitoring Faults
Fault conditions can be detected using the SALERT pin, which will be asserted low when any number of pre-configured fault or warning conditions occurs. The SALERT pin will be held low until faults and/or warnings are cleared by the CLEAR_FAULTS command, or until the output voltage has been re-enabled. It is possible to mask which fault conditions should not assert the SALERT pin by the command SMBALERT_MASK. In response to the SALERT signal, the user may read a number of status commands to find out what fault or warning condition occurred, see table below.

Fault & Warning Status	PMBus Command
Overview, Power Good	STATUS_BYTE STAUS_WORD
Output voltage level	STATUS_VOUT
Output current level	STATUS _IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

Memory Structure
The product incorporates a Non-Volatile Memory area for storage of PMBus command and System register values. The NVM is pre-loaded with Flex factory default values. The values in NVM are loaded during initialization according to section Initialization Procedure, where after commands can be changed through the PMBus Interface.

The STORE_DEFAULT _ALL command will store the changed PMBus command values to the NVM, while the MFR_STORE_MAP command will store both PMBus command values and System register values to the NVM.

When sending any of these two store commands, the CRC code in NVM is automatically recalculated and updated. Commands RESTORE_DEFAULT_ALL and MFR_RESTORE_MAP transfer data in the opposite direction, from NVM to RAM.

NVM memory cells are qualified for 1000 read/erase/write cycles and 10 years data retention at 125 °C.

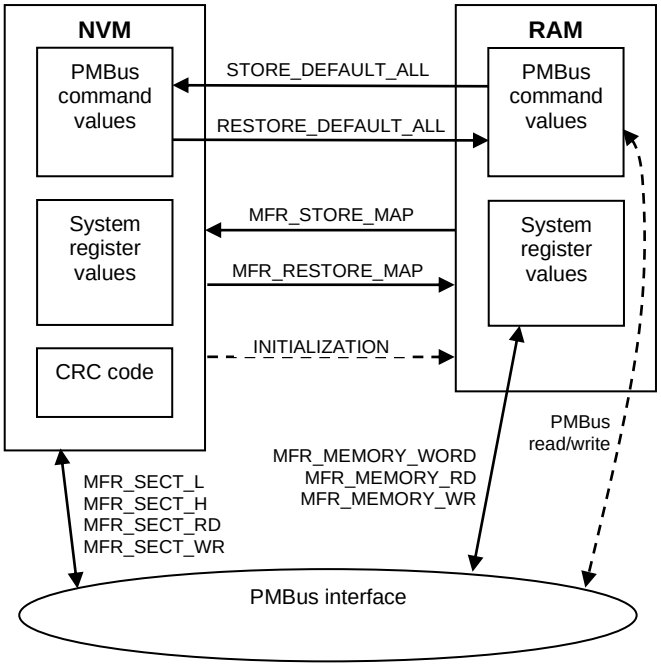


Illustration of memory areas of the product and associated PMBus commands.

In general, Vin must be cycled before a change in a System Register have an effect (thus, storing to NVM is required), while changes to PMBus commands will have immediate effect once written to RAM.

Parameter Protection
Several possibilities are provided to protect configuration parameters in the NVM and RAM:

PMBus Command	Function
WRITE_PROTECT	Control of PMBus command writes in general.
MFR_WRITE_LOCK	
MFR_UNLOCK	Control of System register reads/writes, as well as reads/writes of critical PMBus commands.
MFR_LOCK	

MFR_SVID_REGLOCK	Control of PMBus command and System register writes related to SVID/AVS CPU-link registers.
MFR_PROTECT_DEFAULT	Control of NVM writes.

Initialization Procedure
The product follows an internal initialization procedure after the supply voltage becomes larger than the UVLO threshold:

1. Startup and initialization.
2. The address pin-strap resistor is measured and the associated PMBus address is defined. If a non-valid pin-strap resistor value is used, power conversion will be prohibited, and the device is set to respond to PMBus address 0x7C.
3. Flex factory default values stored in the NVM memory are loaded to operational RAM.
4. A CRC check is performed over memory content and compared with CRC code in NVM. If an error is detected, power conversion is prohibited and STATUS_CML[4] (Memory fault detected) is set and the device is set to respond to PMBus address 0x7C. Thus, the address setting by SADDR pin is ignored.
5. Self-calibration is performed to cancel out offsets in output voltage and output current readings.

Once this procedure is completed and the Initialization Time, T_{INIT}, has passed (see Electrical Specification), the output voltage is ready to be enabled using the EN pin. The product is also ready to accept commands via the PMBus interface, which in case of writes will overwrite any values loaded during the initialization procedure.

Operating Information

Product Overview

The product provides a compact and scalable IBC solution, operate up to 3 phases, it is flexible to expand power by adding power blade, and the sandwich baseplate/heatsink design provide good thermal performance.

Input Voltage
The product is designed for 42.5 to 75 Vdc input voltage range, which meets the requirements of the European Telecom Standard ETS 300 132-2 for normal input voltage range in –48 and -60 Vdc systems, and -50 to -72 V respectively.

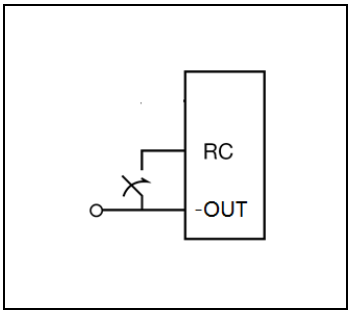
At input voltages exceeding 75 V, the power loss will be higher than at normal input voltage and T_{P1} must be limited to absolute max +125°C.

Above 42.5 V the product operates with normal regulation with constant output voltage and constant maximum power. The product operates down below 40 V will trig the internal under voltage lock out and turns off the product.

Short duration transient disturbances can occur on the DC distribution and input of the product when a short circuit fault occurs on the equipment side of a protective device (fuse or circuit breaker). The voltage level, duration and energy of the disturbance are dependent on the particular DC distribution network characteristics and can be sufficient to damage the product unless measures are taken to suppress or absorb this energy. The transient voltage can be limited by capacitors and other energy absorbing devices like Zener diodes connected across the positive and negative input conductors at a number of strategic points in the distribution network. The end-user must secure that the transient voltage will not exceed the value stated in the Absolute maximum ratings. ETSI TR 100 283 examines the parameters of DC distribution networks and provides guidelines for controlling the transient and reduce its harmful effect.

Turn-off Input Voltage
The product monitors the input voltage and will turn on and turn off at configured thresholds (see Electrical Specification). The turn-on input voltage threshold is set higher than the corresponding turn-off threshold. The minimum hysteresis between turn on and turn off input voltage is 2V.

Remote Control (RC)



The products are fitted with a remote control function referenced to the 2nd side negative input connection (-OUT), with positive logic options available. The RC function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch.

The RC pin has an internal pull up resistor of 10 kΩ to +5V. The external device must provide a minimum required sink current to guarantee a voltage not higher than maximum voltage on the RC pin (see Electrical characteristics table). When the RC pin is left open, the voltage generated on the RC pin is 5 V.

The standard product is configured with “positive logic” RC. To turn off the product the RC pin should be connected to -OUT. In situations where it is desired to have the product to power up automatically without the need for control signals or a switch, the RC pin can be left OPEN.

The RC function incorporates a short delay in order to not trigger on glitches. This setup reduces the risk that the noise may cause the converter to shut down or power up accidently.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. The products are designed for stable operation with a minimum of 100 uF external capacitors connected to the input. The electrolytic capacitors will be degraded in low temperature and the ESR value may increase. The needed input capacitance in low temperature should be equivalent to 100 uF at 20° C. This means that the input capacitor value may need to be substantially larger to guarantee a stable input at low temperatures. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors. The minimum required capacitance value depends on the output power and the input voltage. The higher output power the higher input capacitance is needed.

External Input Capacitors
It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage at large load transients.

It is recommended to use at least 100uF electrolytic bulk capacitors and 2 x 4.7 uF ceramic external input capacitors for each power blade, placed closed to input pins and with low impedance connections to the VIN and GND pins in order to be effective. See application note AN323 for further guidelines on how to choose and apply input capacitors.

External Output Capacitors
The output capacitor requirement depends on two considerations; output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to minimize output voltage deviation. Improved transient response can also be achieved by adjusting the settings of the control loop of the product. Adding output capacitance decreases loop band-width.

It is recommended to place low ESR ceramic and low ESR oscon/polymer capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts in order for capacitance to be effective.

Control Loop
The controller features a high performance digital control loop. During operation, the output voltage is sensed differentially and the error in the regulation is digitized by a fast analog-to-digital converter (ADC). The resultant digital error signal is fed into an oversampled (40 MHz) digital PID compensator and then processed by digital control and converted into PWM pulses using a digital pulse width modulator (DPWM). The pulse scheme is Constant On-time (COT) with variable frequency. Thus, the PWM pulses has a fixed on time while switching frequency (and consequently duty cycle) will depend on operating conditions such as input voltage, output voltage and load levels.

By default the product is configured with robust PID coefficients to provide stability for a wide range of operating conditions and output filters. Where specific load transient response requirements exists Flex Power Designer should be used to simulate and find optimized control loop settings

Enabling Output Voltage
The following options are available to enable and disable the output voltage:

1. Through the EN pin. Only active high logic is supported.
2. By using the PMBus command OPERATION.

The EN pin has an internal 10 kΩ pull-up resistor to 5 V. The external device must have a sufficient sink current ability to be able pull EN pin voltage down below logic low threshold level (see Electrical Characteristics).

Output Voltage Adjust
With PMBus interface the output voltage level is controlled by PMBus command VOUT_COMMAND.

Voltage Margining Up/Down
Using the PMBus interface it is possible to adjust the output voltage predefined levels above or below the nominal voltage setting in order to determine whether the load device is capable of operating outside its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit outside its typical operating range. This functionality can also be used to test of supply voltage supervisors. Margin limits of the nominal output voltage ±5% are default, but the margin limits can be reconfigured using the PMBus commands VOUT_MARGIN_LOW and VOUT_MARGIN_HIGH. Margining is activated by the command OPERATION and can be used regardless of the output voltage being enabled by the EN pin or by the PMBus.

Output Voltage Range Limitation
The output voltage range that is possible to set by the PMBus interface, and is limited by the PMBus command VOUT_MAX. The limitation applies to the actual regulated output voltage rather than to the configured value. Thus, it is possible to write and read back a VOUT_COMMAND value higher than the limit, but the actual output voltage will be limited.

Power Good
The PG pin indicates when the product is ready to provide regulated output voltage to the load. During ramp-up and during a fault condition when the output voltage has shutdown, PG is held low. PG is asserted high after the output has completed ramping to the set voltage level and de-asserted low when the output voltage is controlled to off. Thus, de-

assertion is not controlled by the voltage level.

The PG output is held low during the initialization procedure

Output Under Voltage Protection (UVP)

The product includes under voltage limiting circuitry. The threshold is set as a negative offset to the commanded output voltage level (see Electrical Specification). The product can be configured to respond in different ways when the UVP limit is passed:

1. immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.

The default response is option 1. The UVP limit and fault response are configured using the PMBus commands MFR_UV_LIMIT_OFFSET and VOUT_UV_FAULT_RESPONSE

Output Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The threshold is set as a positive offset, to the commanded output voltage level (see Electrical Specification). The product can be configured to respond in different ways when the OVP limit is exceeded, see below options.

1. immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch
2. Ignore fault and continue operation.

The default response is option 1. The OVP limit and fault response are configured using the PMBus commands MFR_OV_LIMIT_OFFSET and VOUT_OV_FAULT_RESPONSE

Over Current Protection (OCP)

The product includes robust current limiting circuitry for protection at overload. The OCP function has two parts; a fast peak detection and a detection that works on average current. In both cases the protection applies to the total output current of all phases in the rail.

The peak protection is always enabled with a latched response, while for the average current protection different response options are available:

1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.

The default response from an over current fault is option 1.

The average OCP warning and fault limits are configured using the commands IOUT_OC_WARN_LIMIT and IOUT_OC_FAULT_LIMIT. The response options are set by IOUT_OC_FAULT_RESPONSE.

Soft-on

The soft-on functionality allows the output voltage to ramp-up with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple loads.

The rise time is the time taken for the output to ramp to its target voltage. The on delay time sets a delay from when the output is enabled until the output voltage starts to ramp up

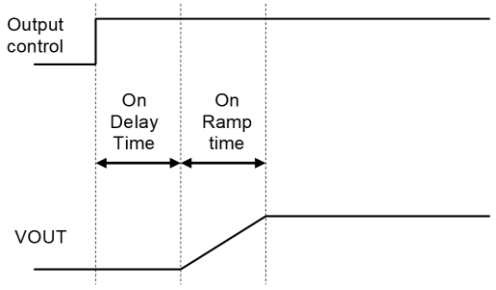


Illustration of soft-on.

The on delay time is reconfigured using the PMBus command TON_DELAY, while the on ramp time is reconfigured by setting a slew rate by PMBus command MFR_SVID_SLOW_SR_SELECTOR together with System Register DVID_SR_SLOW_STEP.

Soft-off

When enabled, the soft-off functionality makes the output voltage to ramp down with a defined slew rate, after output voltage being turned off. In order to prevent a reverse current through the power train, which may cause excessive voltage across switching elements, the regulator will ramp down to a voltage of ~0.25 V and keep this level for a few ms, before finally turn switching completely off.

The time after output control is turned off until voltage starts to ramp down is not reconfigurable.

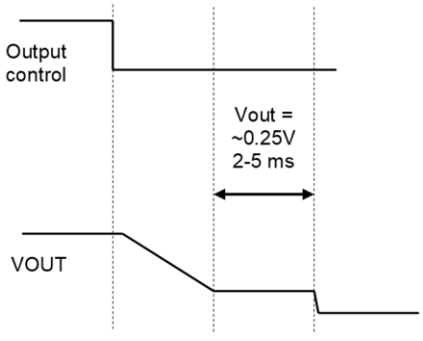


Illustration of soft-off.

By default soft-off is enabled. The slew rate of the ramp is set by PMBus command MFR_SVID_SLOW_SR_SELECTOR together with System Register DVID_SR_SLOW_STEP.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-

supply logic component, such as FPGAs or ASICs. There could also be still charged output capacitors when starting up shortly after turn-off.
The product incorporates synchronous rectifiers, but will not sink current during startup.

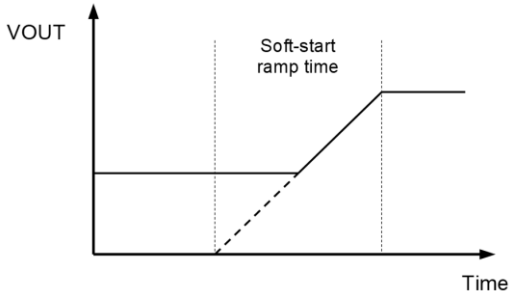


Illustration of pre-bias startup.

Switching Frequency
The switching frequency is configured to 250KHz, recommend don't modify the value because it relates to power train design.

Multiphase Operation (Current Sharing)
Up to three power blades can be connected to control assembly, to increase the output current capability. All power blades are managed by the control assembly, that provides a common interface for control and telemetry as a single rail.

Active current sharing balancing can be activated by the PMBus command MFR_CS_PROP_INTEGR. The control assembly will actively control the output current of each power blade, based on the monitored output current from each power blade, to achieve balance between all phases. This function can correct for unit and layout differences and increase the thermal performance of a multiphase rail.

Phase Interleaving
When operating the product in a multiphase setup, the control assembly will automatically spread the phases evenly in time, based on the number of active phases at the moment, in order to minimize the input and voltage ripple.

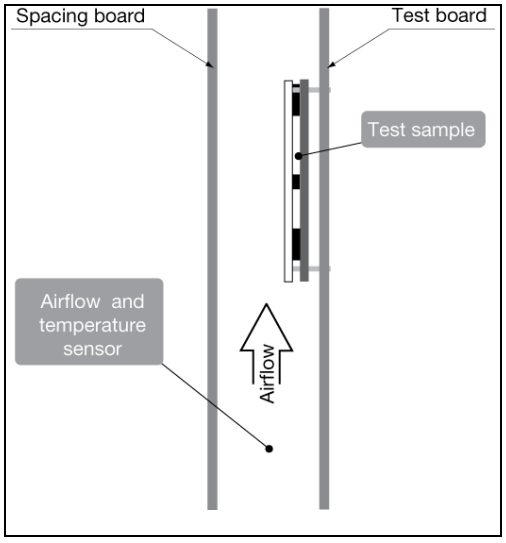
Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Electrical Specification Output section for each module provides the available output current versus ambient air temperature and air velocity at specified V_I.

The product is tested on a 254 x 254 mm test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 16 layers with average 35 µm (1 oz) copper thickness.



Note that the cooling via power pins does not only have to handle the power loss from the module. A low resistance between module and target device is of major importance to reduce additional power loss.

See Design Note 019 for further information.

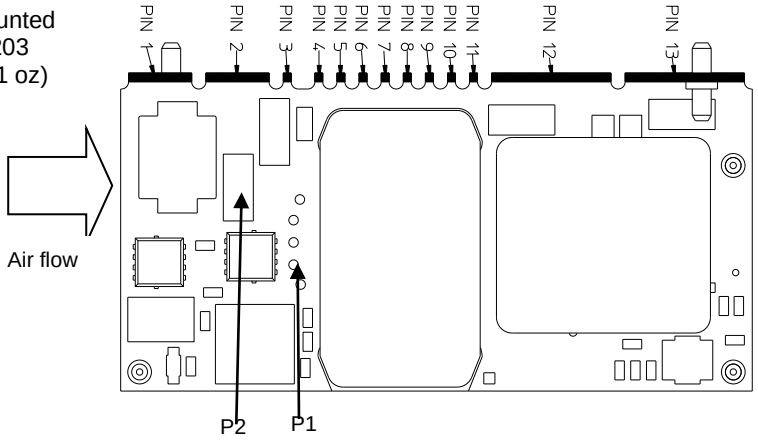
Definition of Product Operating Temperature

The temperature at position P1, P2 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperature above specified maximum measured at the specified position is not allowed and may cause permanent damage. (P1 and P2 are only accessible for internal test. For further technical support, please contact local Flex sales.)

Position	Description	Max Temperature
P1	PCB, Transformer winding	T_{P1} = 125°C
P2	input MLCC cap	T_{P2} = 120°C

Note that the maximum value is the maximum operating temperature and that the provided Electrical Specification data is guaranteed up to T_{P1} = +95°C.

Perspective drawing from baseplate



Air Flow Direction

The result from thermal test shows the air flow direction from input pin to output pin for best thermal performance. Showed as above picture.

Over Temperature Protection (OTP)

The product is protected from thermal overload by an internal over temperature shutdown function circuit, monitoring the temperature of the transformer winding PCB.

The temperature is continuously monitored and when the temperature rises above the configured fault threshold level the product will respond as configured. The product can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled (latch).
2. Ignore fault and continue operation.

Default response is option 1. The default OTP limit is specified in Electrical Characteristics.

The OTP fault and warning limits and response are configured using the PMBus commands OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE.

Ambient Temperature Calculation
For products with base plate/heatsink the maximum allowed ambient temperature can be calculated by using the thermal resistance.

1. The power loss is calculated by using the formula ((1/η) - 1) × output power = power losses (Pd).
η = efficiency of product. E.g. 95.5% = 0.955

2. Find the thermal resistance (Rth) in the Thermal Resistance graph found in the Output section for each model.

Calculate the temperature increase (ΔT).
ΔT = Rth x Pd

3. Max allowed ambient temperature is:
Max T_{P1} - ΔT.

E.g. BMR520 at 2m/s:

η=0.946 Rth=3.2°C/W

1. $((\frac{1}{0.945}) - 1) \times 300\ W = 17.46\ W$

2. 17.46W × 3.2°C/W = 56°C

3. 125 °C – 56°C = max ambient temperature is 69°C

The actual temperature will be dependent on several factors such as the PWB size, number of layers and direction of airflow.

PCB Layout Consideration

The radiated EMI performance of the product will depend on the PCB layout and ground layer design. A ground plane shall be used, to increase the stray capacitance in the PCB and improve the high frequency EMC performance. The ground plane shall connect to the GND pins of the devices and the equipment ground or chassis.

Further layout recommendations are listed below.

1. For a multiphase rail layout should be as symmetrical as possible in order to give a good current balance between devices.
2. If possible use planes on several layers to carry V_I, V_O and ground. There should be a large number of vias close to the -IN, +IN, VOUT and GND pins in order to lower input and output impedances and improve heat spreading between the product and the host board.
3. The address pin strap resistor R_{SADDR} should be placed as close to the product as possible to minimize loops that may pick up noise. Avoid capacitive load on these signals as it may result in false pin strap reading. Also avoid current carrying planes under the pin strap resistor.
4. The external input capacitors, C_{I_EXT}, shall be placed as close to the input pins as possible and with low impedance connections, e.g. using via stitching around capacitors' terminals. See AN323 for more details.
5. The external output capacitors, C_{O_EXT}, should in general be placed close to the load. However typically you would like to place larger ceramic output capacitors close to the regulator module output in order to handle the output ripple current. See AN321 for more details. Low impedance connections must be used, e.g. via stitching around capacitors' terminals.
6. Care should be taken in the routing the following connections:

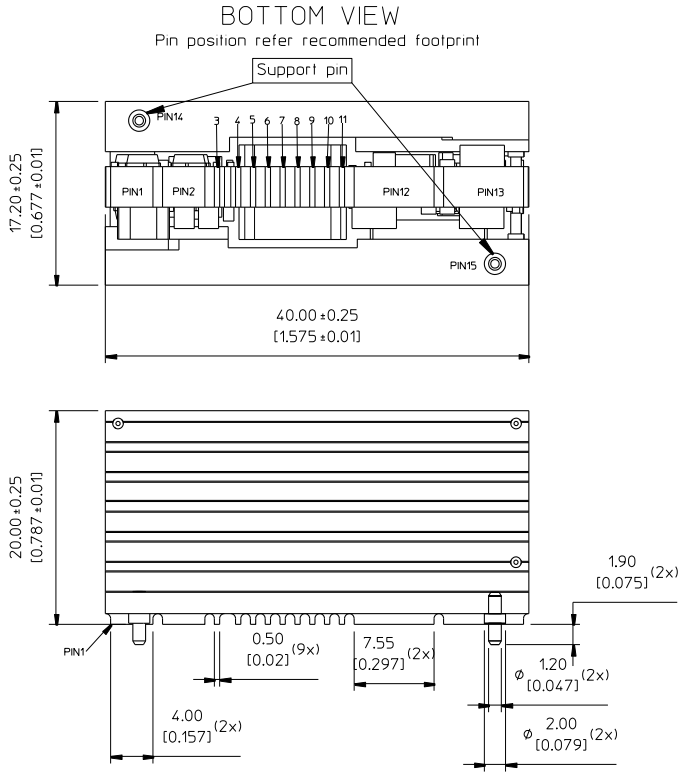
   VOUT sense line from power blade output to control assembly Vout pin.

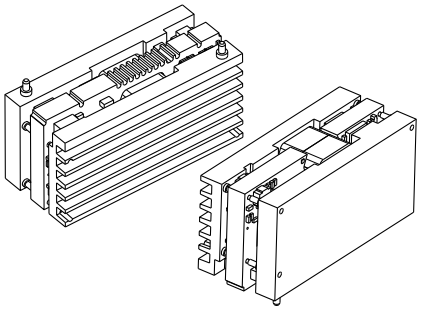
   Current sense line IO_SENSEx from each power blade to control assembly IO_SENSEx

   Temperature sense line TMx from each power blade to control assembly TMx.

   These sensing connections preferably shielded between ground planes which are not carrying high currents, to reduce noise susceptibility. The routing should avoid areas of switching signals or high electric or magnetic fields, e.g. keep away from PWMxX, PWMxY and STARTx signals.

Mechanical Information – Power Board





Case
Material: Aluminium

Pins
Pin 1 ~ 13 Material: ENIG
Plating: Min Au 0.05 µm over 3-8 µm Ni

Pin 14 & 15 Material: Brass alloy
Plating: Min Au 0.1 µm over 1-3 µm Ni

Recommended keep away area for user components to withstand input to output isolation voltage according to absolute maximum ratings.

Footprint
Recommended hole dimensions are only for reference. It's end users' decison based on different situations like productions process, substrate thickness, etc

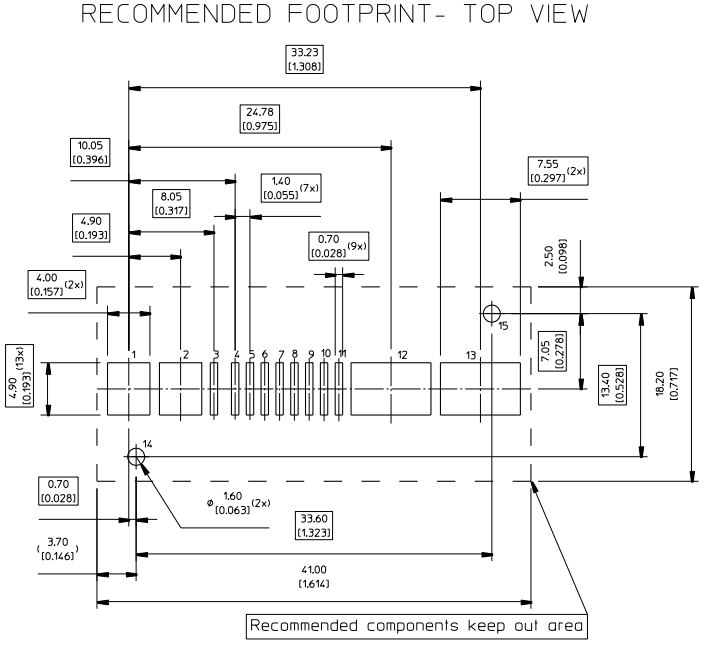
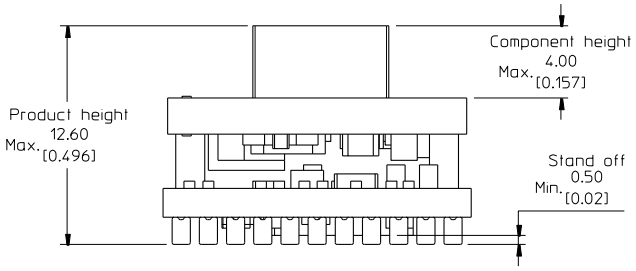


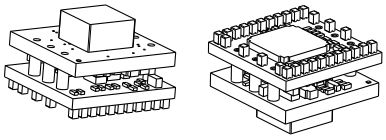
Table 1

PIN #	Function
1	VIN+
2	VIN-
3	VP
4	PWMX
5	PWMY
6	VCC5
7	VCC1V8
8	VS
9	Io_SENSE
10	START
11	TM
12	GND
13	Vo+
14	NC
15	NC

Weight:typical 37 g
All dimensions in mm [inch].
Tolerances unless specified
x.x mm ±0.50 mm [0.02], x.xx mm ±0.25 mm [0.01]
(not applied on footprint or typical values)

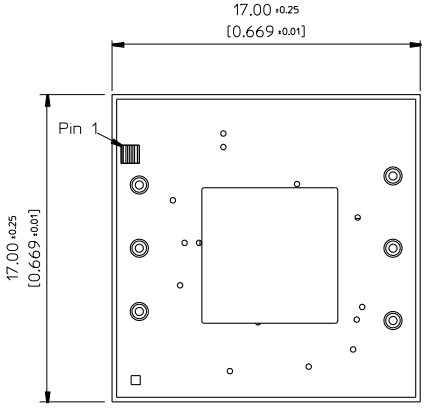
Mechanical Information – Controller Board





TOP VIEW

Pin positon refer recommended footprint



RECOMMENDED FOOTPTINT - TOP VIEW

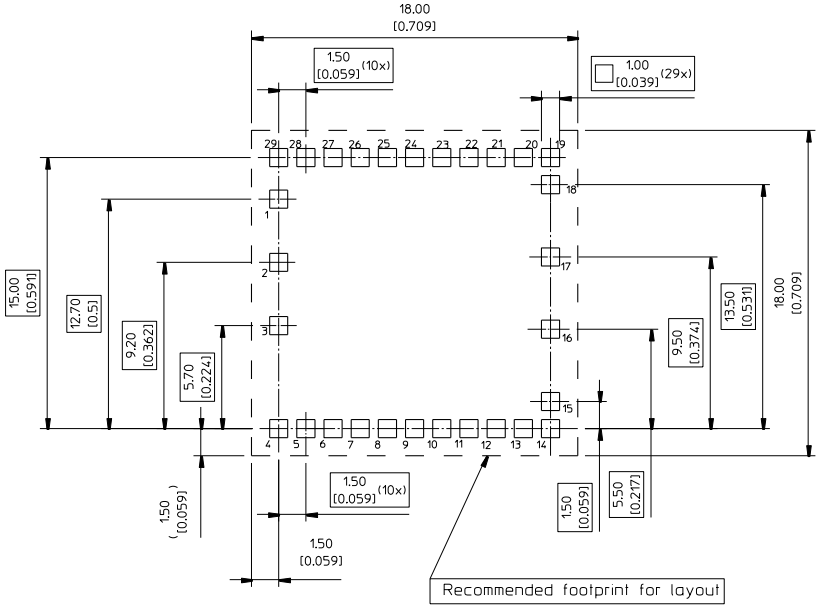


Table 1

PIN #	Function
1	VIN+
2	VP
3	VIN-
4	Io_SENSE3
5	Io_SENSE2
6	Io_SENSE1
7	PG
8	EN
9	SA
10	SCL
11	SDA
12	SALERT
13	VOUT
14	START3
15	START2
16	VS
17	GND
18	START1
19	PWM3Y
20	PWM3X
21	PWM2Y
22	PWM2X
23	PWM1Y
24	PWM1X
25	VCC5
26	VCC1V8
27	TM3
28	TM2
29	TM1

Pins
Material: Copper alloy
Plating: min 0.1 µm Au over 2 µm Ni

Recommended keep away area for user components to withstand input to output isolation voltage according to absolute maximum ratings.

Footprint
Recommended pad dimensions are only for reference. It's end users' decison based on different situations like productions process, substrate thickness, etc

Weight: typical 4.6g
All dimensions in mm [inch].
Tolerances unless specified
x.x mm ±0.50 mm [0.02], x.xx mm ±0.25 mm [0.01]
(not applied on footprint or typical values)

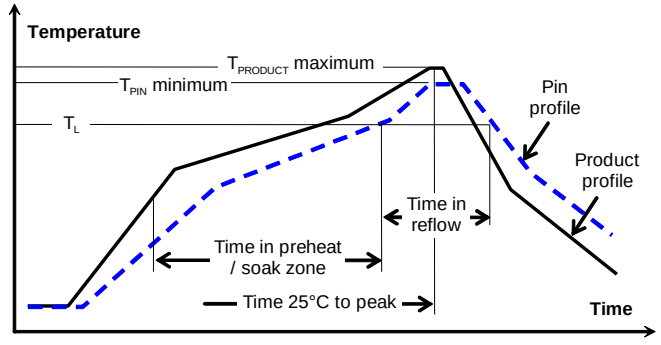
Soldering Information - Surface Mounting (Power Blade)

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PWB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up ($T_{PRODUCT}$)		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above T_L		60 s	60 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	$T_{PRODUCT}$	225°C	260°C
Average ramp-down ($T_{PRODUCT}$)		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Pin number 13 is chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L, 183°C for Sn63Pb37) for more than 60 seconds and a peak temperature of 220°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L, 217 to 221°C for SnAgCu solder alloys) for more than 60 seconds and a peak temperature of 245°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

PWB near pin 7 is chosen as reference location for the maximum (peak) allowed product temperature ($T_{PRODUCT}$) since this will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

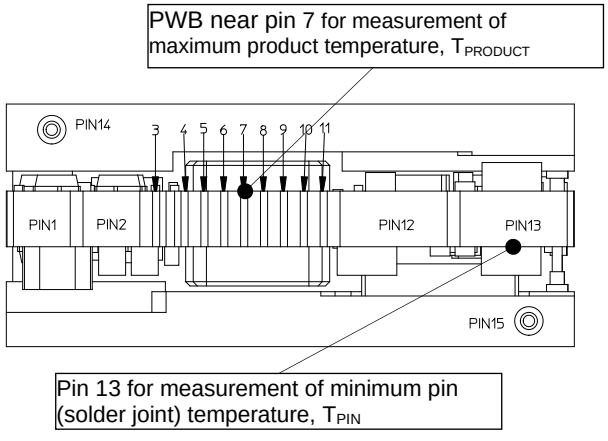
During reflow $T_{PRODUCT}$ must not exceed 260 °C at any time.

Dry Pack Information

Surface mount versions of the products are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033 (If the vacuum package is found broken, please bake the product for minimum 24 hrs at 125°C.)

Thermocoupler Attachment

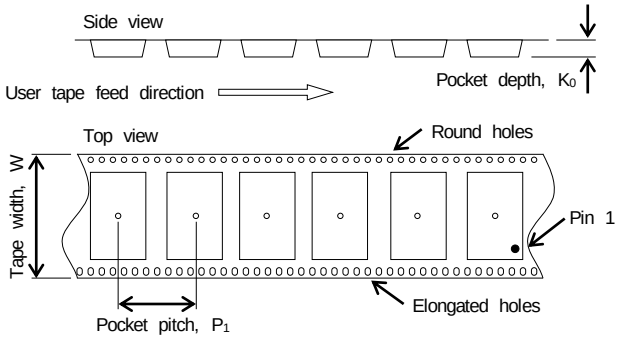


Surface Mount Assembly (Power Blade)

Automatic pick and place equipment should be used to mount the product on the host board. The use of a vision system, utilizing the fiducials on the bottom side of the product, will ensure adequate accuracy. Manual mounting of products is not recommended.

This module is **not** recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

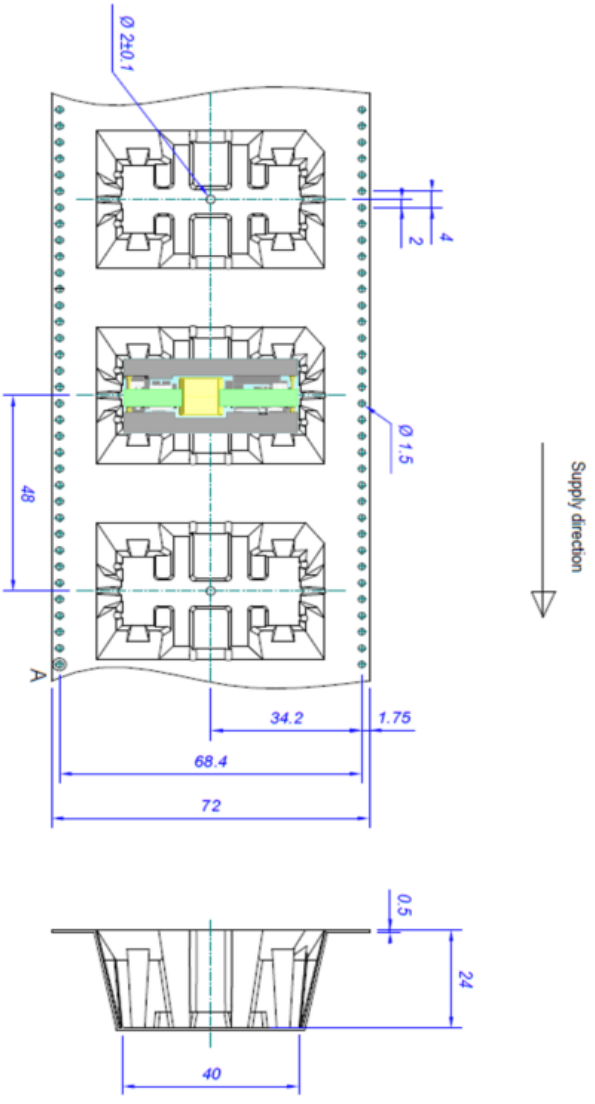
EIA standard carrier tape



Delivery Package Information

The products are delivered in antistatic carrier tape (EIA 481 standard).

Carrier Tape Specifications	
Material	Transparent PET
Surface resistance	< 10^{11} Ohm/square
Bakeability	The tape is not bakable
Tape width, W	72 mm [2.83 inch]
Pocket pitch, P_1	48 mm [1.89 inch]
Pocket depth, K_0	24 mm [0.945 inch]
Reel diameter	330 mm [13 inch]
Reel capacity	40 products /reel
Reel weight	2 kg/full reel
Box capacity	80 products (2 reels/box)



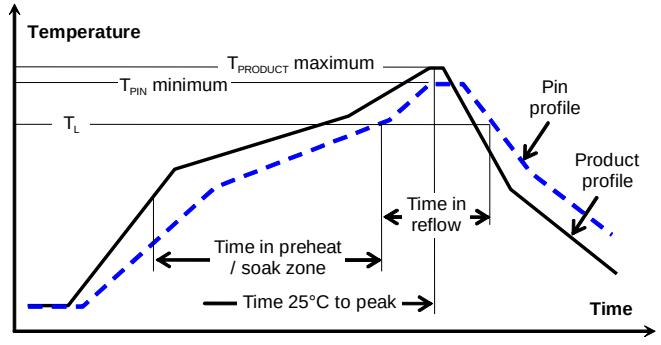
Soldering Information - Surface Mounting (Controller Assembly)

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PWB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up ($T_{PRODUCT}$)		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above T_L		60 s	60 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	$T_{PRODUCT}$	225°C	260°C
Average ramp-down ($T_{PRODUCT}$)		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Pin number 3 or 16 is chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L, 183°C for Sn63Pb37) for more than 60 seconds and a peak temperature of 220°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L, 217 to 221°C for SnAgCu solder alloys) for more than 60 seconds and a peak temperature of 245°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

PWB near pin 24 is chosen as reference location for the maximum (peak) allowed product temperature ($T_{PRODUCT}$) since this will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 260 °C at any time.

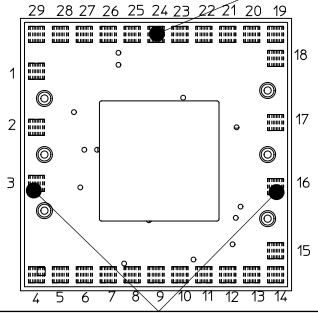
Dry Pack Information

Surface mount versions of the products are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033 (If the vacuum package is found broken, please bake the product for minimum 24 hrs at 125°C.)

Thermocoupler Attachment

PWB near pin 24 for measurement of maximum product temperature, $T_{PRODUCT}$



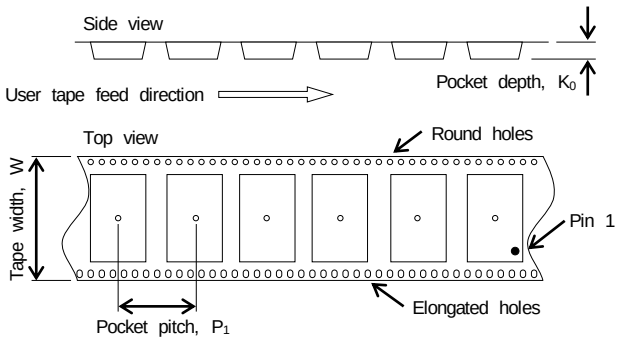
Pin 3 or 16 for measurement of minimum pin (solder joint) temperature, T_{PIN}

Surface Mount Assembly (Controller Assembly)

Automatic pick and place equipment should be used to mount the product on the host board. The use of a vision system, utilizing the fiducials on the bottom side of the product, will ensure adequate accuracy. Manual mounting of products is not recommended.

This module is **not** recommended for assembly on the bottom side of a customer board. If such an assembly is attempted, components may fall off the module during the second reflow process.

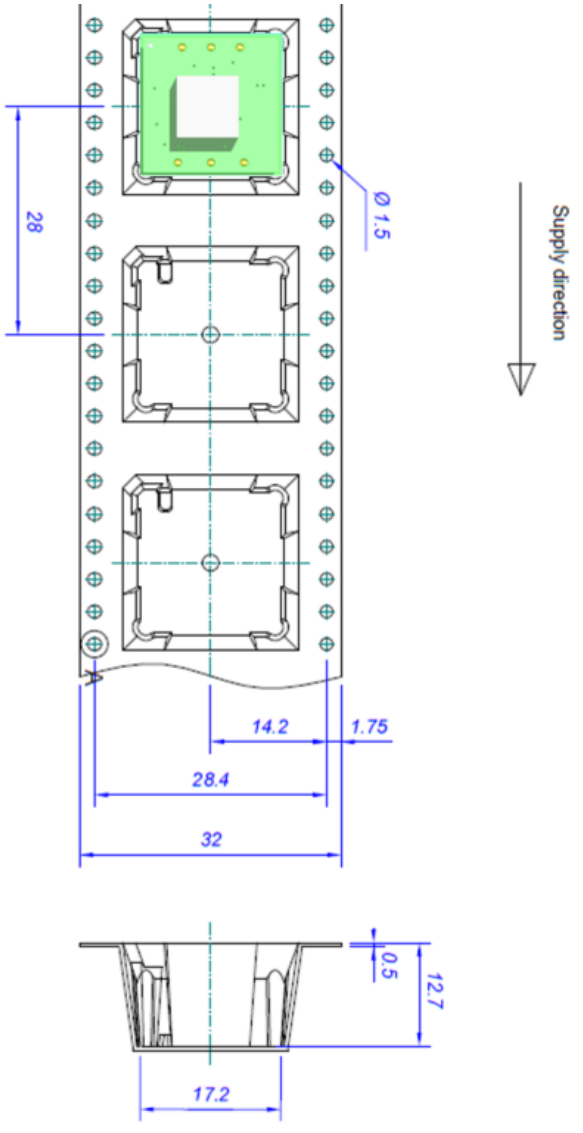
EIA standard carrier tape



Delivery Package Information

The products are delivered in antistatic carrier tape (EIA 481 standard).

Carrier Tape Specifications	
Material	Antistatic PS
Surface resistance	< 10^{11} Ohm/square
Bakeability	The tape is not bakable
Tape width, W	32 mm [1.26 inch]
Pocket pitch, P_1	28 mm [1.1 inch]
Pocket depth, K_0	12.7 mm [0.5 inch]
Reel diameter	381 mm [15 inch]
Reel capacity	100 products /reel
Reel weight	1.2 kg/full reel



flex

Technical Specification

BMR520 series DC-DC Converters Input 42.5-75 V, Output up to 25 A / 300 W	28701-BMR520 Rev A March 2022 © Flex

Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T_A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether {Isopropyl alcohol}	55°C 35°C {35°C}
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity	J-STD-020E	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	900 h
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g^2/Hz 10 min in each direction

PMBus Command Appendix

This appendix contains a detailed reference of the PMBus commands supported by the product.

Data Formats
The products make use of a few standardized numerical formats, along with custom data formats. A detailed walkthrough of the above formats is provided in AN304, as well as in sections 7 and 8 of the PMBus Specification Part II. The custom data formats vary depending on the command, and are detailed in the command description.

Standard Commands
The functionality of commands with code 0x00 to 0xCF is usually based on the corresponding command specification provided in the PMBus Standard Specification Part II (see Power System Management Bus Protocol Documents below). However there might be different interpretations of the PMBus Standard Specification or only parts of the Standard Specification applied, thus the detailed command description below should always be consulted.

Forum Websites
The System Management Interface Forum (SMIF)
http://www.powersig.org/
The System Management Interface Forum (SMIF) supports the rapid advancement of an efficient and compatible technology base that promotes power management and systems technology implementations. The SMIF provides a membership path for any company or individual to be active participants in any or all of the various working groups established by the implementer forums.

Power Management Bus Implementers Forum
(PMBUS-IF)
http://pmbus.org/
The PMBus-IF supports the advancement and early adoption of the PMBus protocol for power management. This website offers recent PMBus specification documents, PMBus articles, as well as upcoming PMBus presentations and seminars, PMBus Document Review Board (DRB) meeting notes, and other PMBus related news.

PMBus – Power System Management Bus Protocol Documents
These specification documents may be obtained from the PMBus-IF website described above. These are required reading for complete understanding of the PMBus implementation. This appendix will not re-address all of the details contained within the two PMBus Specification documents.

Specification Part I – General Requirements Transport And Electrical Interface
Includes the general requirements, defines the transport and electrical interface and timing requirements of hard wired signals.

Specification Part II – Command Language
Describes the operation of commands, data formats, fault management and defines the command language used with the PMBus.

SMBus – System Management Bus Documents
System Management Bus Specification, Version 2.0, August 3, 2000
This specification specifies the version of the SMBus on which Revision 1.2 of the PMBus Specification is based. This specification is freely available from the System Management Interface Forum Web site at:
http://www.smbus.org/specs/

PMBus Command Summary and Factory Default Values of Standard Configuration

The factory default values provided in the table below are valid for the Standard configuration. Factory default values for other configurations can be found using the Flex Power Designer tool.

Code	Name	Data Format	Factory Default Value Standard Configuration BMR 520 20XX/001 R1	
0x01	OPERATION	R/W Byte	0x48	
0x02	ON_OFF_CONFIG	R/W Byte	0x16	
0x03	CLEAR_FAULTS	Send Byte		
0x10	WRITE_PROTECT	R/W Byte	0x00	
0x11	STORE_DEFAULT_ALL	Send Byte		
0x12	RESTORE_DEFAULT_ALL	Send Byte		
0x19	CAPABILITY	Read Byte		
0x1B	SMBALERT_MASK (STATUS_BYTE)	SMBAlert Mask	0x80	
0x1B	SMBALERT_MASK (STATUS_VOUT)	SMBAlert Mask	0x08	
0x1B	SMBALERT_MASK (STATUS_IOUT)	SMBAlert Mask	0x2A	
0x1B	SMBALERT_MASK (STATUS_INPUT)	SMBAlert Mask	0x00	
0x1B	SMBALERT_MASK (STATUS_TEMPERATURE)	SMBAlert Mask	0x40	
0x1B	SMBALERT_MASK (STATUS_CML)	SMBAlert Mask	0xF1	
0x1B	SMBALERT_MASK (STATUS_MFR_SPECIFIC)	SMBAlert Mask	0xFD	
0x20	VOUT_MODE	Read Byte		
0x21	VOUT_COMMAND	R/W Word	0x00B3	
0x24	VOUT_MAX	Read Word	0x00CA	
0x25	VOUT_MARGIN_HIGH	R/W Word	0x00CA	
0x26	VOUT_MARGIN_LOW	R/W Word	0x009C	
0x28	VOUT_DROOP	R/W Word	0xD000	
0x35	VIN_ON	R/W Word	0xE950	
0x40	VOUT_OV_FAULT_LIMIT	Read Word		
0x41	VOUT_OV_FAULT_RESPONSE	Read Byte	0x80	
0x44	VOUT_UV_FAULT_LIMIT	Read Word		
0x45	VOUT_UV_FAULT_RESPONSE	R/W Byte	0x80	
0x46	IOUT_OC_FAULT_LIMIT	R/W Word	0xF1A4	
0x47	IOUT_OC_FAULT_RESPONSE	R/W Byte	0x80	
0x4A	IOUT_OC_WARN_LIMIT	R/W Word	0xF168	
0x4F	OT_FAULT_LIMIT	R/W Word	0xF21C	
0x50	OT_FAULT_RESPONSE	R/W Byte	0x80	
0x51	OT_WARN_LIMIT	R/W Word	0xF1CC	
0x55	VIN_OV_FAULT_LIMIT	R/W Word	0xEA80	
0x56	VIN_OV_FAULT_RESPONSE	R/W Byte	0x80	
0x59	VIN_UV_FAULT_LIMIT	R/W Word	0xE940	
0x5A	VIN_UV_FAULT_RESPONSE	R/W Byte	0x80	
0x60	TON_DELAY	R/W Byte	0x00	
0x68	POUT_OP_FAULT_LIMIT	R/W Word	0x00D2	
0x69	POUT_OP_FAULT_RESPONSE	R/W Byte	0x00	
0x78	STATUS_BYTE	Read Byte		
0x79	STATUS_WORD	Read Word		
0x7A	STATUS_VOUT	Read Byte		
0x7B	STATUS_IOUT	Read Byte		
0x7C	STATUS_INPUT	Read Byte		
0x7D	STATUS_TEMPERATURE	Read Byte		
0x7E	STATUS_CML	Read Byte		
0x80	STATUS_MFR_SPECIFIC	Read Byte		
0x88	READ_VIN	Read Word		
0x8B	READ_VOUT	Read Word		
0x8C	READ_IOUT	Read Word		
0x8D	READ_TEMPERATURE_1	Read Word		
0x96	READ_POUT	Read Word		
0x98	PMBUS_REVISION	Read Byte		

Code	Name	Data Format	Factory Default Value Standard Configuration BMR 520 20XX/001 R1	
0x99	MFR_ID	Read Block3	Unit Specific	
0x9A	MFR_MODEL	Read Block8	Unit Specific	
0x9B	MFR_REVISION	Read Block3	Unit Specific	
0x9D	MFR_DATE	Read Block4	Unit Specific	
0xB0	USER_DATA_00	Read Word	Unit Specific	
0xB1	USER_DATA_01	Read Word	Unit Specific	
0xD1	MFR_AVERAGE_TIME_SCALE	R/W Byte	0x06	6 ms
0xD2	MFR_READ_VOUT	Read Word		
0xD3	MFR_IOUT_CAL_OFFSET	Read Word	0x0000	0 ADC steps
0xD4	MFR_VOUT_CAL_OFFSET	Read Word	0x0066	
0xD6	MFR_PID	Read Block7	0x0001E10004003C	
0xD7	MFR_FILT_PRE_POST	Read Word	0x2A2B	
0xD8	MFR_CELL_MISMATCH_MIN_MAX	Read Byte		
0xD9	MFR_DUTY_PARAMETER	R/W Block3	0x000000	
0xDB	MFR_LOCK	Send Byte		
0xDC	MFR_FAULT_CONFIG	R/W Word	0x02C7	
0xDE	MFR_IMON	R/W Byte	0x06	
0xDF	MFR_STORE_MAP	Send Byte		
0xE0	MFR_RESTORE_MAP	Send Byte		
0xE1	MFR_CATASTROPHIC_FAULT_LIMIT	R/W Word	0x03FF	
0xE2	MFR_CATASTROPHIC_FAULT_RESPONSE	R/W Byte	0x00	
0xE3	MFR_CS_CELL_WARN_LIMIT	R/W Word	0xF014	
0xE4	MFR_CELL_CONFIG	R/W Byte	0x02	
0xE5	MFR_OV_LIMIT_OFFSET	R/W Byte	0x07	
0xE6	MFR_UV_LIMIT_OFFSET	R/W Byte	0x06	
0xE7	MFR_VBOOT_SET	R/W Word	0x0033	
0xE8	MFR_SVI_PMBUS_SELECT	Read Byte	0x01	
0xE9	MFR_ICC_MAX_ADD	R/W Byte	0x00	
0xEA	MFR_PWR_IN_MAX_ADD	R/W Byte	0x00	
0xEB	MFR_PWR_IN_ALERT_ADD	R/W Byte	0x00	
0xEF	MFR_READ_PIN_PUC	Read Word		
0xF0	MFR_READ_VIN_PUC	Read Word		
0xF1	MFR_DPM1_THR	Read Word	0xF03C	
0xF2	MFR_DPM2_THR	Read Word	0xF078	
0xF3	MFR_DPM3_THR	R/W Word	0xF140	
0xF4	MFR_DPM4_THR	R/W Word	0xF190	
0xF5	MFR_DPM5_THR	R/W Word	0xF1E0	
0xF6	MFR_FSWITCH_PROTECT_COEFF	R/W Byte	0x0F	
0xF7	MFR_CS_PROP_INTEGR	R/W Word	0x0005	
0xF8	MFR_T_START_PH_SHIFT_DELTA_DELAY	R/W Block5	0x0008010001	
0xF9	MFR_KK_FEEDFRWD_GAIN_CTRL	R/W Block6	0x000000028A00	
0xFA	MFR_VOUT_TRIM	R/W Byte	Unit Specific	
0xFB	MFR_MANUAL_CELL_SHED	R/W Word	0x040B	
0xFE02	MFR_SVID_TEMPZONE	R/W Byte		
0xFE03	MFR_SVID_IOUT	R/W Byte		
0xFE04	MFR_SVID_VIDSETTING	R/W Word		
0xFE05	MFR_SVID_PWRSTATE	R/W Byte		
0xFE06	MFR_SVID_OFFSET	R/W Byte	0x00	
0xFE07	MFR_START_THREAD	R/W Block3	0x000064	
0xFE08	MFR_SVID_ICCMAX	R/W Byte	0x32	
0xFE09	MFR_SVID_TEMPMAX	R/W Byte	0x78	
0xFE0A	MFR_SVID_SRFAST	R/W Byte	0x0A	
0xFE0B	MFR_SVID_SRSLOW	R/W Byte	0x00	
0xFE0C	MFR_SVID_MULTI_VR_CONFIG	R/W Byte		
0xFE0D	MFR_SVID_VOUTMAX	R/W Byte	0xBA	
0xFE0E	MFR_SVID_SLOW_SR_SELECTOR	R/W Byte	0x08	
0xFE0F	MFR_SVID_PIN_MAX	R/W Byte	0x00	
0xFE10	MFR_SVID_PIN_ALERT_THR	R/W Byte	0x00	
0xFE11	MFR_SVID_WP0	R/W Byte		

Code	Name	Data Format	Factory Default Value Standard Configuration BMR 520 20XX/001 R1	
0xFE12	MFR_SVID_WP1	R/W Byte		
0xFE13	MFR_SVID_WP2	R/W Byte		
0xFE14	MFR_SVID_WP3	R/W Byte		
0xFE15	MFR_SVID_WP4	R/W Byte		
0xFE16	MFR_RD_TEMPERATURE_PHASE1	Read Word		
0xFE17	MFR_RD_TEMPERATURE_PHASE2	Read Word		
0xFE18	MFR_RD_TEMPERATURE_PHASE3	Read Word		
0xFE19	MFR_RD_TEMPERATURE_PHASE4	Read Word		
0xFE1A	MFR_RD_TEMPERATURE_PHASE5	Read Word		
0xFE1B	MFR_RD_TEMPERATURE_PHASE6	Read Word		
0xFE1C	MFR_CTRL_ID	Read Word		
0xFE1D	MFR_READ_CURR_MISMATCH	Read Word		
0xFE1E	MFR_SVID_REGLOCK	R/W Byte		
0xFE20	MFR_SECT_L	R/W Block8		
0xFE21	MFR_SECT_H	R/W Block8		
0xFE24	MFR_SECT_RD	Write Byte		
0xFE25	MFR_SECT_WR	Write Byte		
0xFE26	MFR_MEMORY_WORD	R/W Block8		
0xFE27	MFR_MEMORY_RD	Write Block3		
0xFE28	MFR_MEMORY_WR	Write Block4		
0xFE29	MFR_READ_BLACKBOX	Send Byte		
0xFE2A	MFR_BLACKBOX	Read Block16		
0xFE2B	MFR_CLEAR_BB	Send Byte		
0xFE2C	MFR_CONFIG_BBR	R/W Word	0x0000	
0xFE2E	MFR_PROTECT_DEFAULT	R/W Byte	0x00	
0xFE2F	MFR_POUT_THREAD	Read Block4		
0xFE30	MFR_PMBUSCFG_REVISION	R/W Word	0000	
0xFE31	MFR_PMBUSCFG_TIMESTAMP	Read Block8	Unit Specific	
0xFE32	MFR_PEAK_FAULT_RESPONSE	R/W Byte	0x00	
0xFE33	MFR_PMBUSCFG_USERID	R/W Word	0x2121	

System Registers

Offset	Name	Factory Default Value Standard Configuration BMR 520 20XX/001 R1
0xA407	K_TRANSIENT	0x00
0xA408	CURRENT_SHARING_RESET	0x00
0xA40B	HIGH_CURR_PROT_EN	0x04
0xA40D	AVS_CONFIG	0x00
0xA40E	FBCOT_TSWITCH_MAIN_NOM	0x0050
0xA410	FBCOT_CONST_FEED_FWD_NVM	0x0308
0xA412	FBCOT_MIXED	0x86
0xA413	FBCOT_T_SWITCH_C	0x0001
0xA415	FBCOT_INV_MOD_INDEX	0x0000
0xA417	FBCOT_NTRAFO	0x08
0xA418	HIZ_HALFB_SYMMETRIC	0x34
0xA419	TSHIFT_MIN	0x0C
0xA41A	CHOPPER_CLK_CONF	0x00
0xB003	SVID_IFC_CONF	0x01
0xB006	CTRL_PFM_ENA_PS	0x03
0xB007	DPM_HYSTERESIS	0x28
0xB00C	DVID_SR_FAST_STEP	0x3F
0xB00D	DVID_SR_SLOW_STEP	0x31
0xB00E	DVID_VAR_OFFSET_PARAM	000000002320
0xB018	TEL_GAIN_VIN	0x81
0xB01A	THERMAL_GAIN	0x00
0xB01B	TEL_IOUT_FSR	0x008A
0xB027	TEL_OFFSET_VIN	0x000A

Offset	Name	Factory Default Value Standard Configuration BMR 520 20XX/001 R1
0xB029	TEL_GAIN_IMON	0x8C
0xB02A	TEL_GAIN_FGBR	0x80
0xB02B	SVI_ADDITIONAL_OFFSET	0x09
0xB02F	TEST_MUXES	0x00000000
0xB038	VIN_FEED_FWD_SOURCE	0x01
0xB039	VIN_MONITORING_SOURCE	0x01
0xB03C	IOUT_VR125_PERC_EN	0x01
0xB03D	OPTO_EN	0x01
0xB03E	EN_TIMEOUT_RESONANT_END	0x01
0xB03F	EN_DUTY_ACTIVE	0x01
0xB040	VR13_TIME_FRAME	0x00
0xB041	CTRL_VERR_CLAMP	0x00
0xB042	T_SWITCHING_OPEN_LOOP	0x0000
0xB044	DISABLE_DPM_PROT	0x00
0xB046	TGB_CONFIG	0x00
0xB048	OPEN_LOOP_CONFIG	0x0000
0xB04A	TON_RED_CONFIG	0x08
0xB04B	EN_DROOP_START	0x00
0xB04C	VR_TAB_RAIL	0x00
0xB04E	CS_OVERFLOW_DISABLE_IRQ	0x01
0xB051	VR_READY_FAST_DISABLE	0x00
0xB052	DCR_INV_COEFF	0x2D
0xB056	ADC_PEAK_EN_TOP	0x01
0xB057	MULTIFUNCTION_PIN_MUX	0x04
0xB05B	NCHECKS	0x04
0xB05E	MONITOR_OFFSET	0x04
0xB061	IMONX2	0x01
0xB062	IOUT_EXP	0x00
0xB063	EXTRA_OFFSET	0x00
0xB064	DPM_OFFSET	0x14
0xB065	SOFT_OFF_CONFIG	0x00

PMBus Command Details

OPERATION (0x01)
Description: Sets the desired PMBus enable and margin operations.

Bit	Function	Description	Value	Function	Description
7:6	Enable	Make the device enable or disable.	00	Immediate Off	Disable immediately without controlled ramp-down or sequencing.
			01	Soft Off	Disable by controlled ramp-down timings or sequencing.
			10	Always On	Enable device to the set voltage or margin state, using ramp up timings / sequencing.
5:4	Output Voltage Source	Select between margin high/low states or nominal output, and control by AVSBus.	00	Nominal	Operate at nominal output voltage given by VOUT_COMMAND.
			01	Margin Low	Operate at margin low voltage set in VOUT_MARGIN_LOW.
			10	Margin High	Operate at margin high voltage set in VOUT_MARGIN_HIGH.
3:2	Act on Fault	Set 10b to act on fault or set to 01b to ignore fault.	10	Act on Faults	Act on Faults when in a margined state. The device will handle appropriate overvoltage/under voltage warnings and faults and respond as programmed by the warning limit or fault response command.

ON_OFF_CONFIG (0x02)
Description: Configures how the device is controlled by the CTRL pin and the PMBus.

Bit	Function	Description	Value	Function	Description
4	Powerup Operation	Sets the default to either operate any time power is present or for the on/off to be controlled by CTRL pin and PMBus commands.	0	Enable Always	Unit powers up any time power is present regardless of state of the CTRL pin.
			1	CTRL pin or PMBus	Unit does not power up until commanded by the CTRL pin and OPERATION command.
3	PMBus Enable Mode	Controls how the unit responds to commands received via the PMBus.	0	Ignore PMBus command	Unit ignores the on/off portion of the OPERATION command from serial bus.
			1	Use PMBus command	To start, the unit requires that the on/off portion of the OPERATION command is instructing the unit to run.
2	Enable Pin Mode	Controls how the unit responds to the CTRL pin.	0	Ignore CTRL pin	Unit ignores the CTRL pin.
			1	Use CTRL pin	Unit requires the CTRL pin to be asserted to start the unit.
1	Enable Pin Polarity	Polarity of the CTRL pin.	1	Active High	CTRL pin will cause device to enable when driven high.

CLEAR_FAULTS (0x03)
Description: Clears all fault status bits

WRITE_PROTECT (0x10)
Description: The WRITE_PROTECT command is used to control writing to the PMBus device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. This command is stored in NVM but not included in a MFR_STORE_MAP operation (STORE_DEFAULT_ALL must be used).

Bit	Description	Value	Function	Description
7:0	All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.	0x80	Disable all writes	Disable all writes except to the WRITE_PROTECT command.
		0x40	Enable operation Only	Disable all writes except to the WRITE_PROTECT, OPERATION and PAGE commands.
		0x20	Enable control and Vout commands	Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG and VOUT_COMMAND commands.
		0x00	Enable all commands	Enable writes to all commands.

STORE_DEFAULT_ALL (0x11)
Description: Commands the device to store its configuration into the Default Store.

RESTORE_DEFAULT_ALL (0x12)
Description: Commands the device to restore its configuration from the Default Store.

CAPABILITY (0x19)
Description: Reads back the supported SMBus features

Bit	Description	Format
7:0	Reads back the supported SMBus features	Byte Array

SMBALERT_MASK (0x1B)
Status Registers: STATUS_BYTE (0x78), STATUS_VOUT (0x7A), STATUS_IOUT (0x7B), STATUS_INPUT (0x7C), STATUS_TEMPERATURE (0x7D), STATUS_CML (0x7E), STATUS_MFR_SPECIFIC (0x80)
Description: The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SALERT output signal.

Bit	Function	Description	Value	Function	Description
7	Mask Bit 7		0	Pull SALERT	
			1	Ignore	
6	Mask Bit 6		0	Pull SALERT	
			1	Ignore	
5	Mask Bit 5		0	Pull SALERT	
			1	Ignore	
4	Mask Bit 4		0	Pull SALERT	
			1	Ignore	
3	Mask Bit 3		0	Pull SALERT	
			1	Ignore	
2	Mask Bit 2		0	Pull SALERT	
			1	Ignore	
1	Mask Bit 1		0	Pull SALERT	
			1	Ignore	
0	Mask Bit 0		0	Pull SALERT	
			1	Ignore	

VOUT_MODE (0x20)
Description: Controls how future VOUT-related commands parameters will be interpreted.

Bit	Function	Description	Value	Function	Description
7:5	Vout mode	Selection of mode for representation of output voltage parameters.	000	Linear	Linear Mode Format.
			001	VID	VID Mode.
			010	Direct	Direct Mode.
4:0	VID code identifier	Five bit VID code identifier. See SVID_IFC_CONF description.	00000	AVSBus	AVSBus Vout mode.
			00011	Intel	Intel Vout mode.

VOUT_COMMAND (0x21)
Description: Commands the device to transition to a new output voltage.

Bit	Description	Format	Unit
9:0	Sets the nominal output voltage value [VID] - Data need to be compliant with format specified in VOUT_MODE. In AVS domain see specifications of OPERATION command. In SVI domain, the command is acknowledged and information stored.	Fixed Point Unsigned	V

VOUT_MAX (0x24)
Description: Configures the maximum allowed output voltage.

Bit	Description	Format	Unit
9:0	Sets the maximum possible value setting of VOUT.	Fixed Point Unsigned	V

VOUT_MARGIN_HIGH (0x25)
Description: Configures the target for margin-up commands.

Bit	Description	Format	Unit
9:0	Sets the value of the VOUT during a margin high.	Fixed Point Unsigned	V

VOUT_MARGIN_LOW (0x26)
Description: Configures the target for margin-down commands.

Bit	Description	Format	Unit
9:0	Sets the value of the VOUT during a margin low.	Fixed Point Unsigned	V

VOUT_DROOP (0x28)
Description: Sets the effective load line (V/I slope) for the rail in which the device is used. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -6 (0b11010).

Bit	Description	Format	Unit
7:0	LSB = 0.015625 mV/A.	Fixed Point Unsigned	mV/A

VIN_ON (0x35)
Description: Input voltage must be above this level before the output can be enabled. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -3 (0b11101).

Bit	Description	Format	Unit
9:0	LSB = 0.125 V	Fixed Point Unsigned	V

VOUT_OV_FAULT_LIMIT (0x40)
Description: Reads the absolute Vout over-voltage fault threshold computed as: Vout target - MFR_OV_LIMIT_OFFSET The returned value is valid only when regulation of Vout is enabled. To change the threshold, MFR_OV_LIMIT_OFFSET should be changed.

Bit	Description	Format	Unit
15:0	LSB = 0.00390625 V.	Fixed Point Unsigned	V

VOUT_OV_FAULT_RESPONSE (0x41)
Description: Sets the VOUT OV fault response. Always set to 0x80 (thus cannot be ignored).

Bit	Description	Value	Function	Description

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x80 (Latched) is implemented.	0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

VOUT_UV_FAULT_LIMIT (0x44)
Description: Reads the absolute Vout under-voltage fault threshold computed as: Vout target - MFR_UV_LIMIT_OFFSET - VOUT_DROOP*Iout The returned value is valid only when regulation of Vout is enabled. To change the threshold, MFR_UV_LIMIT_OFFSET should be changed.

Bit	Description	Format	Unit
15:0	LSB = 0.00390625 V.	Fixed Point Unsigned	V

VOUT_UV_FAULT_RESPONSE (0x45)
Description: Sets the VOUT UV LIMIT Response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

IOUT_OC_FAULT_LIMIT (0x46)
Description: Sets the output over-current fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -2 (0b11110).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

IOUT_OC_FAULT_RESPONSE (0x47)
Description: Sets the IOUT OC LIMIT Response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

IOUT_OC_WARN_LIMIT (0x4A)
Description: Sets the output over-current warning limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -2 (0b11110).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

OT_FAULT_LIMIT (0x4F)
Description: Sets the over-temperature fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -2 (0b11110).

Bit	Description	Format	Unit
9:0	LSB = 0.25 Celsius Degrees.	Fixed Point Unsigned	°C

OT_FAULT_RESPONSE (0x50)
Description: Sets the over-temperature fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

OT_WARN_LIMIT (0x51)
Description: Sets the over-temperature warning limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -2 (0b11110).

Bit	Description	Format	Unit
9:0	LSB = 0.25 Celsius Degrees.	Fixed Point Unsigned	°C

VIN_OV_FAULT_LIMIT (0x55)
Description: Sets the input over-voltage fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -3 (0b11101).

Bit	Description	Format	Unit
9:0	LSB = 0.125 V.	Fixed Point Unsigned	V

VIN_OV_FAULT_RESPONSE (0x56)
Description: Sets the input over-voltage fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

VIN_UV_FAULT_LIMIT (0x59)
Description: Sets the input under-voltage fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -3 (0b11101).

Bit	Description	Format	Unit
9:0	LSB = 0.125 V.	Fixed Point Unsigned	V

VIN_UV_FAULT_RESPONSE (0x5A)
Description: Sets the input under-voltage fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

TON_DELAY (0x60)
Description: Sets the turn-on delay time

Bit	Description	Format	Unit

Bit	Description	Format	Unit
7:0	Sets the delay time from ENABLE to start of the rise of the output voltage. The time can range from 0 ms up to 127.5 ms. For a current sharing group this range is valid if PMBus enable or CTRL pin enable is used. LSB = 0.5 ms.	Fixed Point Unsigned	ms

POUT_OP_FAULT_LIMIT (0x68)
Description: Sets the Output power over-power fault limit. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = 1 (0b00001).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	W

POUT_OP_FAULT_RESPONSE (0x69)
Description: Sets the output power Over-Power fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

STATUS_BYTE (0x78)
Description: Returns a brief fault/warning status byte.

Bit	Function	Description	Value	Description
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No fault
			1	Fault
6	Off	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	0	No fault
			1	Fault
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No fault
			1	Fault
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No fault
			1	Fault
3	Vin under voltage Fault	An input under voltage fault has occurred.	0	No fault
			1	Fault
2	Temperature	A temperature fault or warning has occurred.	0	No fault
			1	Fault
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault
			1	Fault
0	None of the Above	A fault or warning not listed in bits [7:1] has occurred.	0	No fault
			1	Fault

STATUS_WORD (0x79)
Description: Returns an extended fault/warning status byte.

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has occurred.	0	No fault
			1	Fault
14	Iout/Pout	An output current or output power fault or warning has occurred.	0	No Fault.
			1	Fault.
13	Input	An input voltage, input current, or input power fault or warning has occurred.	0	No Fault.
			1	Fault.
12	Mfr	A manufacturer specific fault or warning has occurred.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No Fault.
			1	Fault.
6	Off	This bit is asserted if the unit is not providing power	0	No Fault.

Bit	Function	Description	Value	Description
		to the output, regardless of the reason, including simply not being enabled.	1	Fault.
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No Fault.
			1	Fault.
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No Fault.
			1	Fault.
3	Vin under voltage Fault	An input under voltage fault has occurred.	0	No Fault.
			1	Fault.
2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault.
			1	Fault.
0	None of the Above	A fault or warning not listed in bits [7:1] has occurred.	0	No fault.
			1	Fault.

STATUS_VOUT (0x7A)
Description: Returns Vout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vout Overvoltage Fault	Vout Overvoltage Fault.	0	No Fault.
			1	Fault.
4	Vout under voltage Fault	Vout under voltage Fault.	0	No Fault.
			1	Fault.
3	Vout Max Warning	Vout Max Warning (An attempt has been made to set the output voltage to value higher than allowed by the Vout Max command (Section 13.5).	0	No Warning.
			1	Warning.

STATUS_IOUT (0x7B)
Description: Returns Iout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Iout Overcurrent Fault	Iout Overcurrent Fault.	0	No Fault.
			1	Fault.
5	Iout Overcurrent Warning	Iout Overcurrent Warning.	0	No Fault.
			1	Fault.
3	Current Sharing Unbalance Warning	Triggered when difference in monitored current from two phases is higher than the limit set by MFR_CS_CELL_WARN_LIMIT.	0	No Fault.
			1	Fault.
1	Pout Over Power Fault	Pout Over Power Fault.	0	No Fault.
			1	Fault.

STATUS_INPUT (0x7C)
Description: Returns VIN/IIN-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vin Overvoltage Fault	Vin Overvoltage Fault.	0	No Fault.
			1	Fault.
4	Vin under voltage Fault	Vin under voltage Fault.	0	No Fault.
			1	Fault.

STATUS_TEMPERATURE (0x7D)
Description: Returns the temperature-related fault/warning status bits

Bit	Function	Description	Value	Description
7	Overtemperature Fault	Overtemperature Fault.	0	No Fault.
			1	Fault.
6	Overtemperature Warning	Overtemperature Warning.	0	No Warning.
			1	Warning.

STATUS_CML (0x7E)
Description: Returns Communication/Logic/Memory-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Invalid Or Unsupported Command Received	Invalid Or Unsupported Command Received.	0	No Invalid Command Received.
			1	Invalid Command Received.
6	Invalid Or Unsupported Data Received	Invalid Or Unsupported Data Received.	0	No Invalid Data Received.
			1	Invalid Data Received.
5	Packet Error Check Failed	Packet Error Check Failed.	0	No Failure.
			1	Failure.
4	Memory Fault Detected	Memory Fault Detected. Set if CRC check fails at boot-up.	0	No Fault.
			1	Fault.
0	Other Memory Or Logic Fault	Other Memory Or Logic Fault has occurred.	0	No Fault.
			1	Fault.

STATUS_MFR_SPECIFIC (0x80)
Description: Returns manufacturer specific status information.

Bit	Function	Description	Value	Description
7	Black box full	Black box full	0	No Fault.
			1	Fault.
6	Catastrophic fault precursor	Catastrophic fault precursor	0	No Fault.
			1	Fault.
5	NVM status(1)	NVM status(1)	0	No Fault.
			1	Fault.
4	NVM status(0)	NVM status(0)	0	No Fault.
			1	Fault.
3	VSRMON peak fault	VSRMON peak threshold reached.	0	No Fault.
			1	Fault.
2	Patch code download (from I2C)	Patch code download (from I2C)	0	No Fault.
			1	Fault.
1	Feedback disconnection	Feedback disconnection fault = +S vs VOUT voltage difference is too high.	0	No Fault.
			1	Fault.
0	PUC CRC Fault	PUC CRC Fault	0	No Fault.
			1	Fault.

READ_VIN (0x88)
Description: Returns the input voltage reading, value averaged over configured MFR_AVERAGE_TIME_SCALE. Input voltage source configured by System Register VIN_MONITORING_SOURCE.

Bit	Description	Format	Unit
15:0	LSB=0.125 V.	Linear	V

READ_VOUT (0x8B)
Description: Returns the measured output voltage, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	VID code, see section Output Voltage Format.	Fixed Point Unsigned	V

READ_IOUT (0x8C)
Description: Returns the measured output current, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	LSB weight is given by System Register IOUT_EXP.	Linear	A

READ_TEMPERATURE_1 (0x8D)
Description: Returns the max temperature read from Main/Satellites (and from primary reporting through PuC, if enabled).

Bit	Description	Format	Unit
15:0	LSB=0.25 degree C.	Linear	°C

READ_POUT (0x96)
Description: Returns the computed output power, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	Read system output power.	Fixed Point Unsigned	W

PMBUS_REVISION (0x98)
Description: Returns the PMBus revision number for this device.

Bit	Description	Format
7:0	Returns the PMBus revision number for this device. Returns 0x22, formatted as per PMBus specification.	ASCII

MFR_ID (0x99)
Description: Not used for Flex manufacture information. Instead see USERDATA00, USERDATA01 and MFR_PMBUSCFG_TIMESTAMP.

Bit	Description	Format
23:0		ASCII

MFR_MODEL (0x9A)
Description: Not used for Flex manufacture information. Instead see USERDATA00, USERDATA01 and MFR_PMBUSCFG_TIMESTAMP.

Bit	Description	Format
63:0		ASCII

MFR_REVISION (0x9B)
Description: Not used for Flex manufacture information. Instead see USERDATA00, USERDATA01 and MFR_PMBUSCFG_TIMESTAMP.

Bit	Description	Format
23:0		ASCII

MFR_DATE (0x9D)
Description: Not used for Flex manufacture information. Instead see USERDATA00, USERDATA01 and MFR_PMBUSCFG_TIMESTAMP.

Bit	Description	Format
31:0		ASCII

USER_DATA_00 (0xB0)
Description: Contains serial # from production, together with USER_DATA_01. Complete serial #, e.g. DL5A123456, contains: Factory code ("DL5", represented as enum by 4 bits). Letter ("A", represented by ASCII 8 bits). Number with 6 digits (123456, represented by 20 bits).

Bit	Description	Format
15:0	Least 16 bits of number being part of serial #.	Integer Unsigned

USER_DATA_01 (0xB1)
Description: Contains serial # from production, together with USER_DATA_00. Complete serial #, e.g. DL5A123456, contains: Factory code ("DL5", represented as enum by 4 bits). Letter ("A", represented by ASCII 8 bits). Number with 6 digits (123456, represented by 20 bits).

Bit	Function	Description	Format

Bit	Function	Description	Format
15:12	Factory code of serial #	Factory code being part of serial #. 0x00=DL5. 0x01=CB6, 0x02=DL6, 0x03=DL7. Other values may be used in the future.	Byte Array
11:4	Letter of serial #	Letter after factory code in serial #. For example "A" in serial #: DL5A123456.	ASCII
3:0	Number of serial # - Addend 1	Most 4 bits of number being part of serial #.	Fixed Point Unsigned

MFR_AVERAGE_TIME_SCALE (0xD1)
Description: Used to sets the time period between two measurements.

Bit	Description	Format	Unit
3:0	Manufacture specific average time scale. Used to sets the time period between two measurements. [3:0]: Averaging time = 1.2 * 2^MFR_AVERAGE_TIME_SCALE [ms].	Integer Unsigned	ms

MFR_READ_VOUT (0xD2)
Description: Returns the output voltage, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	Linear format. LSB = 3.90625 mV.	Linear	V

MFR_IOUT_CAL_OFFSET (0xD3)
Description: Mfr output current calibration Offset.

Bit	Description	Format	Unit
15:0	Used to add a calibration offset for READ_IOUT monitoring. # of ADC Steps. ADC step = TEL_IOUT_FSR / 2^9.	Integer Signed	ADC steps

MFR_VOUT_CAL_OFFSET (0xD4)
Description: Mfr output voltage calibration Offset.

Bit	Description	Format	Unit
10:0	Used to add a calibration offset for READ_VOUT monitoring. # of ADC Steps. ADC step = 2.5V / (2^9) = 4.8828 mV.	Fixed Point Signed	mV

MFR_PID (0xD6)
Description: Configures the linear control loop filter coefficients.

Bit	Function	Description	Format
50:32	PID C1 PD	Contains PID coefficient PID_C1_PD. PID_C1_PD = 8 * (kP + kD / 25nSec) - max 0x7FFFF	Integer Unsigned
31:16	PID C1 F	Contains PID coefficient PID_C1_F. PID_C1_F = kI * 25nSec * 2^16 - max 0xFFFF	Integer Unsigned
15:0	PID C3	Contains PID coefficient PID_C3. PID_C3 = kD / 25nSec - max 0xFFFF	Integer Unsigned

MFR_FILT_PRE_POST (0xD7)
Description: Configures the linear control loop filter coefficients.

Bit	Function	Description	Format
14:7	PID LP PRE	Contains PID coefficient PID LP PRE. PID_LP_PRE = 25nSec/(25nSec + tPRE)*2^8. E.g. tPRE = 50 ns => PID_LP_PRE = 85.	Integer Unsigned
6:0	PID LP Post	Contains PID coefficient PID LP POST. PID_LP_POST = 25nSec/(25nSec + tPOST)*2^7; max 0x7F. E.g. tPOST = 50 ns => PID_LP_POST = 43.	Integer Unsigned

MFR_CELL_MISMATCH_MIN_MAX (0xD8)
Description: Returns phase # for phases with min/max output current in case of current sharing unbalance warning, i.e. when mismatch is greater than threshold set by MFR_CS_CELL_WARN_LIMIT.

Bit	Function	Description	Format

Bit	Function	Description	Format
5:3	Current Sharing - Max Current Phase	Phase with max output current. 0d = phase #1, 1d = phase #2, etc.	Integer Unsigned
2:0	Current Sharing - Min Current Phase	Phase with min output current. 0d = phase #1, 1d = phase #2, etc.	Integer Unsigned

MFR_DUTY_PARAMETER (0xD9)
Description: Used to configure TSTART Correction to control average Duty Cycle for the regulation in case of low VIN value (i.e. TSTART is artificially increased to boost secondary Phase Bump to maintain current capability). Integrative and Proportional corrections. Only for resonant topology. VOLTAGE_DUTY_ENABLE is the voltage below which the correction engages. Through System register TON_RED_CONFIG, bit #6, it is possible to disable phase shedding when VIN is below VOLTAGE_DUTY_ENABLE. Note. kDUTY is 8 bit wide and split between this command and MFR_KK_FEEDFRWD_GAIN_CTRL.

Bit	Function	Description	Format	Unit
23:14	KDUTY Voltage Enable	Contains PID coefficient VOLTAGE_DUTY_ENABLE. [#of 0.125V steps]; max 127.875V.	Fixed Point Unsigned	V
13:9	KDUTY Proportional	Contains PID coefficient KDUTY_PROPORTIONAL. Max value is 0x1F.	Integer Unsigned	
8:3	KDUTY Integrative	Contains PID coefficient KDUTY_INTEGRATIVE. Max value is 0x3F.	Integer Unsigned	
2:0	KDUTY[2:0]	Contains PID coefficient KDUTY. KDUTY[2:0] [# of 0.195% Steps]; max = 50%, 0d = OFF. Duty cycle value above which the correction engages. 5 remaining bits are stored into MFR_KK_FEEDFRWD_CTRL.	Integer Unsigned	

MFR_LOCK (0xDB)
Description: Locks the access to Low Level commands. Needs WRITE_PROTECT to be set accordingly.

MFR_FAULT_CONFIG (0xDC)
Description: Used to set up the FAULT# pin behavior. 0b = The event do NOT trigger the FAULT# pin assertion. 1b = The event triggers the FAULT# pin assertion.

Bit	Function	Description	Value	Description
10	PUC Error	PUC Error.	1	Trigger enabled
			0	Trigger blocked
9	Vin Over-Voltage Fault	Vin Over-Voltage Fault.	1	Trigger enabled
			0	Trigger blocked
8	VSRMON peak fault	VSRMON pin peak fault.	1	Trigger enabled
			0	Trigger blocked
7	Vout Over-Voltage Fault (HW)	Vout Over-Voltage Fault (HW).	1	Trigger enabled
			0	Trigger blocked
6	Iout Over-Current Fault (HW)	Iout Over-Current Fault (HW)	1	Trigger enabled
			0	Trigger blocked
5	Catastrophic Fault	Catastrophic Fault.	1	Trigger enabled
			0	Trigger blocked
4	Vput Over-Voltage Fault (HW)	Vput over-voltage Fault (HW).	1	Trigger enabled
			0	Trigger blocked
3	Pout Over-power Fault	Pout Over-power Fault.	1	Trigger enabled
			0	Trigger blocked
2	Feedback disconnection fault	Feedback disconnection fault.	1	Trigger enabled
			0	Trigger blocked
1	Vin Under-voltage Fault	Vin under voltage Fault.	1	Trigger enabled
			0	Trigger blocked
0	Over-Temperature Fault	Over-temperature fault.	1	Trigger enabled
			0	Trigger blocked

MFR_IMON (0xDE)
Description: Mfr Imon.

Bit	Description	Format
5:0	Used to define RIMON/RG ratio from 2.678 to 174.120 in 64 steps; RIMON/RG = 2.678571 * (MFR_IMON + 1), RG=~560 Ohm. Peak OCP limit is impacted as PEAK_OCP = 2.1 / IMONx2 / DCReq / (RIMON/RG) where IMONx2 is given by System Register IMONX2 (OCP is triggered when the drop across RIMON reaches 2.1V). Impacts also READ_IOUT reporting.	Fixed Point Unsigned

MFR_STORE_MAP (0xDF)
Description: Stores the NVM content into RAM, as happens during device initial startup.

MFR_RESTORE_MAP (0xE0)
Description: Restores the NVM content into RAM, as happens during device initial startup.

MFR_CATASTROPHIC_FAULT_LIMIT (0xE1)
Description: Not used since no power loss calculation. Sets catastrophic power loss fault threshold. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = 0 (0b00000).

Bit	Description	Format	Unit
9:0	LSB = 1 W.	Fixed Point Unsigned	W

MFR_CATASTROPHIC_FAULT_RESPONSE (0xE2)
Description: Sets the catastrophic power fault response.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

MFR_CS_CELL_WARN_LIMIT (0xE3)
Description: Sets the warning limit for current sharing unbalance between two phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -2 (0b11110).

Bit	Description	Format	Unit
5:0	LSB = 0.25 A.	Fixed Point Unsigned	A

MFR_CELL_CONFIG (0xE4)
Description: Used to define the number of phases in design.

Bit	Description	Value	Function	Description
2:0	Number of phases/modules in design.	000	1 phase	Control Assembly + 1 PowerBlade.
		001	2 phases	Control Assembly + 2 PowerBlade.
		010	3 phases	Control Assembly + 3 PowerBlade.

MFR_OV_LIMIT_OFFSET (0xE5)
Description: MFR_OV_LIMIT_OFFSET.

Bit	Description	Format	Unit
2:0	Used to program the VOUT reference over voltage threshold as positive offset from 50mV (0x00) to 400mV (0x07) in 50mV steps. OV threshold is set above the commanded Vout setpoint, regardless of the voltage positioning offset (droop).	Fixed Point Unsigned	ΔmV

MFR_UV_LIMIT_OFFSET (0xE6)
Description: MFR_UV_LIMIT_OFFSET.

Bit	Description	Format	Unit
2:0	Used to program the VOUT under voltage threshold as negative offset from 50mV (0x00) to 400mV (0x07) in 50mV steps. UV threshold is set below the commanded setpoint considering the voltage positioning offset (droop).	Fixed Point Unsigned	ΔmV

MFR_VBOOT_SET (0xE7)
Description: MFR_VBOOT_SET.

Bit	Description	Format	Unit
9:0	Used to define VBOOT to which the device regulate after receiving valid enable. [VID] data need to be compliant with format specified in VOUT_MODE. This is the default boot voltage in SVI Mode (Reg26h) and AVS Mode (when OPERATION is set accordingly).	Fixed Point Unsigned	V

MFR_SVI_PMBUS_SELECT (0xE8)
Description: Switch ON (0x01) or OFF (0x00) the Vout control on PMBus domain. In AVS mode this command is NACKed.

Bit	Description	Value	Function	Description
0	[0]: 0b0 = CPU-Link / 0b1 = PMBus"	0	SVID Bus	SVID CPU-Link
		1	PMBus	PMBus

MFR_ICC_MAX_ADD (0xE9)
Description: Additional bytes to standard SVID commands. Formatted per CPU-link definition. LSB = 2A. Check HC_SUPPORT for further info.

Bit	Description	Format
7:0	MFR_ICC_MAX_ADD [A].	Integer Unsigned

MFR_PWR_IN_MAX_ADD (0xEA)
Description: Additional bytes to standard SVID commands. Formatted per CPU-link definition. LSB = 4W. Check HC_SUPPORT for further info.

Bit	Description	Format
7:0	MFR_PWR_IN_MAX_ADD [W].	Integer Unsigned

MFR_PWR_IN_ALERT_ADD (0xEB)
Description: Additional bytes to standard SVID commands. Formatted per CPU-link definition. LSB = 4W. Check HC_SUPPORT for further info.

Bit	Description	Format
7:0	MFR_PWR_IN_ALERT_ADD [W].	Integer Unsigned

MFR_READ_PIN_PUC (0xEF)
Description: Used to read the Input Power communicated through PuC interface, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	LSB=1W.	Linear	W

MFR_READ_VIN_PUC (0xF0)
Description: Used to read the Input voltage communicated through PuC interface, value averaged over configured MFR_AVERAGE_TIME_SCALE.

Bit	Description	Format	Unit
15:0	LSB=0.125 V.	Linear	V

MFR_DPM1_THR (0xF1)
Description: Sets the phase shedding; phase 1 to 2 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -2 (0b11110). bill modify

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_DPM2_THR (0xF2)
Description: Sets the phase shedding; phase 2 to 4 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_DPM3_THR (0xF3)
Description: Sets the phase shedding; phase 3 to 4 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_DPM4_THR (0xF4)
Description: Sets the phase shedding; phase 4 to 5 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_DPM5_THR (0xF5)
Description: Sets the phase shedding; phase 5 to 6 threshold. Offset by DPM_OFFSET to compensate for current ripple. Real-time current used to increase # of phases, time averaged current used to reduce # of phases. Can be handled as Linear format when reading, and also when writing if bits(15:11) = exponent = -1 (0b11111).

Bit	Description	Format	Unit
9:0	LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

MFR_FSWITCH_PROTECT_COEFF (0xF6)
Description: Resonant Loop Only. Used to configure FSW protection during ACLL. Enabled/Disabled through sys reg DISABLE_DPM_PROT

Bit	Description	Format
3:0	FSW_AVG computed as the average frequency of the previous [16 - FSW_AVGd] cycles. 0x01 = 15 cycles; 0x0F = 1 cycles; 0x00 = 0 cycles.	Integer Unsigned

MFR_CS_PROP_INTEGR (0xF7)
Description: Sets Proportional (Kp) and Integral (Ki) correction for Active Current Sharing. In resonant topologies: In order to enable the feature you need to set Ki to 1 or more. The higher value, the faster the regulator recovers current balancing after a load (or number of turned on phases) change. Leave Kp=0. Algorithm: when a phase current is less than average value of load/number of phases, then PWMx to START delay is increased. In non-resonant topologies (PSFB): In order to enable the feature you need to set Kp to 1 or more. The higher value, the faster the regulator recovers current balancing after load (or number of turned on phases) change. Leave Ki=0. Algorithm: when a phase current is less than average value of load/number of phases, then PWMx to PWMy time width is increased.

Bit	Function	Description	Format

Bit	Function	Description	Format
13:7	Current Sharing Loop - Ki	Integral correction for active current sharing	Integer Unsigned
6:0	Current Sharing Loop - Kp	Proportional correction for active current sharing	Integer Unsigned

MFR_T_START_PH_SHIFT_DELTA_DELAY (0xF8)
Description: TPHASESHIFT_CORRECTION: increases the programmed TSHIFT during DVID_Down to control the secondary phases bump amplitude - to be used only in resonant topologies. DELTADELAY is used to optimize ZCD1 (i.e. PSKIP and turnOFF procedures - It delays the START1 transition to HiZ) Default is 0nSec (0x08). TSTART and TSHIFT are to be configured according to the resonant or non-resonant mode selected. TSHIFT and TPHASESHIFT_CORRECTION can be offset by further 12.5nSec according to System Register HIGH_CURR_PROT_EN. TSHIFT cannot be programmed to 12.5nSec or 37.5nSec in non resonant PSFB.

Bit	Function	Description	Format	Unit
35:31	Tphase-Shift Correction (base)	TPHASESHIFT_CORRECTION in number of 25 ns steps. (Active during DVID_Down, summed to TPHASE_SHIFT) Another 12.5 ns can be added by HIGH_CURR_PROT_EN[6].	Fixed Point Unsigned	ns
28:25	Delta Delay	DELTA_DELAY in number of 25 ns steps.	Fixed Point Unsigned	ns
24:9	Tstart	T start in number of 0.195ns steps.	Fixed Point Unsigned	ns
8:0	Tshift (base)	T shift in number of 25 ns steps. Another 12.5 ns can be added by HIGH_CURR_PROT_EN[6].	Fixed Point Unsigned	ns

Bit	Function	Description	Value	Description
30	Reserved (Low Power Enable)	STRG04_LOW_POWER_ENABLE (Pattern on PWMX) - Reserved, set to 0b.	0	Disable
			1	Enable
29	Reserved (Predictive Disable)	STRG04_PREDICTIVE_DISABLE (Pattern on PWMY) - Reserved, set to 1b.	0	Enable
			1	Disable

MFR_KK_FEEDFRWD_GAIN_CTRL (0xF9)
Description: Setups Input Voltage Feed-Forward Compensation. It also allow to setup other parameters. K Feed Forward: It is the input voltage FeedForward Gain for resonant topologies. As default value, it is an integer number which value is =(Tsw_noload*VOUT/VIN*1000) where Tsw_noload is the switching period of one secondary phase at no load in uSeconds. KDUTY sets the duty cycle value above which the TSTART correction applies (See MFR_DUTY_PARAMETER). Note. kDUTY is 8 bit wide and split between this command and MFR_KK_FEEDFRWD_GAIN_CTRL. Enable Ph Order: Enables/disables phase order memory during load transients. V_ERR_CLAMP_SOFTSTART: Used to override ErrorClamp setting (active only during SoftStart). Enable Memory: Enables Pulse memory during ACLL. If the VCO drives more pulses during the current Pulse, these are memorized and fired after the current Pulse has elapsed. K_GAIN_CTRL. Defines the bandwidth of the feed forward loop.

Bit	Function	Description	Format
42:24	K Feed Forward	Feed forward constant, integer. As default value, calculate it as (Tsw_noload*VOUT/VIN*1000) where Tsw_noload is the switching period of one secondary phase at no load in useconds.	Integer Unsigned
23:19	KDUTY[7:3]	KDUTY[7:3][# of 0.195% Steps]; max = 50%, 0d = OFF. Duty cycle value above which the correction engages. 3 remaining bits are stored in MFR_DUTY_PARAMETER.	Integer Unsigned
15:10	V_ERROR_CLAMP_SOFTSTART	Override ErrorClamp setting (active only during SoftStart). LSB = 2mV; => VerrClamp = 2mV * (63 - CTRL_VERR_CLAMP) 128m (0x00) to OFF; max 126mV (0x01).	Integer Unsigned
7:0	K_GAIN_CTRL	Sets K_GAIN_CTRL, the FeedForward Gain. Set to 0x01.	Integer Unsigned

Bit	Function	Description	Value	Description
18	Enable Ph Order On	Phase Order On Enable. 0x01 = Enable sequential; 0x00 = Disables Sequential (=Shuffle).	0xb1	Enabled.
			0xb0	Disabled.
17	Enable Err Clamp Pre	Error Clamp Pre. Reserved, need to be 1 (enabled).	0xb1	Enabled.
			0xb0	Disabled.

Bit	Function	Description	Value	Description
16	Enable Integrative During Phase Memory On	Integrative During Phase Memory On Enable. Reserved, need to be 1 (enabled).	0xb1	Enabled.
			0xb0	Disabled.
9	Secure Off Enable	Secure Off Enable. Reserved, need to be 1 (enabled).	0xb1	Secure Off enabled.
			0xb0	Secure Off disabled.
8	Enable Memory	Enables pulse memory during ACLL.	0xb1	Pulse memory during ACLL enabled.
			0xb0	Pulse memory during ACLL disabled.

MFR_VOUT_TRIM (0xFA)
Description: Mfr Vout Trim

Bit	Description	Format	Unit
7:0	Sets Mfr VOUT trim value. Applies a fixed offset voltage to the value set by VOUT_COMMAND (in # of VID steps). [# of VID]. Applied only in PMBus Domain. # of VID steps to add or remove from setpoint. In AVS mode, if applied, need to be in tracking with EXTRA_OFFSET.	Integer Signed	VID steps

MFR_MANUAL_CELL_SHED (0xFB)
Description: Sets DPM_NPH_PS00, DPM_NPH_PS01 and DPM_NPH_PS02 which are the minimum # of phases for Intel VR power states PS00, PS01 and PS02. Unless otherwise commanded by SVID interface, PS00 power state is used. If trying to set a min # phases higher than # of phases set by MFR_CELL_CONFIG, the write will have no effect and the Unsupported Data bit in STATUS_CML is set.

Bit	Function	Description	Format
9:6	OFFSET_FRACT	Optimizes PSKIP behavior	Integer Unsigned

Bit	Function	Description	Value	Function	Description
12:10	Min # of phases (PS02-SVID)	Minimum # of phases for power state PS02 (Intel VR/SVID only).	001	Min 1 phase	
			010	Min 2 phases	
			011	Min 3 phases	
			100	Min 4 phases	
			101	Min 5 phases	
			110	Min 6 phases	
5:3	Min # of phases (PS01-SVID)	Minimum # of phases for power state PS01 (Intel VR/SVID only).	001	Min 1 phase	
			010	Min 2 phases	
			011	Min 3 phases	
			100	Min 4 phases	
			101	Min 5 phases	
			110	Min 6 phases	
2:0	Min # of phases (PS00)	Minimum # of phases for power state PS00 (default).	001	Min 1 phase	
			010	Min 2 phases	
			011	Min 3 phases	
			100	Min 4 phases	
			101	Min 5 phases	
			110	Min 6 phases	

MFR_SVID_TEMPZONE (0xFE02)
Description: SVID Temperature Zone Register (reg12h). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_IOUT (0xFE03)
Description: SVID Output Current Register (reg15h). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_VIDSETTING (0xFE04)
Description: Last VID code commanded, i.e. actial regulation setpoint. Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
9:0		Integer Unsigned

MFR_SVID_PWRSTATE (0xFE05)
Description: Last PWRState Commanded. Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_OFFSET (0xFE06)
Description: SVID Commanded Offset (reg33h). See System Register CRC_SPI_EN for additional information. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_START_THREAD (0xFE07)
Description: When sent, IC starts to compute the total power delivered. Average Power delivered in 1.2 mSec interval is progressively added until the max time programmed T_THREAD = 1.2mSec * MFR_START_THREAD"

Bit	Description	Format	Unit
19:0	Number of 1 mSec interval to collect the measure on. Max 1,048,576 => 20.97min. Unit in ms.	Fixed Point Unsigned	ms

MFR_SVID_ICCMAX (0xFE08)
Description: ICCMAX Register (reg21h). This is not linked to OC protection in any way. Write unlocked by MFR_SVID_REGLOCK

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_TEMPMAX (0xFE09)
Description: TMAX Register (reg22h). This is not linked to OT protection in any way. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_SRFAST (0xFE0A)
Description: Slew Rate Fast (reg24h). Write unlocked by MFR_SVID_REGLOCK. This is for CPU-Link reading only. Actual slew rate is set through System Register DVID_SR_FAST_STEP.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_SRSLOW (0xFE0B)
Description: Slew Rate Slow (reg25h). Write unlocked by MFR_SVID_REGLOCK. This is for CPU-Link reading only. Actual slew rate is set through System Register DVID_SR_SLOW_STEP.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_MULTI_VR_CONFIG (0xFE0C)
Description: SVID Multi VR Config (reg34h). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
1:0		Integer Unsigned

MFR_SVID_VOUTMAX (0xFE0D)
Description: VOUTMAX (reg30h). Write unlocked by MFR_SVID_REGLOCK

Bit	Description	Format	Unit
7:0	Formatted as per CPU-Link definition LSB=5mV based on VR_TAB_RAIL(0X01) LSB=10mv based on VR_TAB_RAIL(0X00) VALUE=LSB*bitfield value + 0.49	Fixed Point Unsigned	V

MFR_SVID_SLOW_SR_SELECTOR (0xFE0E)
Description: Select SVID SR Slow range as fraction of SVID SR Fast range. Write unlocked by MFR_SVID_REGLOCK. It affects real slew rate as programmed by System Registers DVID_SR_FAST_STEP and DVID_SR_SLOW_STEP. Setting of VR13.1 HC options.

Bit	Function	Description	Value	Function	Description
7	Enable HC support	Configures VR13.HC support Can only be written directly to NVM, read-only in RAM! 0b0: VR13 Protocol support. Exponent for Iout and Pout read/settings and TEL_IOUT_FSR is set by IOUT_EXP. Registers PWR_IN_MAX_ADD and PWR_IN_ALERT_ADD are ignored. 0b1: VR13.HC Protocol support. Iout exponent = -1 (LSB=0.5A), Pout exponent = 1 (LSB=2W), TEL_IOUT_FSR exponent = 1 (LSB=2A), regardless of HC active or not. Registers PWR_IN_MAX_ADD and PWR_IN_ALERT_ADD are supported according to VR13.HC specs. The following commands are affected by the exponent setting: IOUT_OC_FAULT_LIMIT. IOUT_OC_WARN_LIMIT. POUT_OP_FAULT_LIMIT. READ_IOUT. READ_POUT. MFR_DPM1_THR. MFR_DPM2_THR. MFR_DPM3_THR. MFR_DPM4_THR. MFR_DPM5_THR. MFR_READ_PIN_POUT. TEL_IOUT_FSR. DPM_HYSTERESIS.	1	HC supported	HC supported
6	Activate HC	Pre-sets the HC_ACTIVE bit	1		HC activated

Bit	Function	Description	Value	Function	Description
		supposed to be commanded through the SVI interface. Can only be written directly to NVM, read-only in RAM! 0b0: HC mode not active. The device behaves as a VR13 controller. -> DEFAULT. ICCMAX = MFR_SVID_ICCMAX [A]. PIN_MAX = MFR_SVID_PIN_MAX*2 [W]. PIN_ALERT_THRESHOLD = MFR_SVID_PIN_ALERT_THR*2 [W]. 0b1: HC mode active. ICCMAX = MFR_SVID_ICCMAX + MFR_ICC_MAX_ADD*2 [A]. PIN_MAX = MFR_SVID_PIN_MAX*2 + MFR_PWR_IN_MAX_ADD*4 [W]. PIN_ALERT_THRESHOLD = MFR_SVID_PIN_ALERT_THR*2 + MFR_PWR_IN_ALERT_ADD*4 [W].	0		HC not activated
3:0	Slow vs fast slew rate range FRACTION	0x01 = 1/2; 0x02 = 1/4; 0x04 = 1/8; 0x08 = 1/16 Others are rejected"	0x01	1/2	
			0x02	1/4	
			0x04	1/8	
			0x08	1/16	

MFR_SVID_PIN_MAX (0xFE0F)
Description: PINMAX (reg2Eh). Used to set the PIN protection threshold. Set threshold to max allowable to disable the protection. Write unlocked by MFR_SVID_REGLOCK. Formatted per CPU-link definition. LSB = 2W.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_PIN_ALERT_THR (0xFE10)
Description: Used to set the PIN protection ALERT threshold. Set threshold to max allowable to disable the warning signal. Write unlocked by MFR_SVID_REGLOCK. Formatted per CPU-link definition. LSB = 2W.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP0 (0xFE11)
Description: SVID Working point #0 (reg3Ah). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP1 (0xFE12)
Description: SVID Working point #1 (reg3Bh). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP2 (0xFE13)
Description: SVID Working point #2 (reg3Ch). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP3 (0xFE14)
Description: SVID Working point #3 (reg3Dh). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SVID_WP4 (0xFE15)
Description: SVID Working point #4 (reg3Eh). Not stored in NVM. Formatted as per CPU-link definition. Write unlocked by MFR_SVID_REGLOCK.

Bit	Description	Format
7:0		Integer Unsigned

MFR_RD_TEMPERATURE_PHASE1 (0xFE16)
Description: Reads the temperature for Phase 1. Reporting is active only when Phase 1 is switching.

Bit	Description	Format	Unit
15:0	Phase 1 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE2 (0xFE17)
Description: Reads the temperature for Phase 2. Reporting is active only when Phase 2 is switching.

Bit	Description	Format	Unit
15:0	Phase 2 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE3 (0xFE18)
Description: Reads the temperature for Phase 3. Reporting is active only when Phase 3 is switching.

Bit	Description	Format	Unit
15:0	Phase 3 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE4 (0xFE19)
Description: Reads the temperature for Phase 4. Reporting is active only when Phase 4 is switching.

Bit	Description	Format	Unit
15:0	Phase 4 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE5 (0xFE1A)
Description: Reads the temperature for Phase 5. Reporting is active only when Phase 5 is switching.

Bit	Description	Format	Unit
15:0	Phase 5 temperature.	Linear	°C

MFR_RD_TEMPERATURE_PHASE6 (0xFE1B)
Description: Reads the temperature for Phase 6. Reporting is active only when Phase 6 is switching.

Bit	Description	Format	Unit
15:0	Phase 6 temperature.	Linear	°C

MFR_CTRL_ID (0xFE1C)
Description: Used to read controller internal reference code.

Bit	Description	Format
15:0	Used to read controller internal reference code.	Byte Array

MFR_READ_CURR_MISMATCH (0xFE1D)
Description: Returns the output current mismatch between the phase with min current and the phase with max current in a multiphase setup. The value is momentary and will be valid only if more than one phase is active. Command MFR_CELL_MISMATCH_MIN_MAX provides information about which phases had min resp. max current.

Bit	Description	Format	Unit
15:0	LSB = 0.25 A.	Linear	A

MFR_SVID_REGLOCK (0xFE1E)
Description: CPU-Link registers are by default accessible only with read operations (locked). This command allows to lock (0x01) or unlock (0x00) access to these registers. This command is not stored in NVM but will be set to lock state (0x01) efter a RESTORE from NVM command (e.g. MFR_RESTORE_MAP).

Bit	Description	Value	Description
0		1	Protects SVID Registers
		0	Unprotects SVID Registers

MFR_SECT_L (0xFE20)
Description: 8 bytes low sector image data - Used to access read NVM data after writing MFR_SECT_RD or to write NVM data before writing MFR_SECT_WR. [63..56] = byte 00 ... [7..0] = byte 07.

Bit	Description	Format
63:0		Integer Unsigned

MFR_SECT_H (0xFE21)
Description: 8 bytes high sector image data - Used to access read NVM data after writing MFR_SECT_RD or to write NVM data before writing MFR_SECT_WR. [63..56] = byte 08 ... [7..0] = byte 15.

Bit	Description	Format
63:0		Integer Unsigned

MFR_SECT_RD (0xFE24)
Description: Copy from specified NVM sector (0x01 to 0x0E) into a register accessible by PMBus commands MFR_SECT_L and MFR_SECT_H.

Bit	Description	Format
7:0		Integer Unsigned

MFR_SECT_WR (0xFE25)
Description: Copy from register written by PMBus commands MFR_SECT_L and MFR_SECT_H into specified NVM sector (0x01 to 0x0E).

Bit	Description	Format
7:0		Integer Unsigned

MFR_MEMORY_WORD (0xFE26)
Description: 8 bytes - Data for read/write of specified RAM memory location (used by MFR_MEMORY_RD or MFR_MEMORY_WR). [63..56] = Base Address +7 ... [7..0] = Base Address as specified into MFR_MEMORY_RD, MFR_MEMORY_WR.

Bit	Description	Format
63:0		Integer Unsigned

MFR_MEMORY_RD (0xFE27)
Description: 3 bytes - Used to copy 8 bytes of the specified RAM memory location into PMBusTM accessible register, read by MFR_MEMORY_WORD. Byte 1 [7:0] : RAM address low byte. Byte 2 [15:8]: RAM address high byte. Byte 3 [23:16]: Source. 0x00 to read from RAM. Other combinations are reserved. Protected by MFR_UNLOCK.

Bit	Description	Format
23:0		Integer Unsigned

MFR_MEMORY_WR (0xFE28)
Description: "4 bytes - Used to copy the content of PMBusTM accessible registers, written to MFR_MEMORY_WORD, into the specified RAM memory location. Byte 1 [7:0] : RAM address low byte. Byte 2 [15:8] : RAM address high byte. Byte 3 [23:16]: Source. 0x00 to read from RAM. Other combinations are reserved. Byte 4 [31:24]: Number of bytes to be written, 1 to 8. Other combinations are reserved. Protected by MFR_UNLOCK.

Bit	Description	Format
31:0		Integer Unsigned

MFR_READ_BLACKBOX (0xFE29)
Description: NVM BBR Access. Used to copy the content of NVM that contains BBR data into accessible PMBusTM register MFR_BLACKBOX.

MFR_BLACKBOX (0xFE2A)
Description: NVM BBR Access - Shadow register containing the BBR NVM Sector being read. Status Register array is reported before and after the BBR trigger.

Bit	Function	Description	Value	Description
125	After trigger - VSRMON peak fault		0	
			1	
124	After trigger - PATCH_DOWNLOAD		0	
			1	
123	After trigger - MEM_FAULT		0	
			1	
122	After trigger - POUT_OP_FAULT		0	
			1	
121	After trigger - DATACMD_RCV_FAULT		0	
			1	
120	After trigger - IOUT_OC_WARN		0	
			1	
115	After trigger - CATASTROPHIC_FAULT		0	
			1	
114	After trigger - VIN_UV_FAULT		0	
			1	
113	After trigger - VIN_OV_FAULT		0	
			1	
112	After trigger - PUC_CRC_FAULT		0	
			1	
110	After trigger - CURR_SHARE_WARN		0	
			1	
103	After trigger - OFF		0	
			1	
102	After trigger - VOUT_OV_FAULT		0	
			1	
101	After trigger - VOUT_UV_FAULT		0	
			1	
100	After trigger - IOUT_OC_FAULT		0	
			1	
99	After trigger - Feedback disconnection		0	
			1	
98	After trigger - VOUT_MAX_WARNING		0	
			1	
97	After trigger - OT_FAULT		0	
			1	
96	After trigger - OT_WARNING		0	
			1	

Bit	Function	Description	Value	Description
93	Before trigger - VSRMON peak fault		0	
			1	
92	Before trigger - PATCH_DOWNLOAD		0	
			1	
91	Before trigger - MEM_FAULT		0	
			1	
90	Before trigger - POUT_OP_FAULT		0	
			1	
89	Before trigger - DATACMD_RCV_FAULT		0	
			1	
88	Before trigger - IOUT_OC_WARN		0	
			1	
83	Before trigger - CATASTROPHIC_FAULT		0	
			1	
82	Before trigger - VIN_UV_FAULT		0	
			1	
81	Before trigger - VIN_OV_FAULT		0	
			1	
80	Before trigger - PUC_CRC_FAULT		0	
			1	
78	Before trigger - CURR_SHARE_WARN		0	
			1	
71	Before trigger - OFF		0	
			1	
70	Before trigger - VOUT_OV_FAULT		0	
			1	
69	Before trigger - VOUT_UV_FAULT		0	
			1	
68	Before trigger - IOUT_OC_FAULT		0	
			1	
67	Before trigger - Feedback disconnection		0	
			1	
66	Before trigger - VOUT_MAX_WARNING		0	
			1	
65	Before trigger - OT_FAULT		0	
			1	
64	Before trigger - OT_WARNING		0	
			1	

MFR_CLEAR_BB (0xFE2B)
Description: Clear the content of NVM that contains BBR data.

MFR_CONFIG_BBR (0xFE2C)
Description: "Select which events trigger the writing of the BBR in NVM. Set 1b to enable event to trigger BBR, 0b to disable."

Bit	Function	Description	Value	Description
11	PUC_CRC_FAULT		0	Do not trigger on fault
			1	Trigger event on fault
10	Feedback disconnection fault		0	Do not trigger on fault
			1	Trigger event on fault
9	VSRMON peak fault		0	Do not trigger on fault
			1	Trigger event on fault
8	VOUT_OV		0	Do not trigger on fault
			1	Trigger event on fault
7	IOUT_OC		0	Do not trigger on fault

Bit	Function	Description	Value	Description
			1	Trigger event on fault
6	CATASTROFIC FAULT		0	Do not trigger on fault
			1	Trigger event on fault
5	VOUT Under Voltage Fault		0	Do not trigger on fault
			1	Trigger event on fault
4	Over Output Power Fault		0	Do not trigger on fault
			1	Trigger event on fault
3	Current Sharing Unbalance Warning		0	Do not trigger on fault
			1	Trigger event on fault
2	VIN OV Fault	VIN Over Voltage Fault	0	Do not trigger on fault
			1	Trigger event on fault
1	VIN UV Fault	VIN Under Voltage Fault	0	Do not trigger on fault
			1	Trigger event on fault
0	Over Temperature Fault	Over Temperature Fault	0	Do not trigger on fault
			1	Trigger event on fault

MFR_PROTECT_DEFAULT (0xFE2E)
Description: Protects non volatile memory from writing by inhibiting commands STORE_DEFAULT_ALL and MFR_STORE_MAP. In case, the PMB_ALRT# signal is asserted and “other ML flag” bit is STATUS_CML register is set. 0x00 = Unprotected; 0x01 = Protected.

Bit	Description	Value	Description
0	[7:1]: Don't Care [0]: 0b0 = Unprotected; 0b1 = Protected	0	Unprotected
		1	Protected

MFR_POUT_THREAD (0xFE2F)
Description: When sent, stops the computation started with MFR_START_THREAD and returns the total energy delivered in the programmed time (max 1GW).

Bit	Description	Format	Unit
31:0	LSB weight is given by System Register IOUT_EXP.	Integer Unsigned	Wms

MFR_PMBUSCFG_REVISION (0xFE30)
Description: Can be used for user/custom data.

Bit	Description	Format
15:0	Can be used for user/custom data.	Byte Array

MFR_PMBUSCFG_TIMESTAMP (0xFE31)
Description: Contains product number and revision information.

Bit	Function	Description	Format
59:50	BMR Family Number	Number 000-999.	Integer Unsigned
49:46	X1 Variant	Number 0-9.	Integer Unsigned
45:42	X2 Variant	Number 0-9.	Integer Unsigned
41:38	X3 Variant	Number 0-9.	Integer Unsigned
37:34	X4 Variant	Number 0-9.	Integer Unsigned
22:17	Product Revision Number	Number 0-63.	Integer Unsigned
16:12	Product Revision Letter	Number where 1-26 represent A-Z.	Integer Unsigned
10:6	Configuration Revision	Number where 1-26 represent A-Z.	Integer Unsigned

Bit	Function	Description	Value	Description
23	Preliminary Revision	0=Non-preliminary revision (e.g. R1A), 1=Preliminary revision (e.g. P1A).	0	Non-preliminary revision (e.g. R1A)

Bit	Function	Description	Value	Description
			1	Preliminary revision (e.g. P1A)

MFR_PEAK_FAULT_RESPONSE (0xFE32)
Description: Used to configure how to respond to a peak fault read through VSRMON pin. When enabled, fault is set if VSRMON pin > 3.045V.

Bit	Description	Value	Function	Description
7:0	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers. Only 0x00 (Fault Ignored) and 0x80 (Latched) are implemented.	0x00	Ignore Fault	Continue operation without interruption.
		0x80	Latch	Immediate and definite shutdown of output voltage until fault is cleared and the output voltage is re-enabled.

MFR_PMBUSCFG_USERID (0xFE33)
Description: Can be used for user/custom data.

Bit	Description	Format
15:0	Can be used for user/custom data.	Byte Array

System Registers Details

K_TRANSIENT (0xA407)

Bit	Description	Format
7:0	Used to correct TSTART Correction adjustments during ACLL. Must be set to 0x00.	Fixed Point Unsigned

CURRENT_SHARING_RESET (0xA408)

Bit	Function	Description	Format
5:0	Activation threshold	Activation threshold for current sharing reset. 0x00=126mV, 0x01=124mV, 0x02=122mV, ... , 0x26=50 mV, ... , 0x3D=4mV, 0x3E=2mV, 0x3F=0 mV.	Byte Array

Bit	Function	Description	Value	Function	Description
7	Enable current sharing Reset	For resonant mode only. Enable Current sharing Reset. Needed in case of heavy load transient release to suddenly reduce the TSTART signal delay vs PWMx, in order to avoid secondary phases overvoltage. Adjusts the current sharing correction (dividing its correction /2 or /4) when the current sharing error exceeds a programmable threshold in order to optimize load release.	0		Disable
			1		Enabled
6	Correction division	Dividing correction for current sharing reset.	0	Divide with 2	Divide with 2.
			1	Divide with 4	Divide with 4.

HIGH_CURR_PROT_EN (0xA40B)

Bit	Function	Description	Value	Function	Description
7	Add 12.5 ns to base Tshift correction	Adds 12.5 ns to the base Tshift correction set by MFR_T_START_PH_SHIFT_DELTA_DELAY[35:31].	0		Do not add 12.5 ns
			1		Add 12.5 ns
6	Add 12.5 ns to base Tshift	Adds 12.5 ns to the base Tshift set by MFR_T_START_PH_SHIFT_DELTA_DELAY[8:0]. Cannot be 0 (do not add 12.5 ns) in Resonant application if NCHECKS = 0x00. Cannot be 1 (add 12.5 ns) in NonResonant PSFB if TPHASE_SHIFT = 0nSec or 25nSec.	0		Do not add 12.5 ns
			1		Add 12.5 ns
5	Enable one Phase gain reduction	GAIN_REDU_1PH_EN. Reduces by 1/2 the control loop gain when working in single phase.	0		Disable
			1		Enabled
4	Enable soft start gain reduction	GAIN_REDU_SS_EN. Reduces by 1/2 the control loop gain during SoftStart.	0		Disable
			1		Enabled
3	Enable TGB hysteresis		0		Disable
			1		Enabled
2	Current sharing correction storage.	Enables/disables current sharing correction to be memorized when shedding phases. Reserved, set to 0x01 (not stored).	0	Correction stored	
			1	Correction not stored	
1	AVSBus current monitor	0b0: EXP = -2; 0b1: EXP = -1	0	EXP = -2	EXP = -2
			1	EXP = -1	EXP = -1
0	Enable High Current Protection	Reserved, set to 0 (disabled).	0		Disable
			1		Enabled

AVS_CONFIG (0xA40D)

Bit	Function	Description	Value	Function	Description
3	SDATA release method	Controls when SDATA is released (open) at the end of a frame. 0x00: As per protocol at CLK edge (rising). 0x01: Data line release 1/2 CLK in advance (CLK falling edge).	0	At CLK edge (per protocol)	
			1	1/2 CLK in advance	
2	Do not produce response to wrong address	Controls the response to command with address that doesn't match VRM address. 0x00: Response is produced; 0x01: No Response.	0		Disable
			1		Enabled
1	Do not produce status response	Controls the production of status response frame and response to broadcast commands. 0x00: Response is produced; 0x01: No Response.	0		Disable
			1		Enabled
0	Do not produce interrupt over data line	Controls interrupt produced from the interface in case of OC OT on DAT line of the interface. 0x00: Interrupt is produced over data line; 0x01: No interrupt is produced.	0		Disable
			1		Enabled

FBCOT_TSWITCH_MAIN_NOM (0xA40E)

Bit	Description	Format	Unit
8:0	Sets switching frequency by defining the switching period. Applicable for non-resonant operation. LSB=25 nsec, make double for fullbrige.	Fixed Point Unsigned	us

FBCOT_CONST_FEED_FWD_NVM (0xA410)

Bit	Description	Format
10:0	This constant is used to calculate the TPHASE_SHIFT. Considered only if FBCOT_MIXED[7] = VIN_FF_EN = 0x0. Value should be set to (41943.04 * NTRAFO) / (VIN*2^3). For non-resonant operation.	Fixed Point Unsigned

FBCOT_MIXED (0xA412)

Bit	Function	Description	Value	Function	Description
7	Feedforward enabled (non-resonant)	Feedforward disabled: TPHASE_SHIFT (Ton) is generated according to CONST_FEED_FWD_NVM. Feedforward enabled: TPHASE_SHIFT (Ton) is generated according to reported Vin value.	0		Disabled
			1		Enabled
2	Full bridge operation mode		0	Resonant	-
			1	Non-resonant	_
1:0	FLL max correction (non-resonant)	For non-resonant operations, specifies the max correction that FLL can do.	00	+/- TPHASE_SHIFT	_
			01	+/- TPHASE_SHIFT/2	_
			10	+/- TPHASE_SHIFT/4	_
			11	No limit	_

FBCOT_T_SWITCH_C (0xA413)

Bit	Description	Format
9:0	FLL loop gain for non-resonant operation.	Fixed Point Unsigned

FBCOT_INV_MOD_INDEX (0xA415)

Bit	Description	Format
8:0	T_switching modulation speed for non-resonant operation. LSB = 2^21 x 25 ns. Reserved, set to 0x0000.	Fixed Point Unsigned

FBCOT_NTRAFO (0xA417)

Bit	Description	Format
6:0	Transformer turn ratio for non-resonant operation. LSB = 1 turn.	Fixed Point Unsigned

HIZ_HALFB_SYMMETRIC (0xA418)

Bit	Function	Description	Value	Function	Description
5	SFAS displacement	Current reading Chopper Amplifiers Control. Configures which phase shift is applied once enabled by SFAS. Reserved, set to 0x01.	0	12.5 ns	_
			1	25 ns	_
4	SFAS enable	Current reading Chopper Amplifiers Control. Enables phase shifting between the clock of the six chopper amplifiers. Reserved, set to 0x01.	0		Disabled
			1		Enabled
3	HiZ mode for PWM		0	PWMX/PWMY never HiZ	_
			1	PWMX/PWMY HiZ @ no operation	_
2	Symmetric mode		0	Asymmetric	_
			1	Symmetric	_
1	Bridge functionality		0	Full bridge	_
			1	Half bridge	_
0	Immediate (HiZ) or soft-off	When set, immediate off (HiZ) is used rather than soft-off when the output voltage is disabled. When set, also forces immediate off for all protection shutdowns. Because, in some cases, even if the immediate OFF is configured by OPERATION, the device is defaulting the behavior to soft-off. Vout OVP and OV peak protections by default always make a soft-off even if the OPERATION configures immediate OFF. This removes these default; it overrides and forces a real HiZ when stopping the operations after a FAULT event. For Vin UV/OV, Vout UV, Iout OC, over power and over temperature protections immediate off (HiZ) is always used and this bit has no impact.	0	Soft-off	Use the configured fall time (slew rate).
			1	Immediate off	Turn off the output and stop transferring energy to the output as fast as possible.

TSHIFT_MIN (0xA419)

Bit	Description	Format	Unit
3:0	Specifies the minimum TPHASE_SHIFT (Ton) for the regulation. For non-resonant operation. LSB = 1 CK cycle = 25 ns.	Fixed Point Unsigned	ns

CHOPPER_CLK_CONF (0xA41A)

Bit	Function	Description	Format
2:0	Modulation frequency	Reserved, set to 0x00.	Fixed Point Unsigned

Bit	Function	Description	Value	Function	Description
6:5	Maximum frequency FMAX	Reserved, set to 0x10 (6.6 MHz).	00	10 MHz	_
			10	6.6 MHz	_
			01	8 MHz	_
			11	5.7 MHz	_
4:3	# of frequency steps from FMAX	Reserved, set to 0x00 (no modulation).	00	No modulation	_
			10	3 frequency steps	_
			01	2 frequency steps	_
			11	4 frequency steps	_

SVID_IFC_CONF (0xB003)

Bit	Description	Value	Function	Description
5:0	Sets AVSBus or SVID bus mode and output voltage format. 5mV or 10mV DAC Step for SVID bus mode is selectable through VR_TAB_RAIL System register. When AVSBus is selected, OPERATION works as in PMBus rev1.3, DAC step is 5mV. Voltage commanded through AVS is truncated to the 5mV DAC. Warning: NOT SUPPOSED TO BE CHANGED WHILE SWITCHING. 0x00 = SVID (INTEL VR12.5 => VOUT_MODE = 0x23). 0x01 = SVID (INTEL VR13 => VOUT_MODE = 0x23). 0x02 = IBM => REJECTED. 0x03 = AVSBus => VOUT_MODE = 0x20. 0x04 = SVID (DDR VR12.5 => VOUT_MODE = 0x23). 0x05 = SVID (DDR VR13 => VOUT_MODE = 0x23). Other combinations are not supported. When a not supported combination is stored in NVM, device will boot in PMBus address 0x7C, highlighting MEMORY FAULT bit in STATUS_CML register and setting MFR_VBOOT_SET=0x00.	0000	SVID (VR12.5)	
		0001	SVID (VR13)	
		0011	AVSBus	
		0100	SVID (DDR VR12.5)	

CTRL_PFM_ENA_PS (0xB006)

Bit	Description	Value	Function	Description
1:0	Enable the PFM working mode vs power state.	00	PFM enabled in any PS	
		01	PFM enabled in PS01-03	
		10	PFM enabled in PS02-03	
		11	PFM disabled	

DPM_HYSTERESIS (0xB007)

Bit	Description	Format	Unit
7:0	Used to define the hysteresis for Phase Shedding. DPM_OFFSET may optimize the hysteresis settings. LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

DVID_SR_FAST_STEP (0xB00C)

Bit	Description	Value	Function	Description
5:0	Programs the [# of 25nSec] to step VOUT by 5mV. This setting actively drives the reference slew. dV/dt = 5mV / (SR_FAST_STEP * 25nSec) Actual fast	0x01	200 mV/us	
		0x02	100 mV/us	
		0x03	66.67 mV/us	

Bit	Description	Value	Function	Description
	slew rate (mV/us) = 200 / DVID_SR_FAST_STEP[5:0]. [7:6]: Don't Care [5:0]: SR_FAST_STEP. Values accepted from 0x01 to 0x3F. If 0x00, wraps to 0x3F.	0x04	50.00 mV/us	
		0x05	40.00 mV/us	
		0x06	33.33 mV/us	
		0x07	28.57 mV/us	
		0x08	25.00 mV/us	
		0x09	22.22 mV/us	
		0x0A	20.00 mV/us	
		0x0B	18.18 mV/us	
		0x0C	16.67 mV/us	
		0x0D	15.38 mV/us	
		0x0E	14.29 mV/us	
		0x0F	13.33 mV/us	
		0x10	12.50 mV/us	
		0x11	11.76 mV/us	
		0x12	11.11 mV/us	
		0x13	10.53 mV/us	
		0x14	10.00 mV/us	
		0x15	9.52 mV/us	
		0x16	9.09 mV/us	
		0x17	8.70 mV/us	
		0x18	8.33 mV/us	
		0x19	8.00 mV/us	
		0x1A	7.69 mV/us	
		0x1B	7.41 mV/us	
		0x1C	7.14 mV/us	
		0x1D	6.90 mV/us	
		0x1E	6.67 mV/us	
		0x1F	6.45 mV/us	
		0x20	6.25 mV/us	
		0x21	6.06 mV/us	
		0x22	5.88 mV/us	
		0x23	5.71 mV/us	
		0x24	5.56 mV/us	
		0x25	5.41 mV/us	
		0x26	5.26 mV/us	
		0x27	5.13 mV/us	
		0x28	5.00 mV/us	
		0x29	4.88 mV/us	
		0x2A	4.76 mV/us	
		0x2B	4.65 mV/us	
		0x2C	4.55 mV/us	
		0x2D	4.44 mV/us	
		0x2E	4.35 mV/us	
		0x2F	4.26 mV/us	
		0x30	4.17 mV/us	
		0x31	4.08 mV/us	
		0x32	4.00 mV/us	
		0x33	3.92 mV/us	
		0x34	3.85 mV/us	
		0x35	3.77 mV/us	
		0x36	3.70 mV/us	
		0x37	3.64 mV/us	
		0x38	3.57 mV/us	
		0x39	3.51 mV/us	
		0x3A	3.45 mV/us	
		0x3B	3.39 mV/us	
		0x3C	3.33 mV/us	
		0x3D	3.28 mV/us	
		0x3E	3.23 mV/us	
		0x3F	3.17 mV/us	

DVID_SR_SLOW_STEP (0xB00D)

Bit	Description	Value	Function	Description
5:0	Programs the [# of 25nSec] to step VOUT by 5mV. This setting actively drives the reference slew. Data computed over MFR_SVID_SLOW_SR_SELECTOR. Actual slow slew rate (mV/us) = FRACTION x 200 / DVID_SR_SLOW_STEP[5:0] where FRACTION = 2 x MFR_SVID_SLOW_SR_SELECTOR[3:0]. [7:6]: Don't Care. [5:0]: SR_SLOW_STEP. Values accepted from 0x01 to 0x3F. If 0x00, wraps to 0x3F.	0x01	FRACTION x 200 mV/us	
		0x02	FRACTION x 100 mV/us	
		0x03	FRACTION x 66.67 mV/us	
		0x04	FRACTION x 50.00 mV/us	
		0x05	FRACTION x 40.00 mV/us	
		0x06	FRACTION x 33.33 mV/us	
		0x07	FRACTION x 28.57 mV/us	
		0x08	FRACTION x 25.00 mV/us	
		0x09	FRACTION x 22.22 mV/us	
		0x0A	FRACTION x 20.00 mV/us	
		0x0B	FRACTION x 18.18 mV/us	
		0x0C	FRACTION x 16.67 mV/us	
		0x0D	FRACTION x 15.38 mV/us	
		0x0E	FRACTION x 14.29 mV/us	
		0x0F	FRACTION x 13.33 mV/us	
		0x10	FRACTION x 12.50 mV/us	
		0x11	FRACTION x 11.76 mV/us	
		0x12	FRACTION x 11.11 mV/us	
		0x13	FRACTION x 10.53 mV/us	
		0x14	FRACTION x 10.00 mV/us	
		0x15	FRACTION x 9.52 mV/us	
		0x16	FRACTION x 9.09 mV/us	
		0x17	FRACTION x 8.70 mV/us	
		0x18	FRACTION x 8.33 mV/us	
		0x19	FRACTION x 8.00 mV/us	
		0x1A	FRACTION x 7.69 mV/us	
		0x1B	FRACTION x 7.41 mV/us	
		0x1C	FRACTION x 7.14 mV/us	
		0x1D	FRACTION x 6.90 mV/us	
		0x1E	FRACTION x 6.67 mV/us	

Bit	Description	Value	Function	Description
		0x1F	FRACTION x 6.45 mV/us	
		0x20	FRACTION x 6.25 mV/us	
		0x21	FRACTION x 6.06 mV/us	
		0x22	FRACTION x 5.88 mV/us	
		0x23	FRACTION x 5.71 mV/us	
		0x24	FRACTION x 5.56 mV/us	
		0x25	FRACTION x 5.41 mV/us	
		0x26	FRACTION x 5.26 mV/us	
		0x27	FRACTION x 5.13 mV/us	
		0x28	FRACTION x 5.00 mV/us	
		0x29	FRACTION x 4.88 mV/us	
		0x2A	FRACTION x 4.76 mV/us	
		0x2B	FRACTION x 4.65 mV/us	
		0x2C	FRACTION x 4.55 mV/us	
		0x2D	FRACTION x 4.44 mV/us	
		0x2E	FRACTION x 4.35 mV/us	
		0x2F	FRACTION x 4.26 mV/us	
		0x30	FRACTION x 4.17 mV/us	
		0x31	FRACTION x 4.08 mV/us	
		0x32	FRACTION x 4.00 mV/us	
		0x33	FRACTION x 3.92 mV/us	
		0x34	FRACTION x 3.85 mV/us	
		0x35	FRACTION x 3.77 mV/us	
		0x36	FRACTION x 3.70 mV/us	
		0x37	FRACTION x 3.64 mV/us	
		0x38	FRACTION x 3.57 mV/us	
		0x39	FRACTION x 3.51 mV/us	
		0x3A	FRACTION x 3.45 mV/us	
		0x3B	FRACTION x 3.39 mV/us	
		0x3C	FRACTION x 3.33 mV/us	
		0x3D	FRACTION x 3.28 mV/us	

Bit	Description	Value	Function	Description
		0x3E	FRACTION x 3.23 mV/us	
		0x3F	FRACTION x 3.17 mV/us	

DVID_VAR_OFFSET_PARAM (0xB00E)

Bit	Function	Description	Format
47:42	RISE_FAST offset	Offset can be added to the reference to compensate for the apparent Droop generated by dV/dt. Offset are expressed in # of VID_Step. Signed Integer. Offset [+/- # of 5mV Steps].	Integer Signed
41:36	RISE_SLOW offset	Offset can be added to the reference to compensate for the apparent Droop generated by dV/dt. Offset are expressed in # of VID_Step. Signed Integer. Offset [+/- # of 5mV Steps].	Integer Signed
35:30	FALL_FAST offset	Offset can be added to the reference to compensate for the apparent Droop generated by dV/dt. Offset are expressed in # of VID_Step. Signed Integer. Offset [+/- # of 5mV Steps].	Integer Signed
29:24	FALL_SLOW offset	Offset can be added to the reference to compensate for the apparent Droop generated by dV/dt. Offset are expressed in # of VID_Step. Signed Integer. Offset [+/- # of 5mV Steps].	Integer Signed
23:10	Offset expiration TauDVID	Offset application/removal time constant. LP_CONST = (25 * 2^14) / (25 + TauDVID[nSec]). [# of non-linear steps -> value[ns]= 25 *(1-(LP_CONST/2^14)) / (LP_CONST/2^14)].	Integer Unsigned
9:0	OC mask after DVID ends	[9..0] = OCP_TAU = (TOCP-25nSec) / 100nSec. OC Disable TOCP after DVID ends. [# of 100nSec steps +25ns internal offset].	Integer Unsigned

TEL_GAIN_VIN (0xB018)

Bit	Description	Format
7:0	VSRMON ADC: Used to define the Gain correction for VIN monitoring over VSRMON when Opto Mode is Enabled. Ranges linearly from 0 (0x00) to 2 (0xFF). 0x80 = Gain = 1 shall be used for a 1/40 divider, which is the recommended configuration. VSRMON ADC range is 0 to 3.2V and VSRMON pin has an internal 10k pull-down resistor, thus a 1/40 divider is achieved by a 390k resistance to VIN.	Fixed Point Unsigned

THERMAL_GAIN (0xB01A)

Bit	Description	Format
7:0	Used to set T_COMP variable for Thermal Compensation of output current sense. T_COMP makes an adjustment of the correction factor that is ideal for copper, according to: Iinfo_TC = Iinfo x Kcorr = Iinfo x 1 / (1 + alfa x deltaT_DCR) = Iinfo x 1 / (1 + alfa x deltaT_NTC x T_COMP / 128) where alfa = 0.0039 and deltaT_NTC is calculated difference from Tmin, given by TEL_NTC_MAP_Q6. Thus, T_COMP is used to compensate for the temp difference between NTC-resistor and output inductor DCR. T_COMP = 128 means ideal correction alfa is used. Note that Kcorr must always be in the range 0.67 to 1.0, which limits the maximum deltaT_NTC that can be handled.	Fixed Point Unsigned

TEL_IOUT_FSR (0xB01B)

Bit	Description	Format	Unit
8:0	Defines the READ_IOUT monitoring ADC Full scale. Shall be set to match the peak OCP limit as defined by MFR_IMON. LSB weight is given by System Register IOUT_EXP.	Fixed Point Unsigned	A

TEL_OFFSET_VIN (0xB027)

Bit	Function	Description	Format	Unit
10	Sign	1 = Positive 0 = Negative	Integer Unsigned	
9:0	Value of offset	VSRMON ADC: Used to define the Offset correction for VIN monitoring over VSRMON when Opto Mode is Enabled. LSB=0.125V	Integer Unsigned	0.125 V

TEL_GAIN_IMON (0xB029)

Bit	Description	Format

Bit	Description	Format
7:0	Sets the gain correction to be applied to IMON reading (both PMBus and CPU-Link). Computed at controller startup as TEL_GAIN_IMON_RAM adjusted per trimming calibration. Ranges linearly from 0 (0x00) to 2 (0xFF). Note. If modified, when MFR_STORE_MAP is issued, IC automatically stores into TEL_GAIN_IMON_RAM the RAW value adjusted per trimming calibration.	Fixed Point Unsigned

TEL_GAIN_FGBR (0xB02A)

Bit	Description	Format
7:0	Used to define the Gain correction for VOUT monitoring. Ranges linearly from 0 (0x00) to 2 (0xFF). 0x80 = Gain = 1	Fixed Point Unsigned

SVI_ADDITIONAL_OFFSET (0xB02B)

Bit	Function	Description	Format
1:0	DPM # of phases PS2	0x01 = NCELL=1 through 0x06 = NCELL=6. Other combinations are not supported. Configures the minimum number of operating phases in PS02.	Integer Unsigned

Bit	Function	Description	Value	Function	Description
7	Enable hiccup mode	Enable hiccup fault response mode. When enabled, after a fault occurred, the controller re-attempts to startup Vout after 1 mSec. When enabled, the hiccup fault response mode applies for the fault types that are enabled in MFR_FAULT_CONFIG. After a restart due to hiccup, the fault flag set in STATUS_WORD will be cleared.	0		Disable hiccup mode
			1		Enable hiccup mode
6	IMON divider @ dynamic VID	IMON divider in dynamic VID condition. Delivers reduced IMON current to the IMON resistor to prevent from false OC being trip.	0	IMON/2	Divide by 2.
			1	IMON/4	Divide by 4.
5:4	IMON divider @ soft start	IMON divider in soft start transitions. Delivers reduced IMON current to the IMON resistor to prevent from false OC being trip.	00	IMON	Divide by 1.
			01	IMON/2	Divide by 2.
			10	IMON/4	Divide by 4.
			11	IMON/8	Divide by 8.
3	Enable soft bias current sense	Enable soft bias to allow current sense below Vout 0.7V. Prevent damage at startup with short circuit for full bridge. Optimizes current reading amplifier biasing at low output voltages preventing saturation. Reserved, need to be 0b1 (enabled).	0		Disable
			1		Enable

TEST_MUXES (0xB02F)

Bit	Description	Format
31:0	Control of data to output on PFAULT pin.	Byte Array

VIN_FEED_FWD_SOURCE (0xB038)

Bit	Description	Value	Function	Description
0	Used to define which input to be used for VIN FeedForward Compensation. 0x00 = Uses data from PuC. 0x01 = Uses data from VSRMON at secondary. Other combinations are not supported.	00	PuC	
		01	VSRMON at secondary	

VIN_MONITORING_SOURCE (0xB039)

Bit	Description	Value	Function	Description
0	Used to define which input to be used for VIN	00	PuC	

Bit	Description	Value	Function	Description
	monitoring and Protection between PuC and VSRMON. VSRMON needs to be further configured. 0x00 = Uses data from PuC. 0x01 = Uses data from VSRMON at secondary. Other combinations are not supported.	01	VSRMON at secondary	

IOUT_VR125_PERC_EN (0xB03C)

Bit	Description	Value	Function	Description
0	Used to define whether the IOUT reporting on reg15h is to be in percentage of ICCMAX (given by MFR_SVID_ICCMAX) or absolute value in Amperes.	0	Absolute in [A]	
		1	% of ICCMAX	

OPTO_EN (0xB03D)

Bit	Description	Value	Function	Description
0	Used to define which information is sent to ADC to realize VIN sensor on VSRMON. 0x00 = Peak Detector is sent to ADC. Need to connect divider from PHASE to VSRMON. 0x01 = Direct connection to ADC (Opto-Mode). Other combinations are not supported.	00	Peak Detector	
		01	Opto-Mode	

EN_TIMEOUT_RESONANT_END (0xB03E)

Bit	Description	Format
7:0	Reserved - must be 0x01.	Fixed Point Unsigned

EN_DUTY_ACTIVE (0xB03F)

Bit	Description	Format
7:0	Reserved - must be 0x01.	Fixed Point Unsigned

VR13_TIME_FRAME (0xB040)

Bit	Description	Value	Function	Description
0	Used to define averaging interval for VR1xx IMON reporting register. Update interval is always 100uSec while averaging can be programmed.	0	Averaging on 200 us	
		1	Averaging on 100 us	

CTRL_VERR_CLAMP (0xB041)

Bit	Description	Format	Unit
5:0	[5:0]: CTRL_VERR_CLAMP; LSB = 2mV; VerrClamp = 2mV * (63 - CTRL_VERR_CLAMP). Set 128m (0x00) to OFF; max 126mV (0x01).	Fixed Point Unsigned	mV

T_SWITCHING_OPEN_LOOP (0xB042)

Bit	Description	Format	Unit
8:0	Used to set the switching period for Open Loop Mode. Period is set as a multiple of internal clock periods (25nSec).	Fixed Point Unsigned	us

DISABLE_DPM_PROT (0xB044)

Bit	Description	Value	Description
0	Used to disable DPM Protection that, during ACLL, increases the # of phases by 1 if instantaneous FSW gets greater than averaged FSW_AVG. FSW_AVG set by MFR_FSWITCH_PROTECT_COEFF in Resonant Loop	0	DPM Protection Enabled - # of phases reset in load transient

Bit	Description	Value	Description
	while in Non Resonant Loop the comparison is made over the nominal FSW set. Trigger threshold changes with the number of active phases: # of active phases = 1 => Fthreshld = 2.00*FSW_AVG. # of active phases = 2 => Fthreshld = 1.50*FSW_AVG. # of active phases = 3 => Fthreshld = 1.33*FSW_AVG. # of active phases = 4 => Fthreshld = 1.25*FSW_AVG. # of active phases = 5 => Fthreshld = 1.20*FSW_AVG.	1	DPM Protection Disabled - # of phases NOT reset in load transient

TGB_CONFIG (0xB046)

Bit	Function	Description	Format	Unit
7:2	TGB Threshold on Error from Control ADC	LSB = 2mV, max 126mV (0b111111)	Fixed Point Unsigned	mV

Bit	Function	Description	Value	Function	Description
1:0	Mode of Transient Gain Boost	Used to configure Transient Gain Boost to improve ACLL response. When Control ADC error exceeds the threshold, VCO gain is doubled. [1:0]: TGB Mode. 0b00 = Disabled. 0b01 = Enabled when # of phases >= 2. 0b10 = Enabled. 0b11 = Enabled with 2x threshold when # of phases=1.	00	TGB Disabled	
			01	Enabled when # of phases >= 2	
			10	Enabled	
			01	Enabled with 2x threshold when # of phases=1	

OPEN_LOOP_CONFIG (0xB048)

Bit	Function	Description	Value	Function	Description
3:1	Phase selection	Selection of which phase to operate.	000	All phases	All phases
			001	Phase 1	Phase 1
			010	Phase 2	Phase 2
			011	Phase 3	Phase 3
			100	Phase 4	Phase 4
			101	Phase 5	Phase 5
			110	Phase 6	Phase 6
0	Open Loop Mode	Enable open loop operation. Only for bringup. PWMs generates a fixed waveforms regardless of loop compensator. TSHIFT and TSTART are programmed by MFR_T_START_PH_SHIFT_DELTA_DELAY regardless of the control loop configured resonant or non-resonant.	0		Disable
			1		Enable

TON_RED_CONFIG (0xB04A)

Bit	Function	Description	Format	Unit
1:0	ZCDM offset	Used to set an offset on ZCD to optimize PFM (not for Phase 1 which uses ZCD1_OFFSET). Offset in [uA], how this is translated into [A] on inductor ripple depends on the real application implemented. 0x03 = 2.4uA ; 0x02 = 4uA; 0x01 = 5.6uA; 0x00 = 7.2uA. Other combinations are not supported.	Fixed Point Unsigned	uA

Bit	Function	Description	Value	Description
7	Boost on Phase number change	On phase change, boost ON. Reserved, set to 0.	0	Disabled
			1	Enabled
6	All phases enable	If DUTY_CONTROL is on, all phase on. See MFR_DUTY_PARAMETER, enables all phases if VIN lower than VOLTAGE_DUTY_ENABLE.	0	Disabled
			1	Enabled
5	Force VR_READY	When set/enabled, VRREADY = 0 regardless of regulation. Reserved bit #4 need to be set to 0b.	0	Disabled
			1	Enabled
3	Prevent spec patterns	NO_PINTA: Prevents issuing special patterns in case of primary driver replacement.	0	Disabled
			1	Enabled

Bit	Function	Description	Value	Description
2	VIN hysteresis	1V hysteresis on DUTY_CONTROL activation threshold. See MFR_DUTY_PARAMETER, enables 1V hysteresis on DUTY_CONTROL activation threshold.	0	Disabled
			1	Enabled

EN_DROOP_START (0xB04B)

Bit	Description	Value	Function	Description
0	Enables fake droop effect at startup to keep Control-ADC Error negative to avoid bumps on VOUT at Start-up. 0x00 = DROOP_START Disabled. 0x01 = DROOP_START Enabled. Other combinations are not supported.	00	DROOP_START Disabled	
		01	DROOP_START Enabled	

VR_TAB_RAIL (0xB04C)

Bit	Description	Value	Function	Description
0	Selection of VR13 10mV/5mV table. Impact all relative SVID registers. In AVSBus mode 5 mV is always used, regardless of setting. 0x00 = 10mV. 0x01 = 5mV.	0	10mV Table	
		1	5mV Table	

CS_OVERFLOW_DISABLE_IRQ (0xB04E)

Bit	Description	Value	Function	Description
0	Used to disable current sharing overflow fault. 0x00 = Current Sharing FAULT Enable. 0x01 = Current Sharing FAULT Disable. Other combinations are not supported.	00	Enable Current Sharing FAULT	
		01	Disable Current Sharing FAULT	

VR_READY_FAST_DISABLE (0xB051)

Bit	Description	Value	Function	Description
0	Used to allow immediate VR_RDY signal de-assertion in case of disable from EN pin. If not set, VR_RDY may be delayed from EN de-assertion up to 400 us.	00	Disable fast de-assertion	
		01	Enable fast de-assertion	

DCR_INV_COEFF (0xB052)

Bit	Description	Format	Unit
7:0	Used to program the value of 1/DCReq, where DCReq value is expressed in mOhm. Warning: CANNOT BE ZERO. Note. Since every Main/Satellite features 2 output inductor, the number to be programmed here (1/DCReq) is half of the single inductor DCR (1/DCReq = 2/DCR - the parallel between the two DCRs). DCReq [mOhm] = 0.291 * 64 / DCR_INV_COEFF. DCR_INV_COEFF = 0.291 * 64 / DCReq [mOhm].	Fixed Point Unsigned	1/mOhm

ADC_PEAK_EN_TOP (0xB056)

Bit	Description	Value	Description
0	Used to enable the ADC to convert information on VSRMON to recover information about VIN. Must be set 0x01.	0	Disable ADC
		1	Enable ADC

MULTIFUNCTION_PIN_MUX (0xB057)

Bit	Function	Description	Value	Function	Description
2	Enable IMON filtering	[2:2]: Enable additional analog filtering on IMON (800nSec time constant) to prevent from false OC tripping and to reduce overall ripple noise. Should always be enabled.	0		Disable IMON filtering
			1		Enable IMON filtering

Bit	Function	Description	Value	Function	Description
1:0	Configure droop start	Configure DROOP_START which enables fake droop effect at startup to keep Control-ADC Error negative to avoid bumps on VOUT at Start-up.	00	Standard	Standard (only on FBR pin)
			01	FBR and RDROOP	DROOP_START_CONFIG on FBR and RDROOP
			10	FBR and 2X RDROOP	DROOP_START_CONFIG on FBR and RDROOP, 2x on RDROOP
			11	FBR and 3X RDROOP	DROOP_START_CONFIG on FBR and RDROOP, 3x on RDROOP

NCHECKS (0xB05B)

Bit	Description	Value	Function	Description
2:0	Blanking time between PWMX,Y. Defines the minimum blank time between two consecutive TSHIFTs generated. See HIGH_CURR_PROT_EN for interactions with TSHIFT_LSB parameters. 0x00 = 25 ns - Not to be used in non-resonant PSFB. Resonant Application: HIGH_CURR_PROT_EN[6] cannot be set 0x01 = 50 ns - Not to be used in non-resonant PSFB 0x02 = 75 ns - Not to be used in non-resonant PSFB 0x03 = 100 ns 0x04 = 125 ns 0x05 = 150 ns 0x06 = 175 ns 0x07 = 200 ns	000	25 ns	
		001	50 ns	
		010	75 ns	
		011	100 ns	
		100	125 ns	
		101	150 ns	
		110	175 ns	
		111	200 ns	

MONITOR_OFFSET (0xB05E)

Bit	Description	Format	Unit
4:0	Vout monitoring offset applied to READ_VOUT (not applied to MFR_READ_VOUT). LSB depends on the table used (10mV or 5mV by VR_TAB_RAIL). Signed. It is an additional contribute to MFR_VOUT_CAL_OFFSET which is usually tuned to compensate internal ADC VSS (0.5V).	Fixed Point Signed	mV

IMONX2 (0xB061)

Bit	Description	Value	Function	Description
0	Impacts the equation for RIMON/RG given by MFR_IMON. Used to gain more granularity in OC setting when lower values of RIMON are used. See MFR_IMON command for more details.	00	IMON x 1	
		01	IMON x 2	

IOUT_EXP (0xB062)

Bit	Description	Value	Function	Description
1:0	Controls (linear) format used for Iout and Pout settings/readings. When HC support (see MFR_SVID_SLOW_SR_SELECTOR) is disabled: 0x00: Iout exponent = -2 (LSB=0.25A), Pout exponent = 0 (LSB=1W), TEL_IOUT_FSR exponent = 0 (LSB=1A). 0x01: Iout exponent = -1 (LSB=0.5A), Pout exponent = 1 (LSB=2W), TEL_IOUT_FSR exponent = 1 (LSB=2A). 0x02: Iout exponent = 0 (LSB=1A), Pout exponent = 2 (LSB=4W), TEL_IOUT_FSR exponent = 2 (LSB=4A). When HC support (see MFR_SVID_SLOW_SR_SELECTOR) is enabled, the settings as IOUT_EXP = 0x01 are used. The following commands are affected: IOUT_OC_FAULT_LIMIT. IOUT_OC_WARN_LIMIT. POUT_OP_FAULT_LIMIT. READ_IOUT. READ_POUT. MFR_DPM1_THR. MFR_DPM2_THR. MFR_DPM3_THR. MFR_DPM4_THR. MFR_DPM5_THR. DPM_HYSTERESIS (Sys Reg). TEL_IOUT_FSR (Sys Reg).	00	LSB=0.25A (Exp=-2)	
		01	LSB=0.5A (Exp=-1)	
		10	LSB=1A (Exp=0)	

EXTRA_OFFSET (0xB063)

Bit	Description	Format	Unit
7:0	Additional offset for SVID and AVSBus domain (does not apply to PMBus) In AVSBus mode, if applied, need to be in tracking with MFR_VOUT_TRIM. # of VID LSB to add to setpoint (unsigned, always positive).	Fixed Point Unsigned	mV

DPM_OFFSET (0xB064)

Bit	Description	Format	Unit
7:0	DPM threshold offset. Always Negative. Used to offset phase shedding thresholds in order to compensate for each phase current ripple without playing with DPM_HYSTERESYS. LSB weight based on IOUT_EXP and HC support enabled or disabled.	Fixed Point Unsigned	A

SOFT_OFF_CONFIG (0xB065)

Bit	Description	Value	Function	Description
0	Controls method of turning off phases after a soft off. 0x00 = Soft off procedure is performed by shutting down all phases sequentially after Vout ramps down to 0.25V. Recommended in in PSFB or resonant solutions. 0x01 = Soft off procedure is performed by shutting down all phases at the same time after Vout ramps down to 0.25V. This procedure will not be used in PSFB or resonant solutions but it will be used in other applications.	0	Phases sequentially	
		1	All phases at the same time	