THERMAL MODEL

BMR511

FLEX INC.

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General

The model is an estimation of the thermal behavior of BMR511, which is an open frame LGA/BGA design. The mechanical structure, PCB stack-up, components and materials are similar to other products in the same family, which means that this thermal model is applicable for several products within the BMR511 family.

The model is intended for steady-state thermal simulations.

Model Description

The model is a readymade Flotherm 11.1 model. The model consists of three major components:

3D CAD Geometry

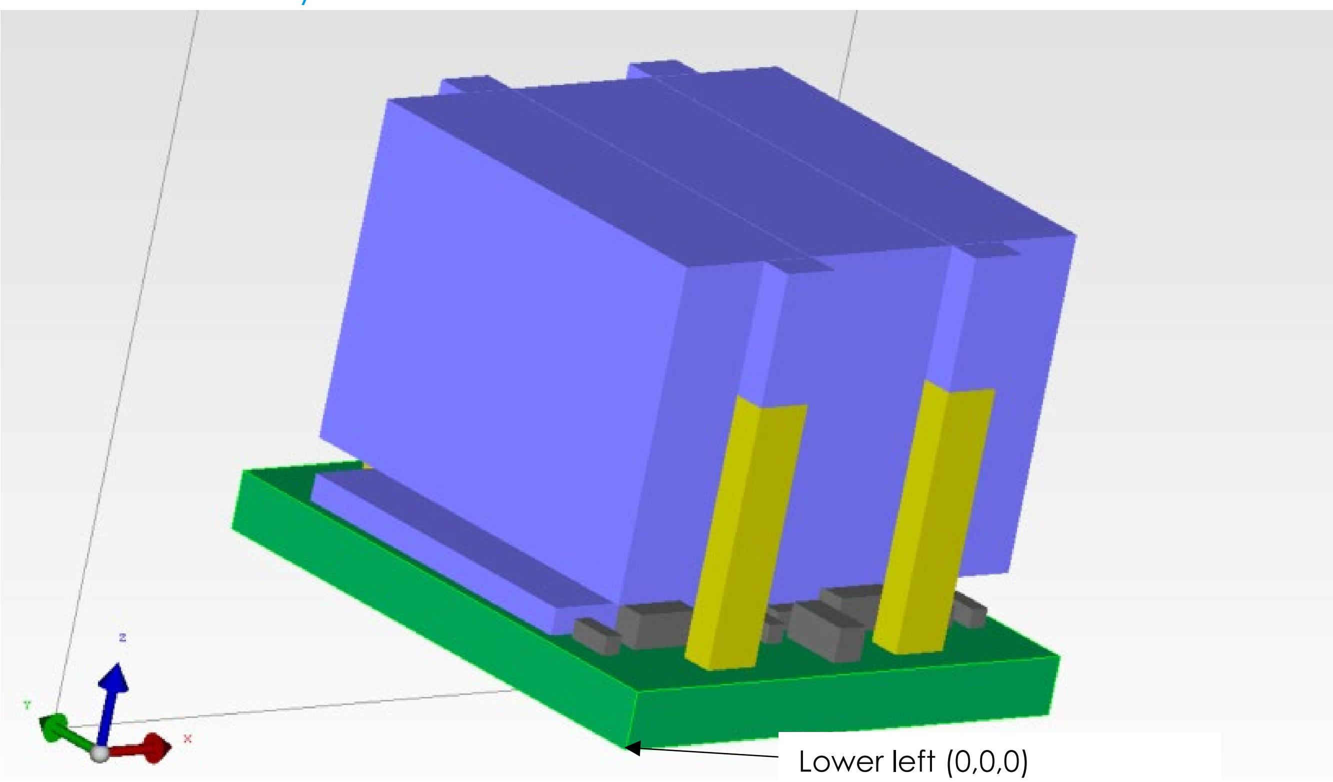


Figure 1

In the geometry most components are maintained per the original design but have been simplified in FloMCAD to cuboids. The inner layers of the PCB have been modeled as cuboids with averaged thermal conductivity (based on copper coverage). The outer layers have been processed for patches in FloEDA. To capture the blind vias, the via sets are processed as copper patches. The buried vias are defined as electrical vias (adjusted for height).

Origin has been placed so that [0,0,0] is in the lower left corner of the PCB.

Unit in file: [mm]

Domains of power loss distribution

There are several sources for power loss. The power loss for each of them, at certain combinations of module voltage and current, are given in *Appendix 1 - Power Loss Distribution*.

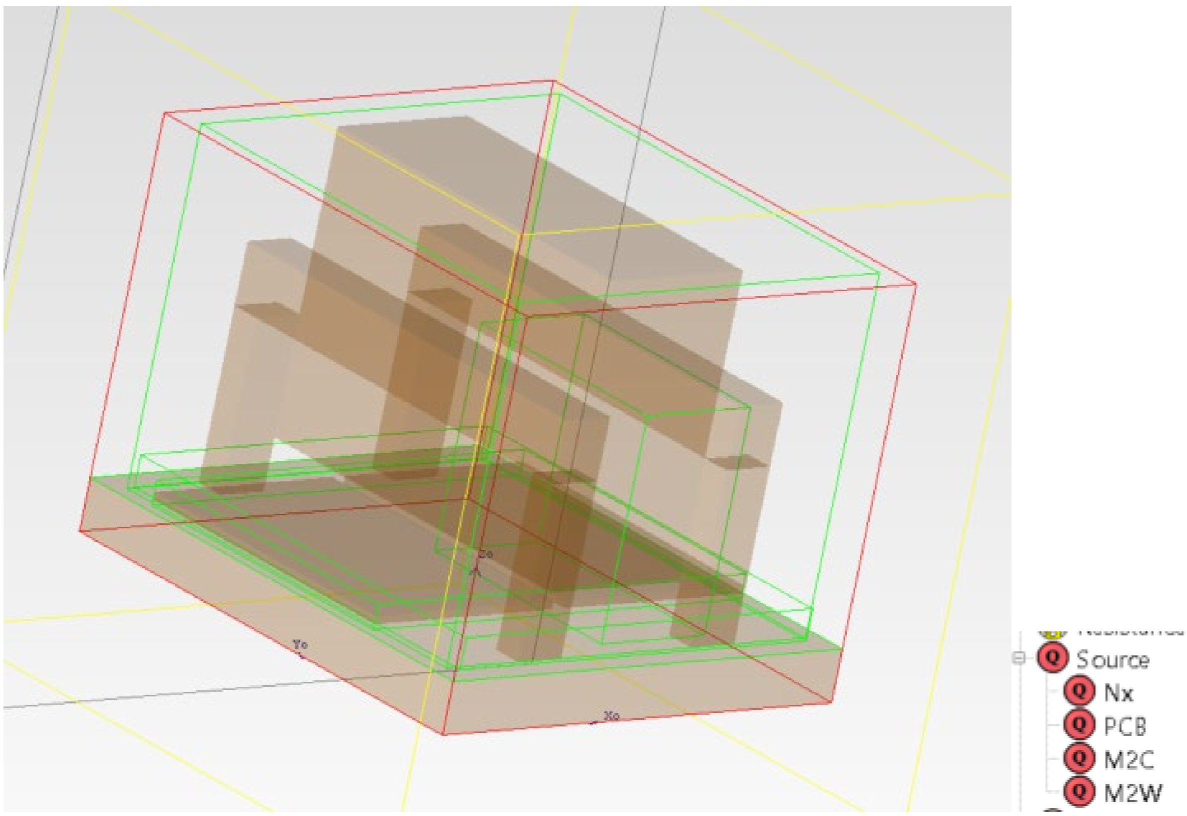


Figure 2 Domains of power losses

Domains of material data

There are several material domains. The heat conductivity for each of them is given either as isotropic, or anisotropic values in x-,y-, and z-direction (x,y,z) in the figures following.

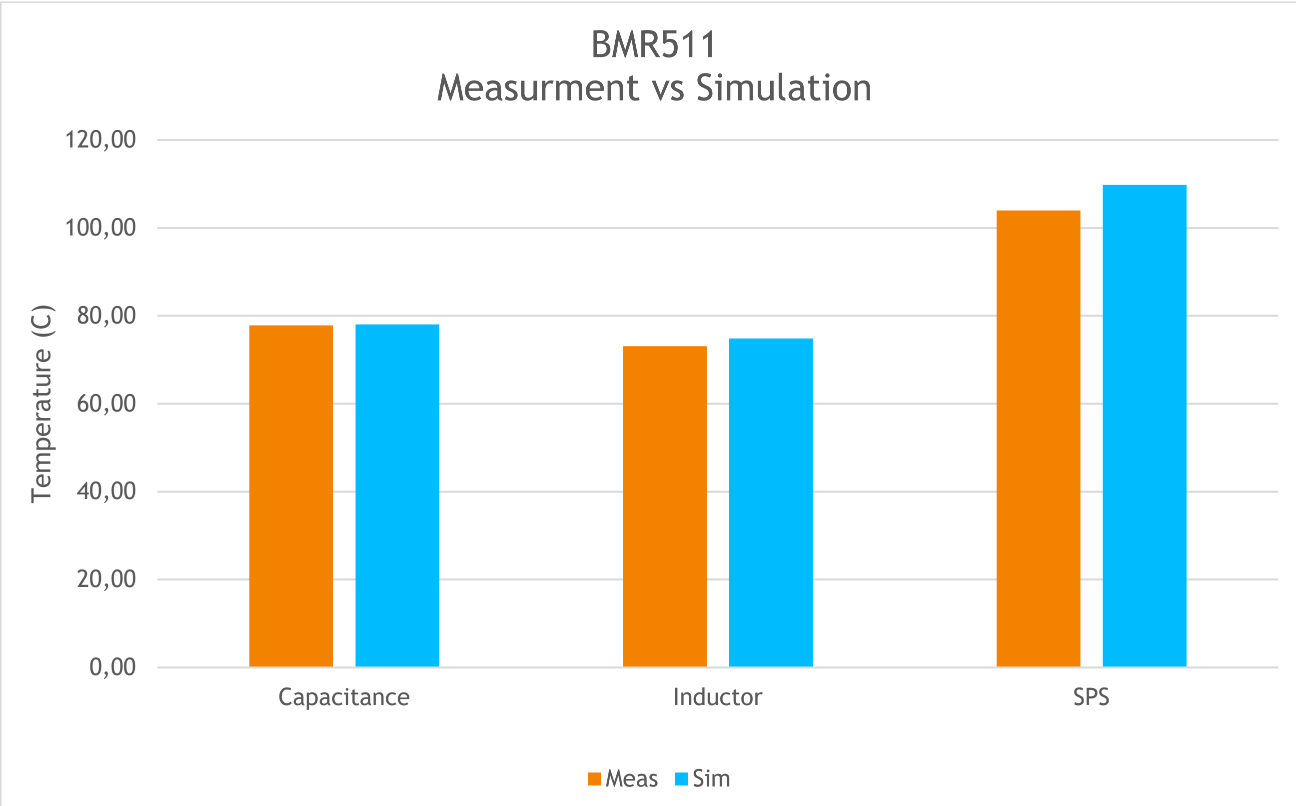
Figure 3: Materials

Note. The given heat conductivity is only intended to model the temperature distribution of the module in this application. The values should not be treated as physical true or transferable to other applications.

Model Calibration

The model has been calibrated to give temperatures as similar as possible for V_{in}=12V, I_{in}=13A, V_{out}=1.8V, I_{out}=80A, P_{loss}=12.6-13.1, compared to thermal verification document *2/102 65-BMR511A*. In the thermal verification test board and cold wall was controlled in the range 60C-90C. The SPS temperature reading comes from the component internal temperature sensing, and have been read-out through the PMBus.

The result of the calibration can be seen in Figure 4.



Type	*Cold Wall*	*PCB*	*Capacitance*	*Inductor*	*SPS*	*Ploss W*
Meas	*60.00*	*60.00*	*77.81*	*73.13*	*104.00*	*12.7*
Sim	*60.00*	*60.00*	*78.04*	*74.87*	*109.76*	*12.61*

Figure 4: Model calibration result

As a reference the calibration set-up is provided as an assembly "Verification Set-up", see Figure 5. It consists of one domain for cold wall, and one domain for the test board. This assembly should be deleted when the model is imported into a project.

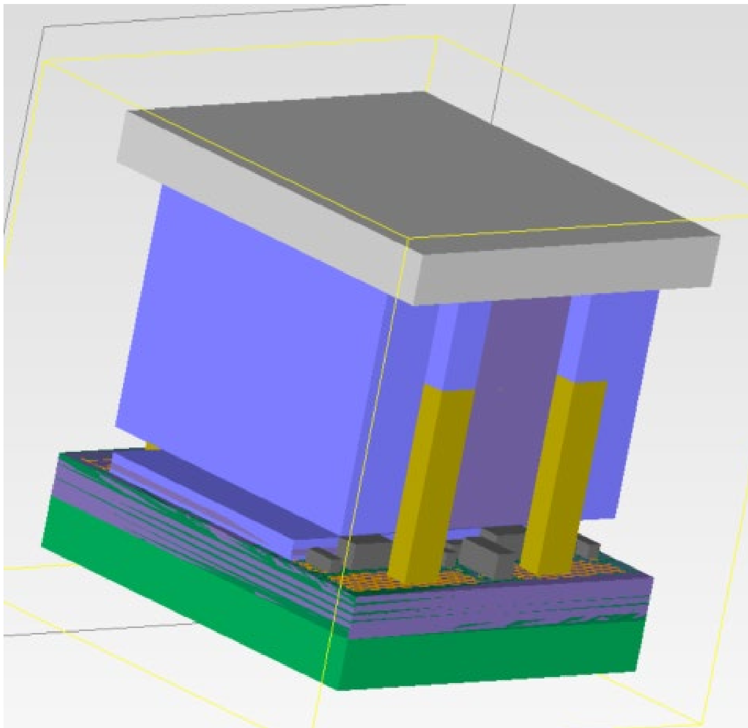


Figure 5. Verification Set-up including cold wall and test board.

Model Usage

Import the *.pdml file into the desired project. Delete the assembly "Thermal Verification Set-Up".

Assign power losses per table in *Appendix 1 - Power Loss Distribution* to the sources in section *Domains of power loss distribution*. Default settings are for V_{in}=12V, I_{in}=13A, V_{out}=1.8V, I_{out}=80A, P_{loss}=12.6-13.1T≈100[C]

If the model is rotated, make sure that the orientation of the orthotropic materials properties are preserved (also rotated).

Do not change the order of power sources and geometry objects, as this can change the power and material settings.

The module temperatures can be monitored in predefined monitor points, which corresponds to the measured points in the thermal verification. These temperatures are not intended for pass/fail criteria.

Additional Information

Model has been constructed with SI units.

Reference

Thermal report *2/102 65-BMR511*
data file BMR511.pdml

Disclaimer

The model and model documentation described herein are provided for the sole purpose of facilitating thermal modeling of a structure where the referenced product is included. It should not and cannot be interpreted neither as a detailed description of the product itself, nor as a statement of the product's performance.

The model has been constructed on a best effort basis, but we cannot accept liability for any discrepancy between model predictions and actual values.

Revision history

Revision	Revision information	Date	Responsible
A	New document	2023-04-28	KARLADRU
B	Language updated	2023-04-28	KARTWAER
C	Language updated	2023-05-04	KARTWAER

Appendix 1

Power loss distribution example for BMR511.

V_{in}=12V, I_{in}=13A, V_{out}=1.8V, I_{out}=80A, P_{loss}=12.6-13.1, T≈100[C]

Source	Number of domains	Per domain [W]	Total [W]
Nx- Power Stages	2	5.1555	10.311
M2C-Choke core AC+DC	1	0.58	0.58
M2W-Choke winding AC+DC	(*)	(*)	0.813
PCB	1	0.91	0.91
Total [W]			**12.61**

(*) Defined as Source/Volume. Adjust source so that the total adds up.