DESCRIPTION THERMAL MODEL FOR PKJ4716H

FLEX POWER MODULES

Contents

General

The model is based on and valid for PKJ4716H, which is a through hole pin design. The model is intended for steady-state thermal simulations.

Model Description

The model is a readymade FloTHERM 11.1 model. It was created by importing a CAD model in STEP format through the MCAD bridge.

The model consists of the four major components:

3D CAD Geometry

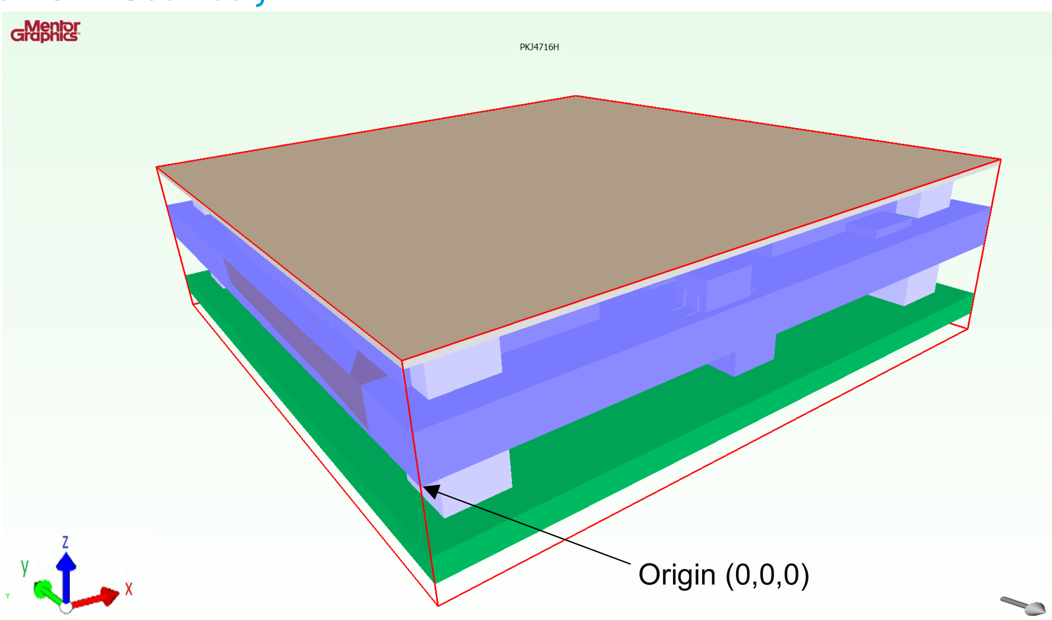


Figure 1 Model origin in lower left corner of the PCB and axis orientation

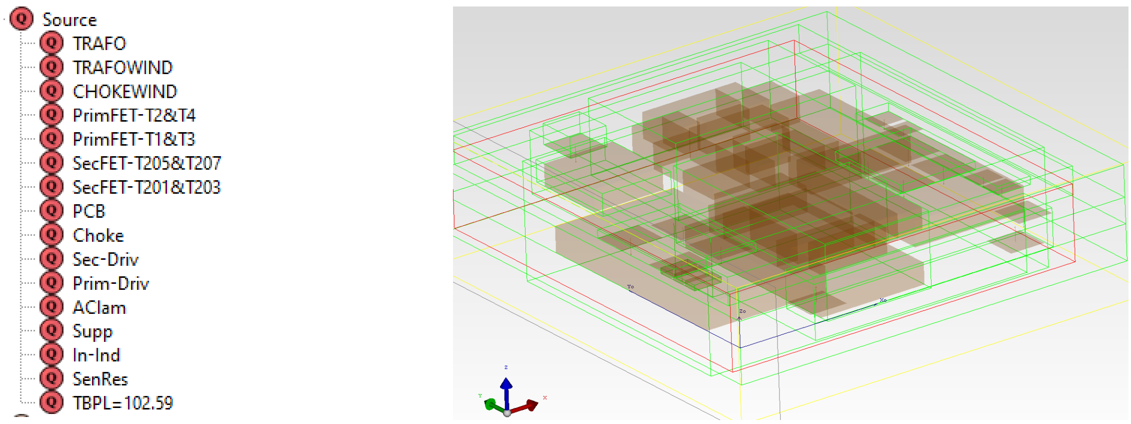
Components that are not contributing to the heat transfer have been removed from the geometry. The PCBs has been simplified to a bulk geometry where the copper layers and via have been taken into consideration by assigning anisotropic material properties to the PCBs domains.

Origin has been placed so that [0,0,0] is in the lower left corner of the PCB. Unit in file: [mm]

Note. In order to make sure there are adequate grid coverage for PCB object, grid constraint in the Z-direction is defined so that PCB has a minimum of 10 cells in this direction.

Domains of power loss distribution

There are several sources for power loss. The power loss for each of them, at certain module total powers, are given in *Appendix 1 - Power Loss Distribution*



(a) (b)

Figure 2: Power loss setting: (a) list of heat sources, and (b) heat sources distribution in the model

Domains of material data

There are several material domains. The heat conductivity for each of them is given either as isotropic, or anisotropic values in x-,y-, and z-direction (x,y,z) per the following list.

- Material
  - FR4
  - Copper (Pure)
  - Glue_T&C
  - Glue_MGS
  - 70,70,3
  - 2,2,1
  - 20,20,2
  - 100,100,3
  - 0.7,0.7,1
  - 50,50,2
  - 1,1,1
  - 0.8,0.8,1
  - 1.25,1.25,1
  - Steel Stainless-302 (Cr18/Ni8)
  - Distance
  - Aluminum-6061
  - Mold
  - CuTe
  - Ferrite

Figure 3. Domains of material data

Note. The given heat conductivities are only intended to model the temperature distribution of the module in this application. The values should not be treated as physically true or transferable to other applications.

Monitor points

Monitor points are set according to 1/10265–BMR68103 document which is the thermal verification report of this product. Figure 4 shows the top and pin sides and the location of the thermo-couples.

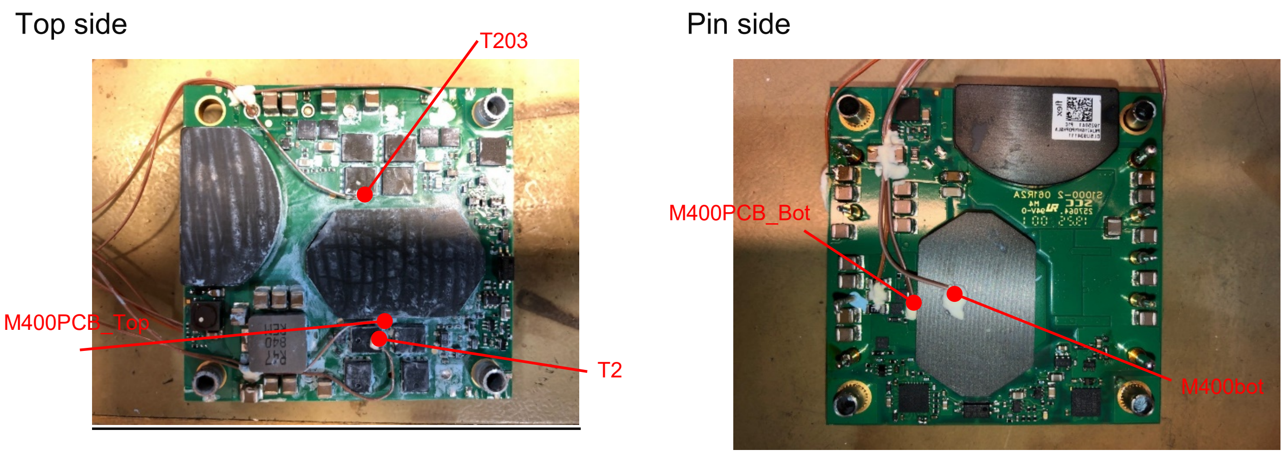


Figure 4. Thermocouple location.

Model Calibration

The FloTHERM simulation temperatures for V_{in}=48[V], V_{out}=50 [V] and I_{out}=14[A] are compared to COMSOL simulation results and measured temperatures from cold wall thermal test reported in 1/10265–BMR68103 document. In these calculations, temperature of the application board is set to 93 ℃. Conduction heat transfer is only considered here which means no heat transfer to the surrounding air.

FloTHERM simulation temperatures are within ±5 ℃ compared to the results from cold wall test and COMSOL detailed model (Figure 5).

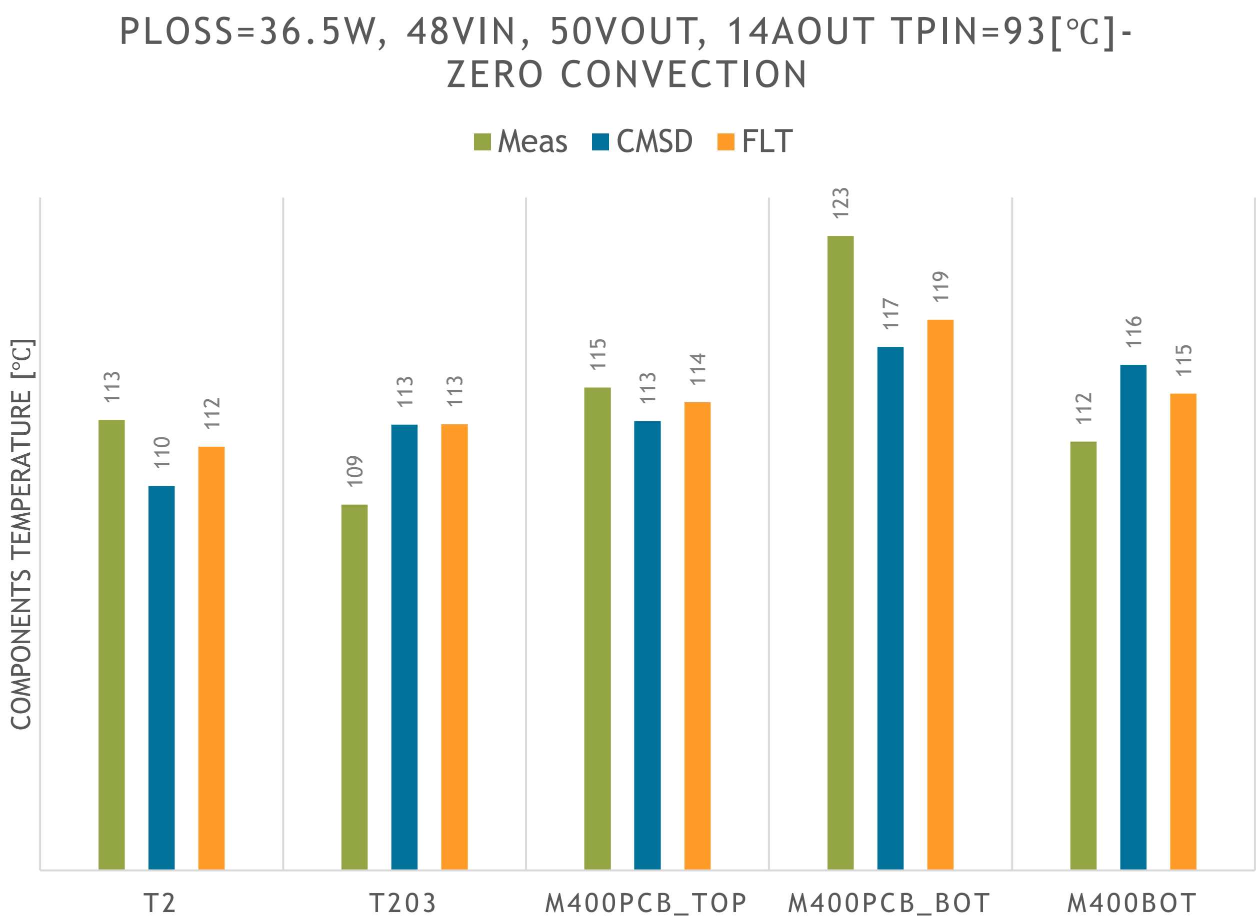


Figure 5: Model calibration result- FLT: FloTHERM simulation results, CMSD: COMSOM detialed model simulation results and Meas: Measured temepratures reported in 1/10265-BMR681 03 document.

Model Usage

Import the *.pdml file into the desired project.

Adjust the dissipated power by altering the thermal heat sources in Figure 2, according to Appendix 1 - Power Loss Distribution. Default settings are for 36.5[W].

Note1: If the model is rotated, make sure that the orientation of the orthotropic materials properties is preserved (also rotated).

Note2: Do not change the order of power sources and geometry objects, as this can change the power and material settings.

The module temperatures can be monitored in predefined monitor points.

Additional Information

Model has been constructed with SI units.

Reference

Thermal report 1/10265-BMR68103.

Disclaimer

The model and model documentation described herein are provided for the sole purpose of facilitating thermal modeling of a structure where the referenced product is included. It should not and cannot be interpreted neither as a detailed description of the product itself, nor as a statement of the product's performance.

The model has been constructed on a best effort basis, but we cannot accept liability for any discrepancy between model predictions and actual values.

Revision history

A	2020/06/15	New document

Appendix 1 - Power Loss Distribution

Power loss distribution example for BMR681 03.

V_{in}= 48 [V] V_{out}= 50 [V] I_{out}=14 [A]

Domain	Number of domains/ boundaries	Domain volume [mm³]	per domain [W]	per volume [mW/mm³]	Subtotal power loss [W]
TRAFO	3	2889		1.23	3.56
TRAFOWIND	6	762		10.42	7.94
CHOKEWIND	11	1653		1.31	2.16
Choke	3	386		2.59	1.0
PrimFET-T1T3	2		0.61		1.22
PrimFET-T2T4	2		0.5		1.0
SecFET-T201T203	2		1.17		2.34
SecFET-T205T207	2		1.29		2.58
PCB	2	3356		1.47	4.94
Prim-Driv	1		0.81		0.81
AClam	4		1.39		5.56
Supp	1		0.61		0.61
In-Ind	1		1.31		1.13
Sec-Driv	2		0.69		1.38
Sen-Res	3		0.1		0.3
				Total (W)	**36.53**