DESCRIPTION
THERMAL MODEL FOR
PKM4516AD

FLEX POWER MODULES

Contents

General

The model is based on and valid for PKM4516AD, which is a through hole pin design. The model is intended for steady-state thermal simulations.

Model Description

The model is a readymade FloTHERM 11.1 model. It was created by importing a CAD model in STEP format through the MCAD bridge.

The model consists of the four major components:

3D CAD Geometry

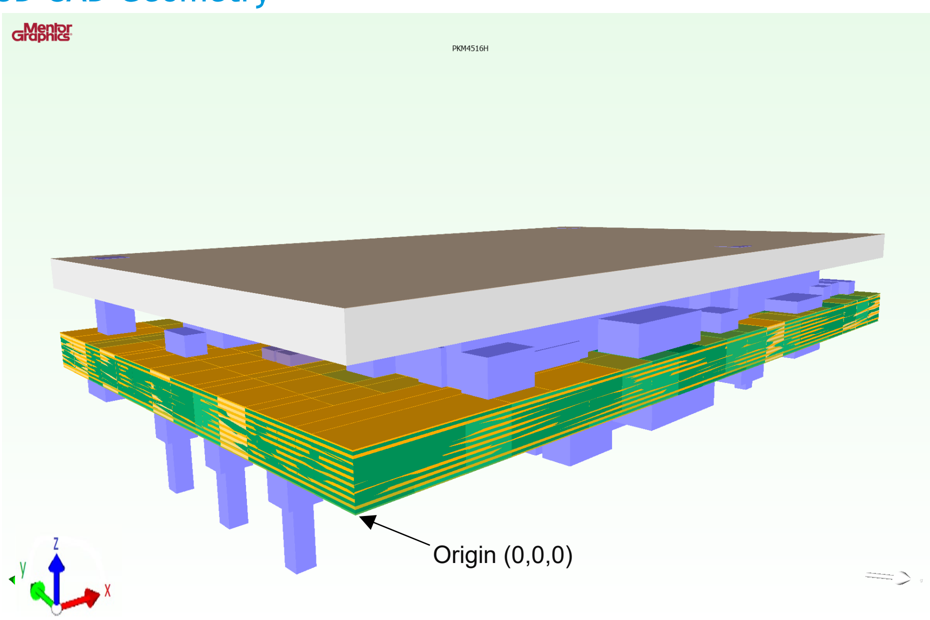

Figure 1. 3D geometry of the model in the software

Origin has been placed so that [0,0,0] is in the lower left corner of the PCB. Unit in file: [mm]

Components that are not contributing to the heat transfer have been removed from the geometry. The PCB has been imported through FloEDA bridge module. The level of modeling is detailed one which means each layer has its own material properties based on the layer copper coverage. This detailed level includes also dielectric layers and vias.

Domains of power loss distribution

There are several sources for power loss. The power loss for each of them, at certain module total powers, are given in *Appendix 1 - Power Loss Distribution*

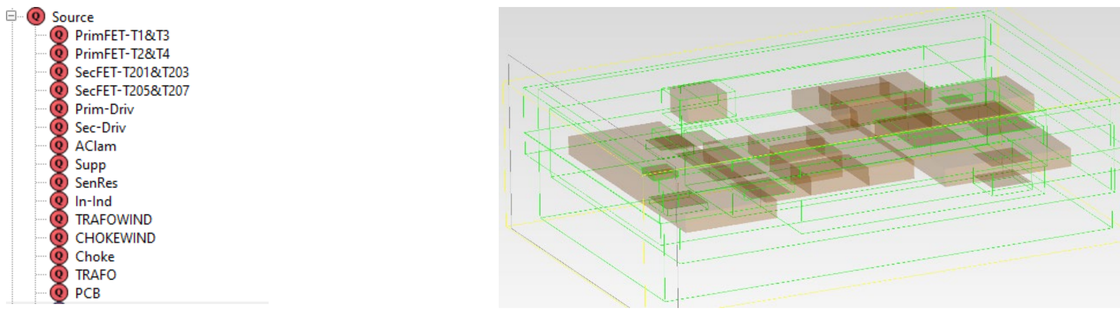

Figure 2. Power loss setting: (a) list of heat sources, and (b) heat sources distribution over the model

Domains of material data

There are several material domains. The heat conductivity for each of them is given either as isotropic, or anisotropic values in x-,y-, and z-direction (x,y,z) per the following list.

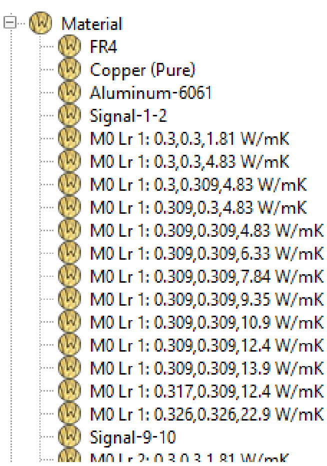

Figure 3. Domains of material data

Note. The given heat conductivities are only intended to model the temperature distribution of the module in this application. The values should not be treated as physically true or transferable to other applications.

Monitor points

Monitor points are set according to the thermal verification report of PKM4516AD. Table 1 and Figure 4 illustrate the thermocouples location in this document.

Table 1- Thermocouples location

Monitor point	Location
T2, T3, and T4	Temperature of primary FETs
T201	Temperature of secondary FET
T210	Temperature of active snubber
PCB pin 8	Temperature of PCB at pin 8
M300 Fe	Temperature of transformer at top side of the core
Vias Primary	Temperature of PCB at transformer's primary side

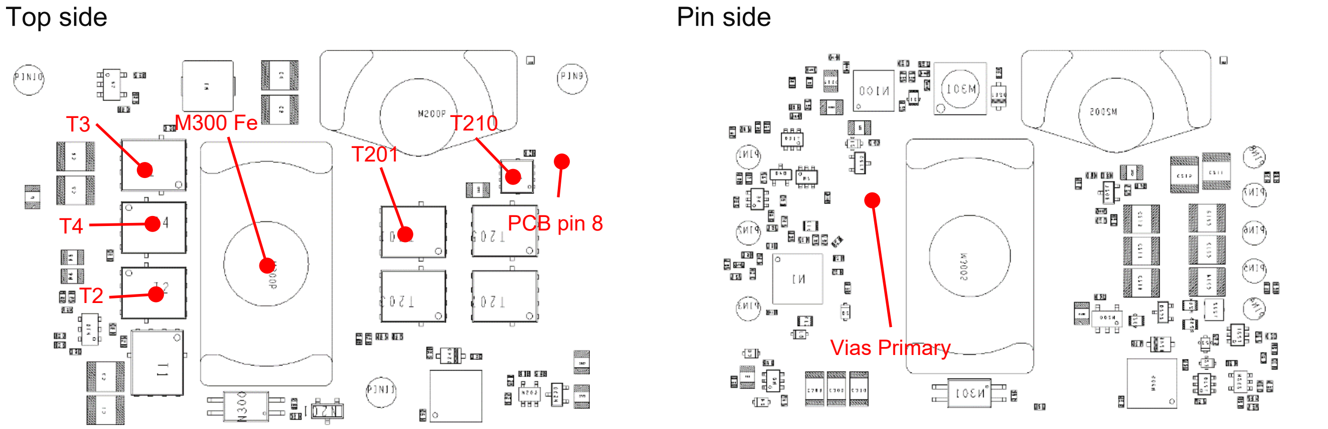

Figure 4. Thermocouple location.

Model Calibration

The FloTHERM simulation temperatures for V_{in}=48[V], V_{out}=28[V] and I_{out}=18[A] are compared to COMSOL simulation results and measured temperatures from thermal verification report of PKM4516HD. In these calculations, temperature of the application board is set to 95℃ and base-plates temperature is 100℃. Conduction heat transfer is only considered here which means no heat transfer to the surrounding air.

FloTHERM simulation temperatures are within ±5 ℃ compared to the results from cold wall test and COMSOL detailed model (Figure 5).

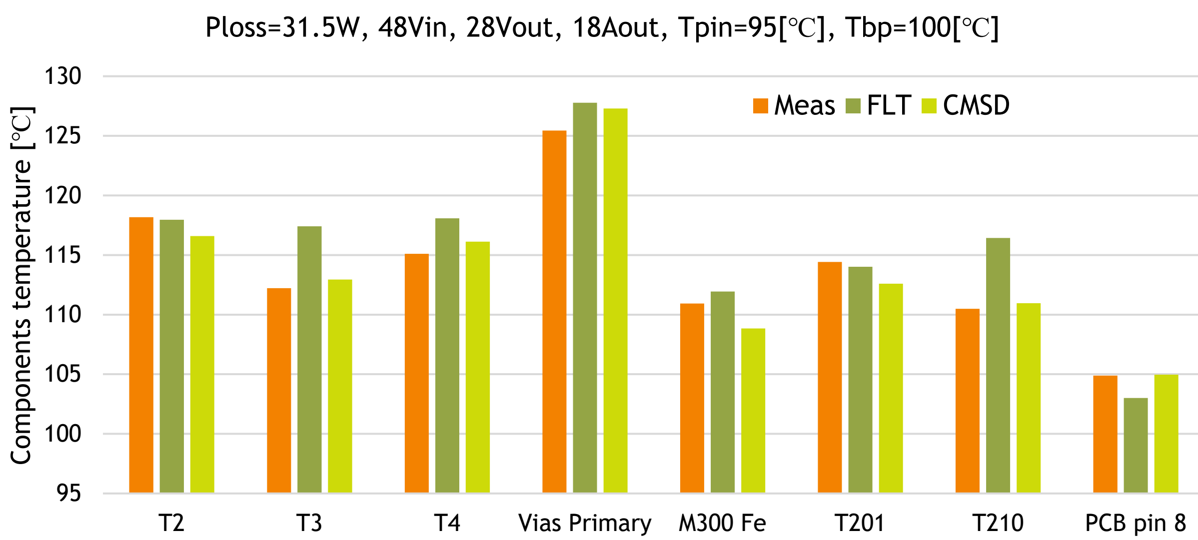

Figure 5: Model calibration result- FLT: FloTHERM simulation results, CMSD: COMSOM detialed model simulation results and Meas: Measured temepratures.

Model Usage

Import the *.pdml file into the desired project.

Adjust the dissipated power by altering the thermal heat sources in Figure 2, according to Appendix 1 - Power Loss Distribution. Default settings are for 31.5[W].

Note1: If the model is rotated, make sure that the orientation of the orthotropic materials properties is preserved (also rotated).

Note2: Do not change the order of power sources and geometry objects, as this can change the power and material settings.

The module temperatures can be monitored in predefined monitor points.

Additional Information

Model has been constructed with SI units.

Reference

Thermal verification report of PKM4516AD

Disclaimer

The model and model documentation described herein are provided for the sole purpose of facilitating thermal modeling of a structure where the referenced product is included. It should not and cannot be interpreted neither as a detailed description of the product itself, nor as a statement of the product's performance.

The model has been constructed on a best effort basis, but we cannot accept liability for any discrepancy between model predictions and actual values.

Revision history

A	2020/06/23	New document
B	2020/08/11	product name change to PKM4516AD

flex

Appendix 1 - Power Loss Distribution

Power loss distribution example for PKM4516AD.

V_{in}= 48 [V] V_{out}= 28 [V] I_{out}=18 [A]

Domain	Number of domains/ boundaries	Domain volume [mm^3]	per domain [W]	per volume [mW/mm^3]	Subtotal power loss [W]
TRAFO	1	112		13.39	1.5
TRAFOWIND	4	588		3.40	2
CHOKEWIND	5	479		7.52	3.6
Choke	1	103		4.84	0.5
PrimFET-T1T3	2		2.35		4.7
PrimFET-T2T4	2		2.33		4.66
SecFET-T201T203	2		1.99		3.98
SecFET-T205T207	2		1.79		3.58
PCB	2	1435		1.73	2.48
Prim-Driv	1		0.81		0.81
AClam	1		0.42		0.42
Supp	1		0.61		0.61
In-Ind	1		0.75		0.75
Sec-Driv	2		0.69		1.38
Sen-Res	2		0.27		0.54
				Total (W)	**31.51**