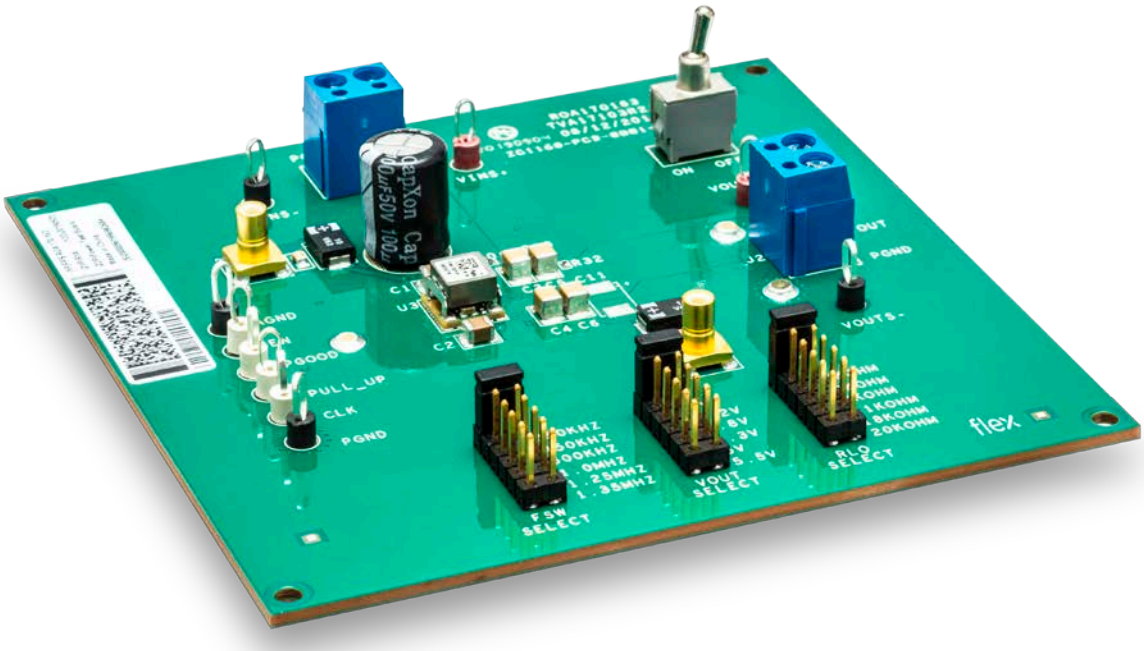
Evaluation Board for PMU product

ROA 170 163

USER GUIDE



Contents

1 Introduction

This User Guide provides a brief introduction and instruction on how to use the Evaluation Board ROA 170 163. This board facilitates evaluation of a PMU module.

The User Guide also provides a description of how the layout guidelines provided in the PMU Technical Specification have been applied to the Evaluation Board layout.

1.1 How to contact Flex

For general questions or interest in our products, please contact your local sales representative. Contact details are available from our website: https://flex.com/expertise/power/scalable-power-modules

1.2 Prerequisites

The test board ROA 170 163 features PMU synchronous buck converter modules operating with a 4.5 V to 17 V input voltage range. The output voltage can be set to six typical values be using a configuration jumper. The switching frequency can also be set to six values corresponding to the six output voltages. The R_{LO} value, which is introduced to optimize transient response, is selectable using a jumper for each output voltage.

Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, loop parameters, line regulation, load regulation, and transient response. Control test points are provided for use of EN, PGOOD and CLK features of the device.

Input and output capacitors are included on the board for the entire range of input and output voltages. Component footprints are provided for adjusting the capacitor combinations and using the main features of the device.

2 Evaluation Board ROA 170 163

Power the board by connecting 4.5-17 V DC power to the “VIN” and “PGND” connectors.

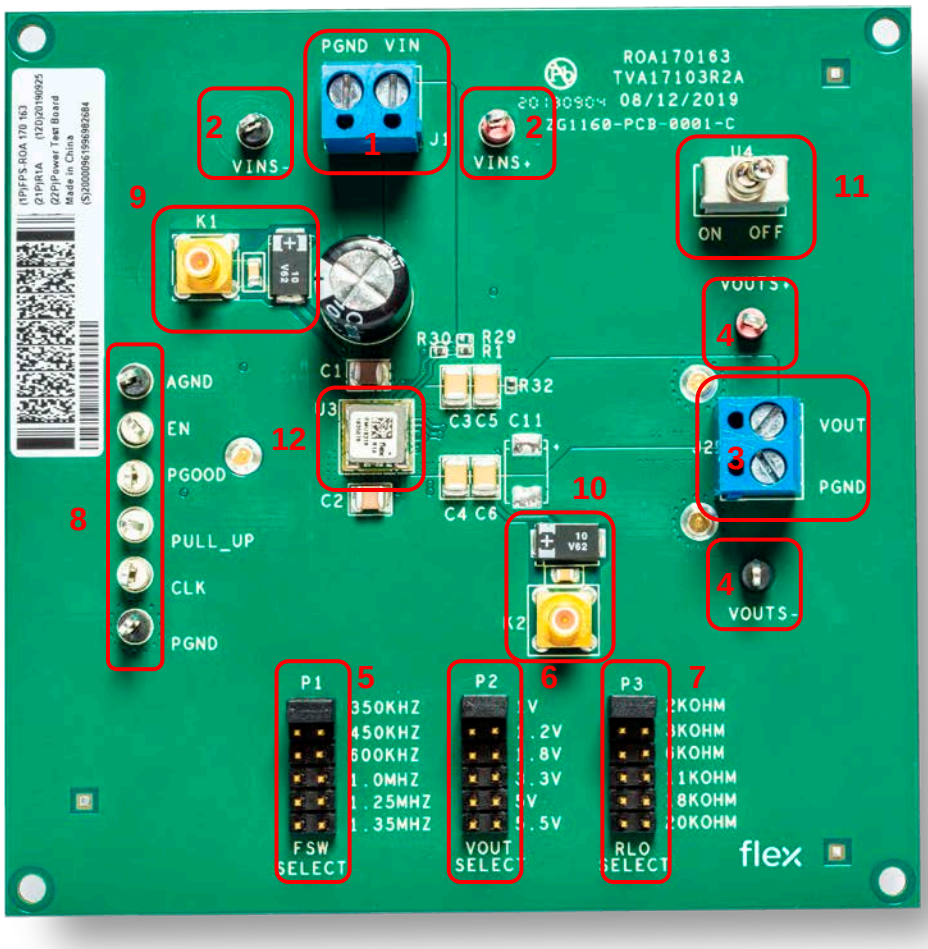


Figure 2.1 Top side of the evaluation board ROA 170 163.

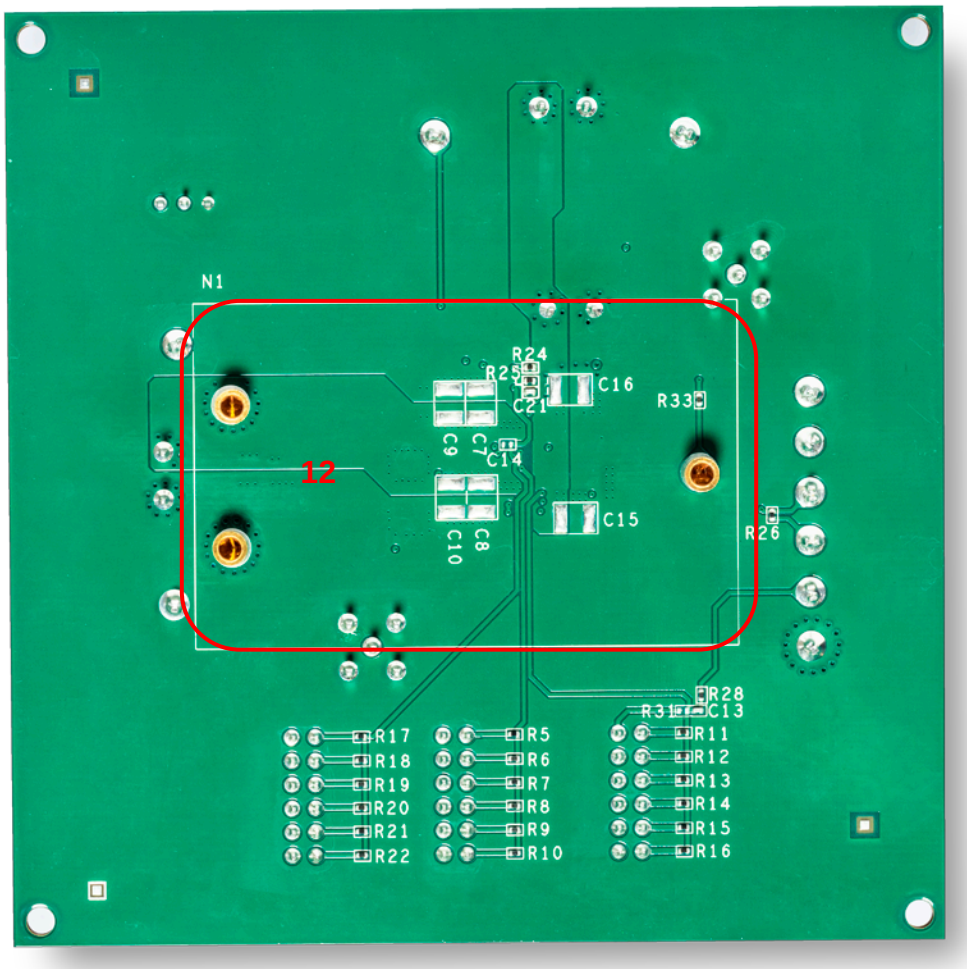


Figure 2.2 Bottom side of the evaluation board ROA 170 163.

Position Description

1 Input voltage connectors, VIN/PGND

2 Input voltage sense points, VINS+/ VINS-

3 Output voltage connectors, VOUT/PGND

4 Output voltage connectors, VOUTS+/VOUTS-

5 Switching frequency setting, FSW SELECT

6 Output voltage setting, VOUT SELECT

7 Loop optimization setting, RLO SELECT

8 Test points, AGND, EN, PGOOD, PULL_UP, PGND

9 Input ripple test point, K1

10 Output ripple test point, K2

11 Control switch, U4

12 Position for populating Flex electronic load module ROA128 5552.

3 Instructions

3.1 Power-up/down instruction

- The module is positive logic by default
- Put the switch U4 in on position with input power to turn on the device
- Put the switch U4 in off position with input power to turn off the device

3.2 EN instruction

Connect a resistor divider to EN pin to implement adjustable under voltage lockout and hysteresis. The resistor divider R24 and R25 are placed on the bottom side of the test board. The default UVLO value is set to 4.5V. Please refer to PMU Technical Specification for more options.

3.3 Output voltage, switching frequency and loop optimization settings

The FSW SELECT (P1), VOUT SELECT (P2) and RLO SELECT (P3) jumpers are provided for selecting the appropriate switching frequency, output voltage and loop optimization resistors. Before applying power to the test board, ensure the jumpers are present and placed in intended values. Make sure the input power has been removed before changing the jumper settings.

See Table 1 for default pin-strap settings of switching frequency, output voltage and loop optimization.

Table 1 Default settings on ROA 170 163

VOUT SELECT	FSW SELECT	RLO SELECT
1.0V	350KHz	2KΩ
1.2V	450KHz	3KΩ
1.8V	600KHz	6KΩ
3.3V	1.0MHz	11KΩ
5.0V	1.25MHz	18KΩ
5.5V	1.35MHz	20KΩ

- NOTE that output voltage adjustable range is from 0.6V to 5.5V.
- For a fixed output voltage, choosing a value between 200KHz to 1.6MHz as fixed switching frequency. Performance of the device is only guaranteed by the default switching frequency for corresponding output voltage. Please refer to PMU Technical Specification for selection guidance when applying different values.
- Same for loop optimization resistor R_{LO}, performance of the device is only guaranteed by the default values. Please refer to PMU Technical Specification for selection guidance when applying different values.

4 Test Points

Input voltage should be measured at test points VINS+/ VINS- which are directly connected to the VIN/PGND pins of the device.

Output voltage should be measured at test points VOUTS+/ VOUTS- which are directly connected to the VOUT/PGND pins of the device.

- Position R30 for sense resistor is remained on top of the board with default value 0Ω.
- A 10Ω sense resistor is recommended for R30 when applying loop measurement.

Input ripple test point K1 and output ripple test point K2 are provided. Each consists of a 100nF ceramic capacitor and a 10uF polymer capacitor.

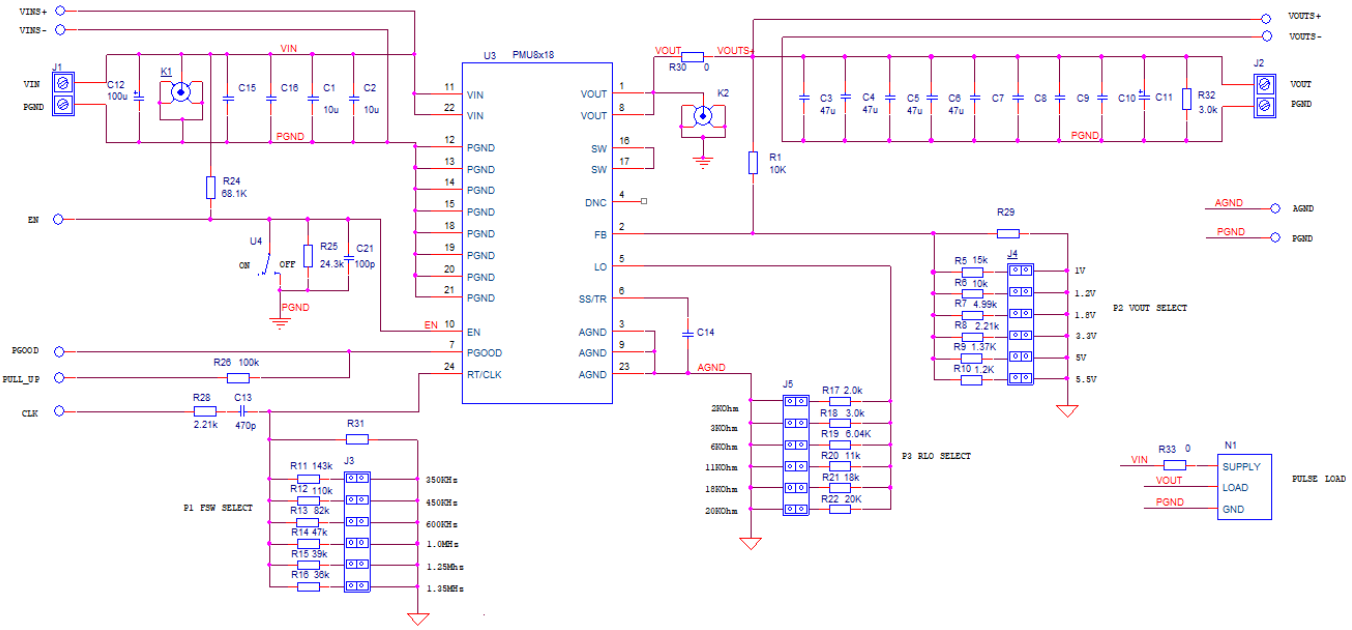
Power good signal could be measured at test point PGOOD. To implement the feature, an external voltage below 6.5V must be applied to the PULL_UP test point. Pull up resistor R26 is on the bottom side of the test board.

An external clock is allowed on point CLK to realize synchronization feature. A series RC circuit consisted of R28 and C13 are used on the bottom side of the board to interface RT/CLK pin. Note that the series RC circuit is not recommended if the transition from CLK mode to RT mode is important.

Note: AGND and PGND is connected internally on device, please do not connect the two points on test board.

5 Schematic

See schematic of Evaluation Board ROA 170 163 for more information.



6 Bill of Materials

Designator	Qty	Value	Description	Package Reference
C1, C2	2	10 µF	10% 50V X7R,CAPACITOR	1210
C3, C4, C5, C6	4	47 µF	20% 10V X7R, CAPACITOR	1210
C12	1	100 µF	20% 50V, CAPACITOR	Radial
C13	1	470 pF	5% 50V C0G,CAPACITOR	0402
C21	1	100 pF	1% 50V C0G,CAPACITOR	0402
R1, R6	2	10 K	1% 0.063W, RESISTOR	0402
R5	1	15 K	1% 063W, RESISTOR	0402
R7	1	4.99 K	1% 0.063W, RESISTOR	0402
R8, R28	2	2.21 K	1% 0.063W, RESISTOR	0402
R9	1	1.37 K	1% 0.063W, RESISTOR	0402
R10	1	1.2 K	1% 0.063W, RESISTOR	0402
R11	1	143 K	1% 0.063W, RESISTOR	0402
R12	1	110 K	1% 0.063W, RESISTOR	0402
R13	1	82 K	1% 0.063W, RESISTOR	0402
R14	1	47 K	1% 0.063W, RESISTOR	0402
R15	1	39 K	1% 0.063W, RESISTOR	0402
R16	1	36 K	1% 0.063W, RESISTOR	0402
R17	1	2.0 K	1% 0.063W, RESISTOR	0402
R18, R32	1	3.0 K	1% 0.063W, RESISTOR	0402
R19	1	6.04 K	1% 0.063W, RESISTOR	0402
R20	1	11 K	1% 0.063W, RESISTOR	0402
R21	1	18 K	1% 0.063W, RESISTOR	0402
R22	1	20 K	1% 0.063W, RESISTOR	0402
R24	1	68.1 K	1% 0.063W, RESISTOR	0402
R25	1	24.3 K	1% 0.063W, RESISTOR	0402
R26	1	100 K	1% 0.063W, RESISTOR	0402
R30, R33	2	0	+50mohm 1A, RESISTOR	0402
C15, C16	0	OPEN	X7R, CAPACITOR	1210
C7, C8, C9, C10	0	OPEN	X7R, CAPACITOR	1210
C11	0	OPEN	Tantalum Polymer, SMD	7343-40
C14	0	OPEN	X7R,CAPACITOR	0402
R29	0	OPEN	1% 0.063W, RESISTOR	0402
R31	0	OPEN	1% 0.063W, RESISTOR	0402

7 Layout description

The following sections describe how the layout guidelines provided in the PMU Technical Specification have been applied to the Evaluation Board layout. The purpose is to give the reader a better understanding of the guidelines by examples. Please note that every system is different and that there may well be considerations to make which are not provided here, depending on the system requirements and limitations set in the end application.

7.1 PCB stack-up summary

Layer	Description	Thickness
Top layer	VIN, VOUT, PGND planes Component footprints, signal traces	2 oz
Layer 2	PGND plane	2 oz
Layer 3	VOUT, PGND, AGND planes Signal traces	2 oz
Bottom layer	VIN, VOUT, PGND planes Component footprints, signal traces	2 oz

7.2 Power pins

Refer to Figure 7.1. The power pins (VIN, VOUT and PGND) should connect with low impedance to internal power planes in order to:

- Provide effective heat spread from module to the application board.
- Provide low electrical impedance to input and output capacitors, minimizing the input and output ripple levels.
- Provide a low resistance path for input and output current of the module, lowering the resistive losses.

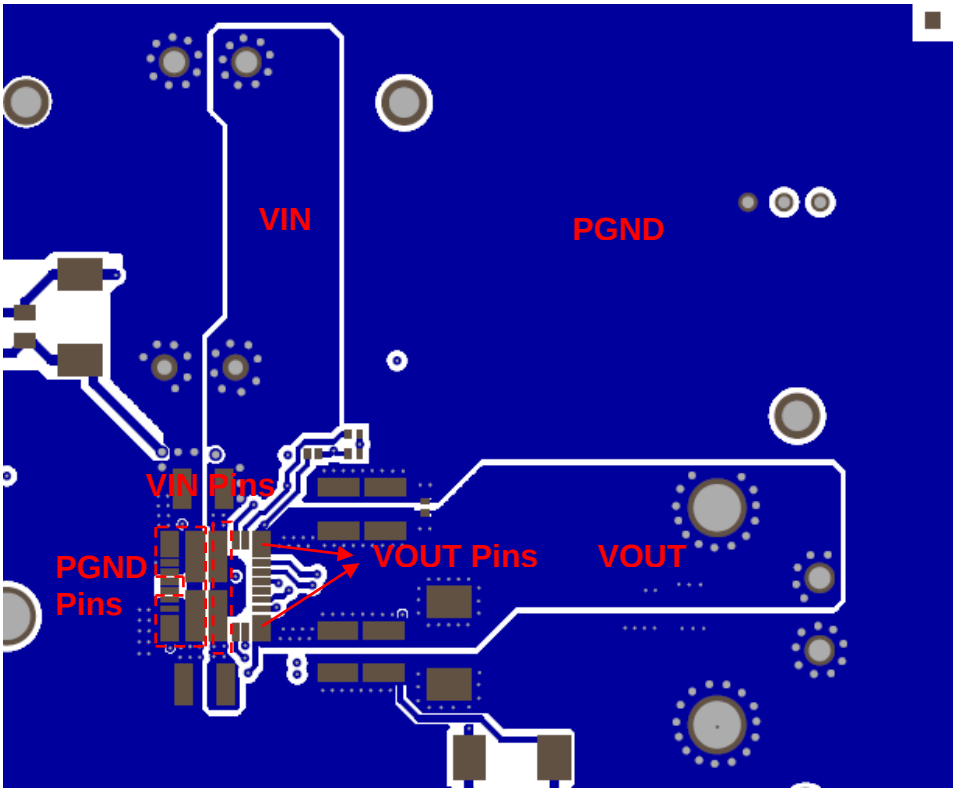


Figure 7.1 Connection of power pins on top layer

7.3 Input capacitance

Refer to Figure 7.2. The ceramic input capacitors should be placed as close as possible to the VIN/GND pins on both sides of the module in order to minimize the connection impedance. For the same reason, multiple vias are placed close to the capacitors' terminals, utilizing inner layers to connect to input pins of the module.

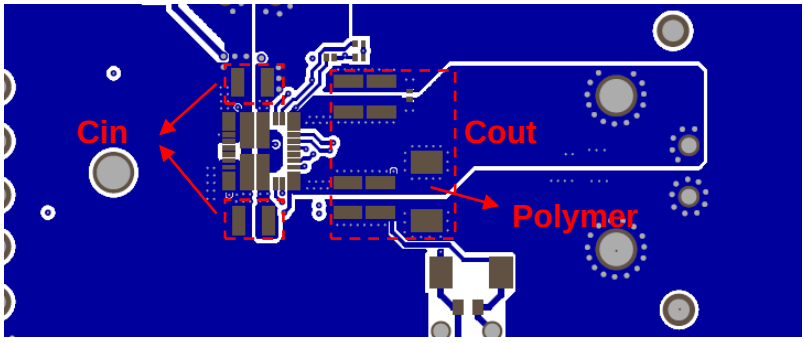


Figure 7.2 Input and output capacitors

Note that input capacitors are also placed on the bottom side of the board, at the same locations as the capacitors shown in Figure 7.2.

Placement and connections of the larger bulk input capacitor (used mainly to hold up the input voltage during large load transients or changes in input voltage) follows the rules of the ceramics described above. However, in this case low impedance is not as critical due to the slower action, so the capacitor can be placed “behind” the ceramic input capacitors at a larger distance from the module.

7.4 Output capacitance

Refer to Figure 7.2. Ceramic output capacitors are placed close to both VOUT pins of the module to handle the module’s output ripple. A position for polymer capacitor is provided to take care of load transient, see Technical Specification for load transient performance with different combinations of ceramic and polymer capacitors. It is important with low impedance connections (to module VOUT/GND pins or to the load’s VOUT/GND pins) and the guidelines described above for the input capacitors are applied.

Note that output capacitors are also placed on the bottom side of the board, at the same locations as the capacitors shown in Figure 7.2.

Further it is important to use planes to distribute the output current to the load in order to minimize losses and the effective output impedance, providing good conditions for the module’s control loop to compensate for load transient.

See layout top view of ROA 170 163 for more information.

8 Layout top view

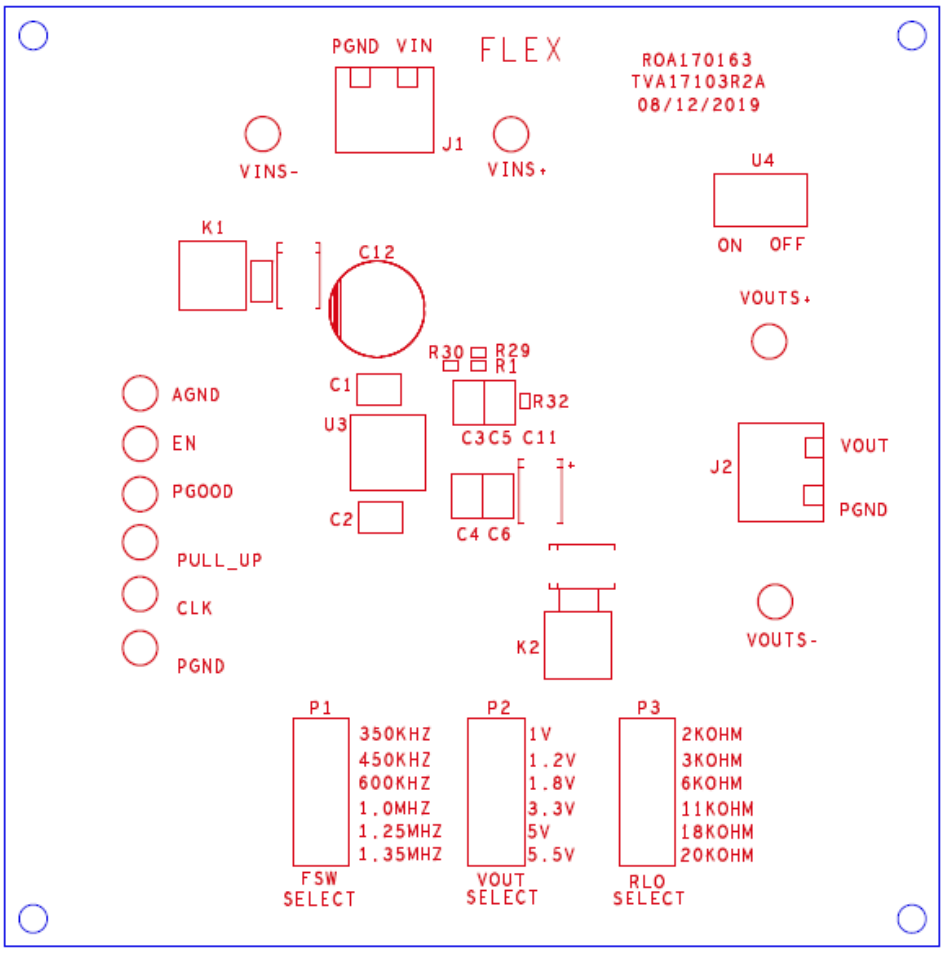


Figure 8.1 Top side component layout

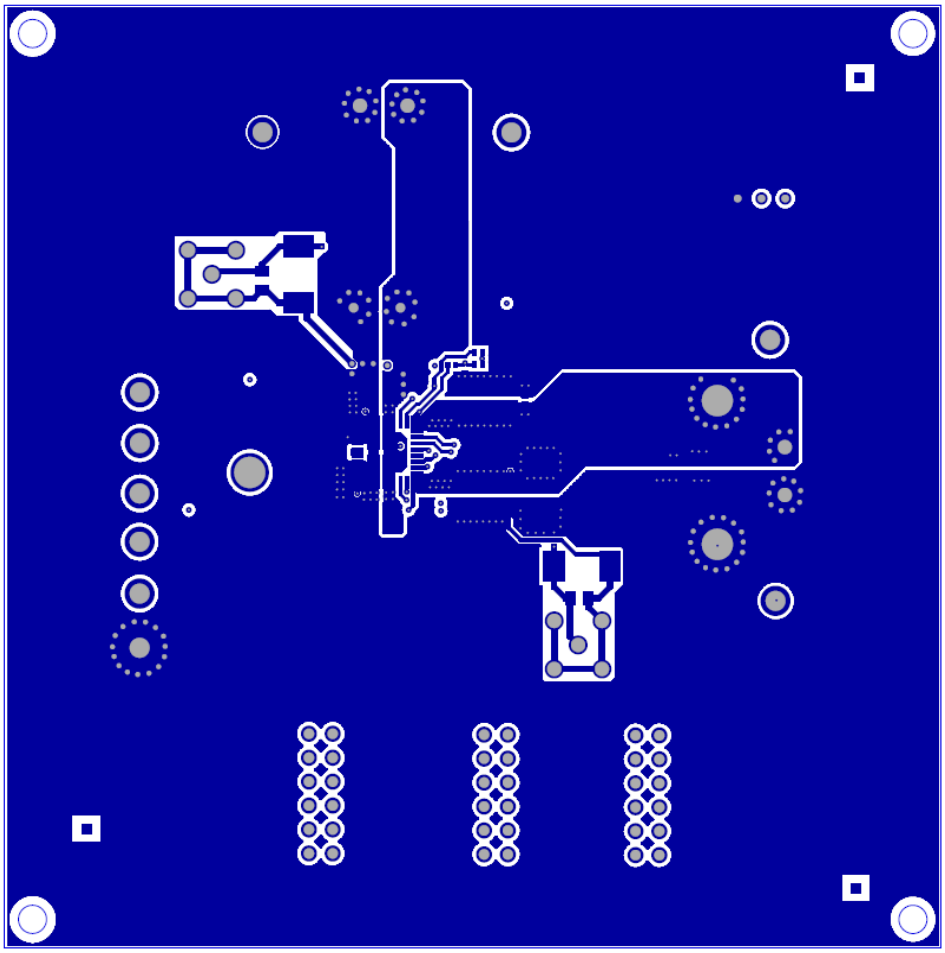


Figure 8.2 Top layer

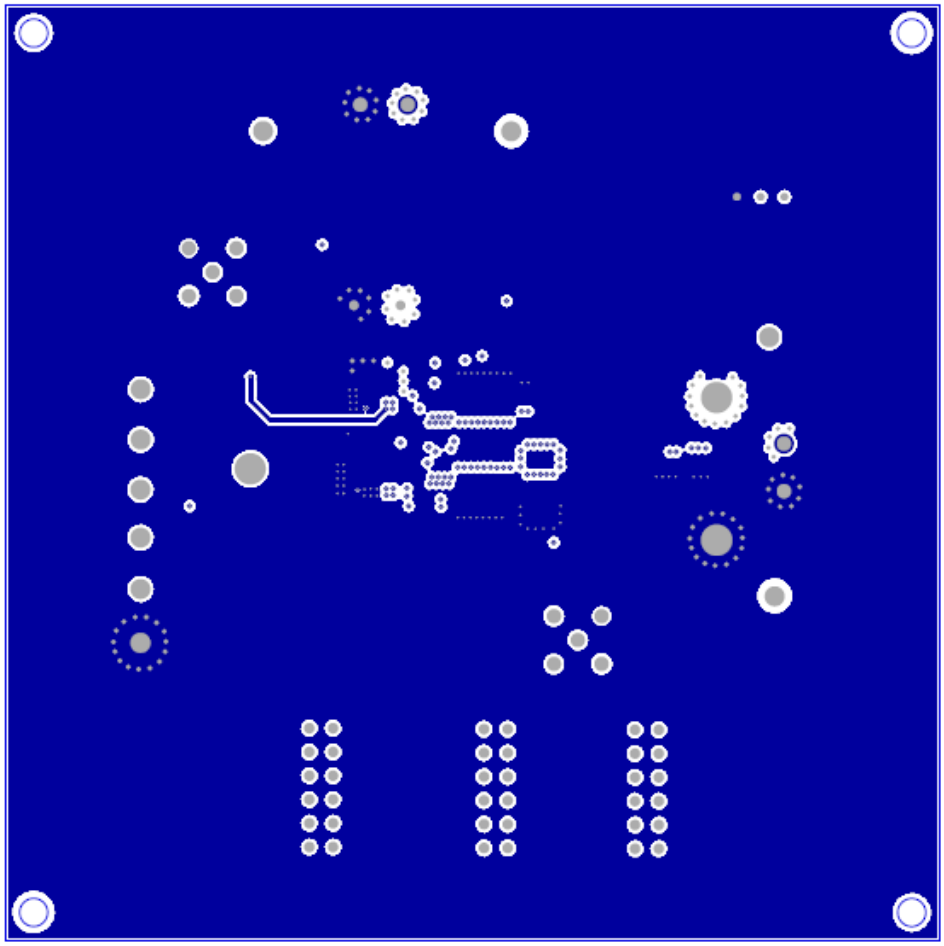


Figure 8.3 Layer 2

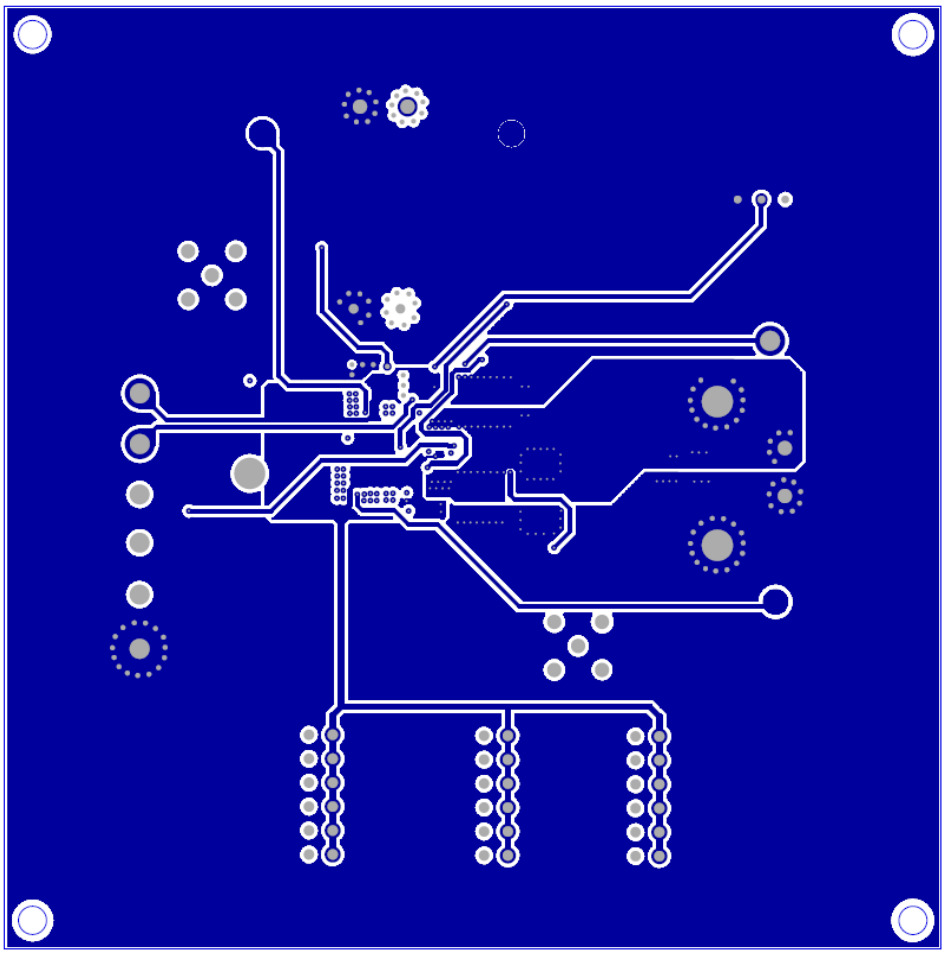


Figure 8.4 Layer 3

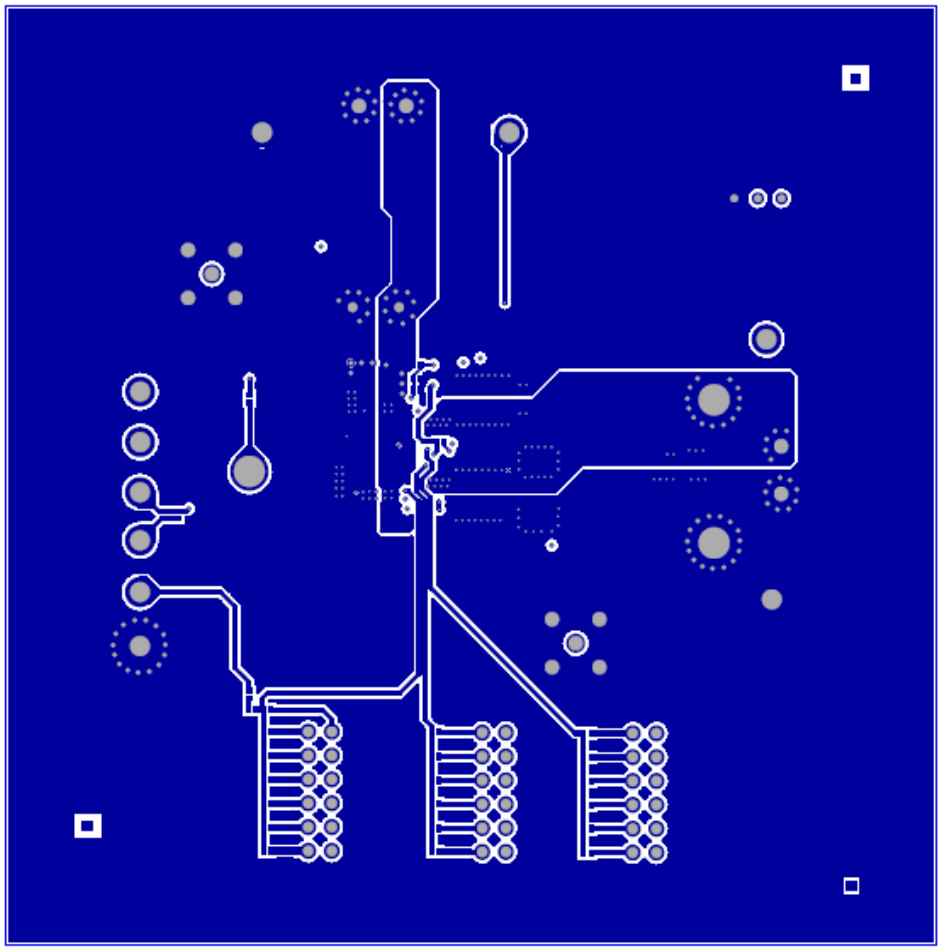


Figure 8.5 Bottom layer

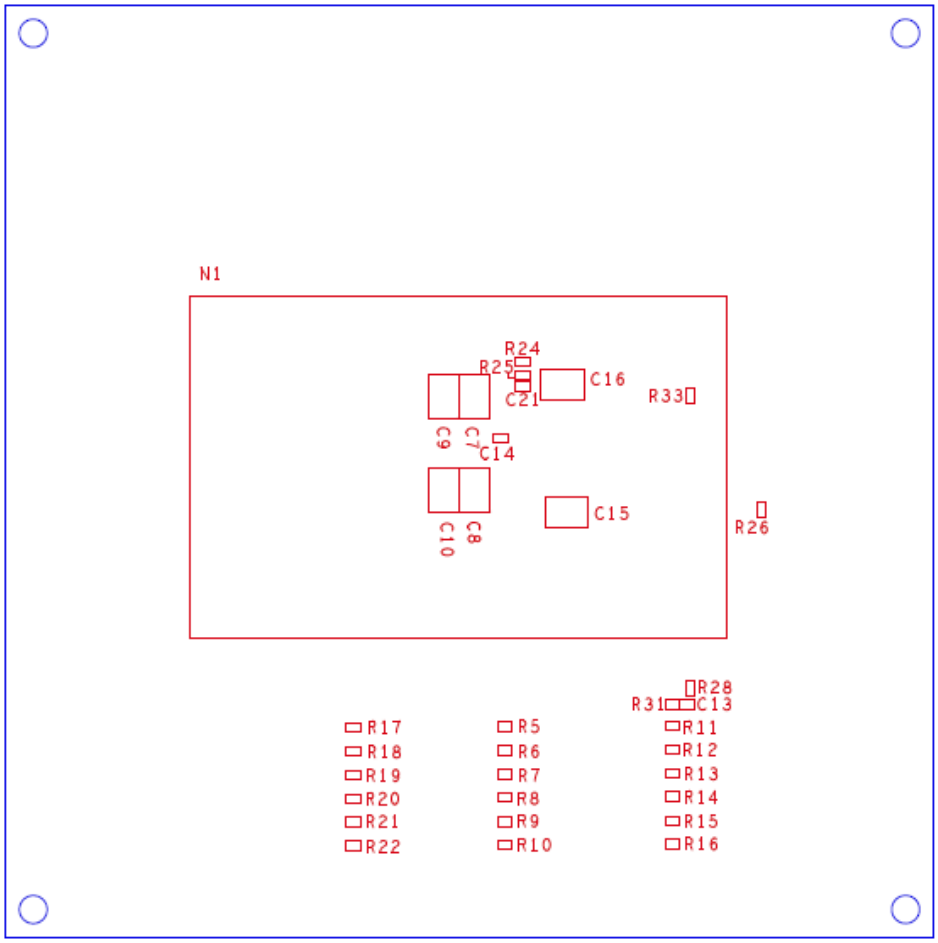


Figure 8.6 Bottom side component layout