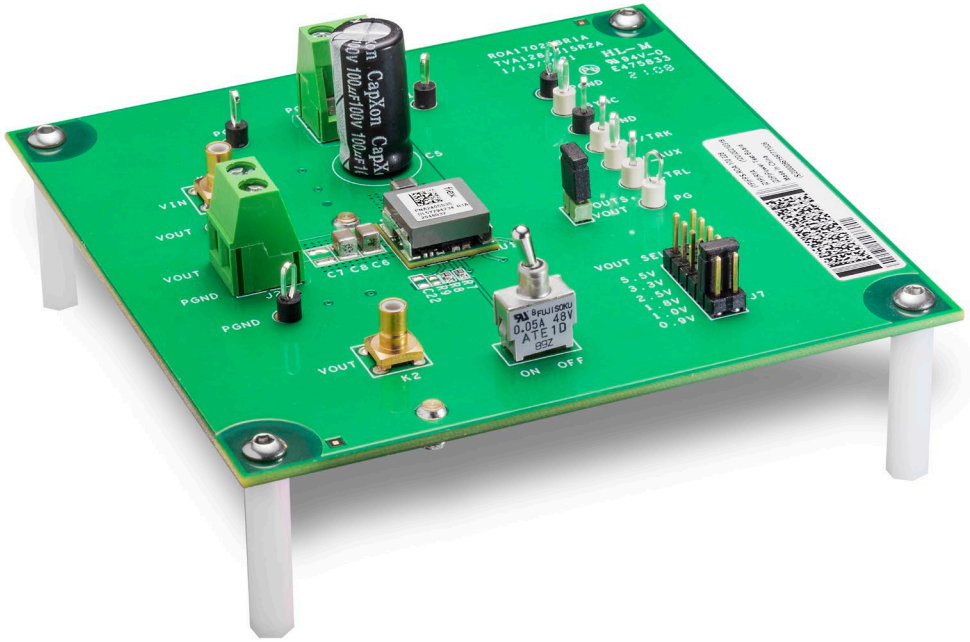
Evaluation board PNA

ROA 170 228

USER GUIDE



Contents

1 Introduction

This User Guide provides a brief introduction and instruction on how to use the Reference Board ROA 170 228. This board facilitates evaluation of a PNA 2405S3S module.

The User Guide also provides a description of how the layout guidelines provided in the PNA 2405S3S Technical Specification have been applied to the reference board layout.

1.1 How to contact Flex

For general questions or interest in our products, please contact your local sales representative. Contact details are available from our website: www.flexpowermodules.com

The Reference Board ROA 170 228 features PNA 2405S3S synchronous buck converter modules operating with 9 V to 36 V input voltage range. The output voltage can be set to six typical values be using a configuration jumper.

Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line regulation, load regulation, and transient response. Control test points are provided for use of SYNC, SS/TRK and CTRL features of the device.

Input and output capacitors are included on the board for the entire range of input and output voltages. Component footprints are provided for adjusting the capacitor combinations and using the main features of the device.

2 Reference Board ROA 170 228

Power the board by connecting 9-36 V DC power to the “VIN” and “PGND” connectors.

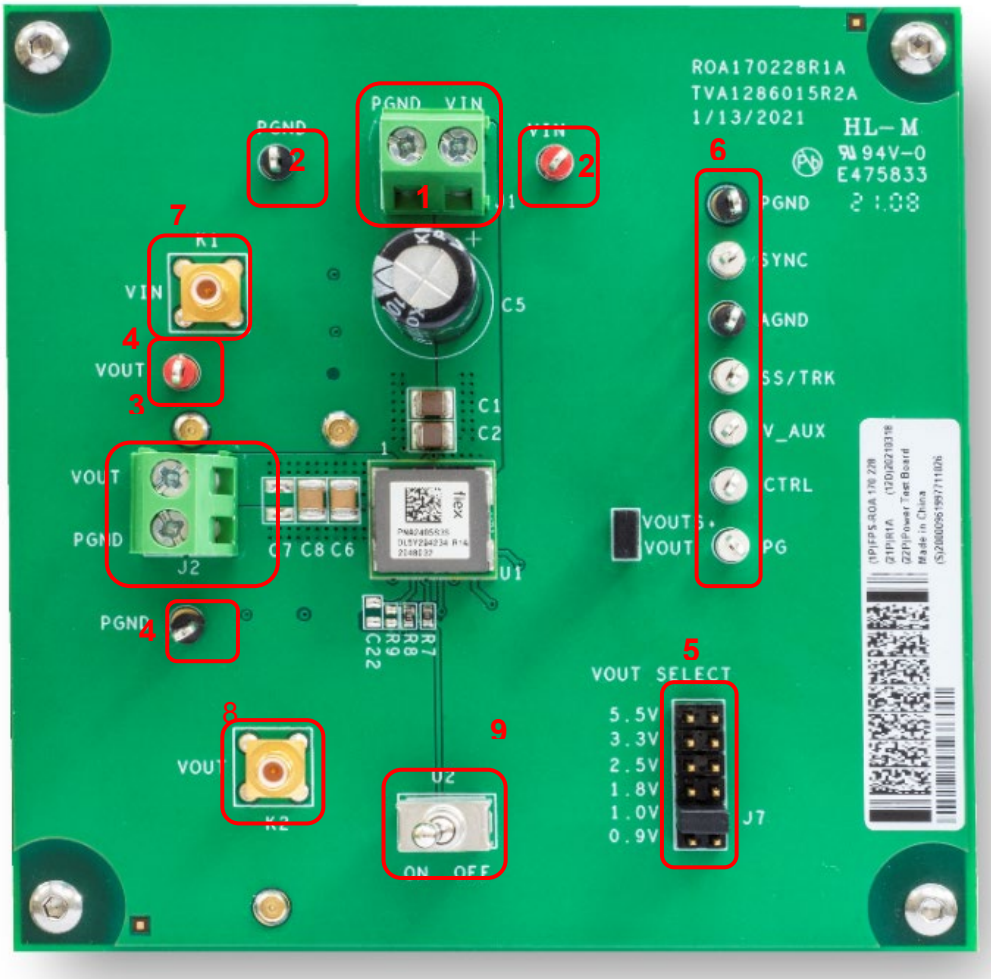


Figure 2.1 Top side of the reference board ROA 170 228.

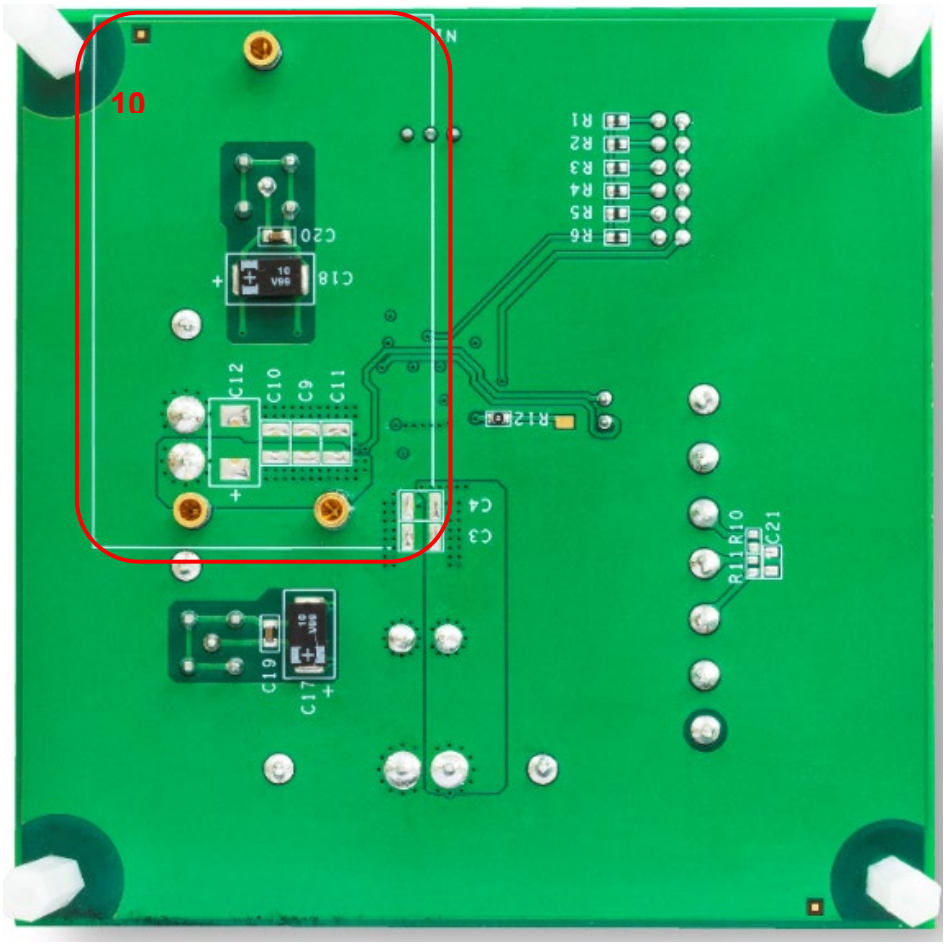


Figure 2.2 Bottom side of the reference board ROA 170 228

Position Description

1 Input voltage connectors, VIN/PGND

2 Input voltage test points, VIN/ PGND

3 Output voltage connectors, VOUT/PGND

4 Output voltage test points, VOUT/PGND

5 Output voltage setting, VOUT SELECT

6 Test points, PGND, SYNC, AGND, SS/TRK, V_AUX, CTRL, PSG

7 Input ripple test point, K1

8 Output ripple test point, K2

9 Control switch, U2

10 Position for populating Flex electronic load module ROA 128 5552

3 Instructions

3.1 Power-up/down instruction

- The module is positive logic by default
- Put the switch U2 in ON position with input power to turn on the device
- Put the switch U2 in OFF position with input power to turn off the device

3.2 CTRL instruction

Connect a resistor divider to EN pin to implement adjustable under voltage lockout and hysteresis. The resistor divider R7 and R8 are placed on the top side of the reference board. The default UVLO value is set to 7V. Please refer to PNA 2405S3S Technical Specification for more options.

Figure 3.1 Position of R7 and R8 on top side

3.3 Output voltage setting

The VOUT SELECT jumpers are provided for selecting the output voltage. Before applying power to the reference board, ensure the jumpers are present and placed in intended values. Make sure the input power has been removed before changing the jumper settings.

See Table 1 for default pin-strap settings of output voltage.

Table 1 Default settings on ROA 170 228

VOUT SELECT	R_{SET} SELECT
0.9V	80.6 KΩ
1.2V	39.2 KΩ
1.8V	8.2 KΩ
3.3V	4.7 KΩ
5.0V	3.24 KΩ
5.5V	1.8 KΩ

- NOTE that output voltage adjustable range is from 0.9V to 5.5V. Please refer to PNA 2405S3S Technical Specification for selection guidance of voltage setting resistor value R_{SET}.

4 Test Points

Input voltage should be measured at test points VIN/ PGND which are directly connected to the VIN/PGND pins of the device.

Output voltage should be measured at test points VOUT/ PGND which are directly connected to the VOUT/PGND pins of the device.

- A 47Ω positive sense resistor is placed internally on device. A jumper is provided to short VOUT and VOUTS+.

Input ripple test point K1 and output ripple test point K2 are provided. Each consists of a 100nF ceramic capacitor and a 10uF polymer capacitor.

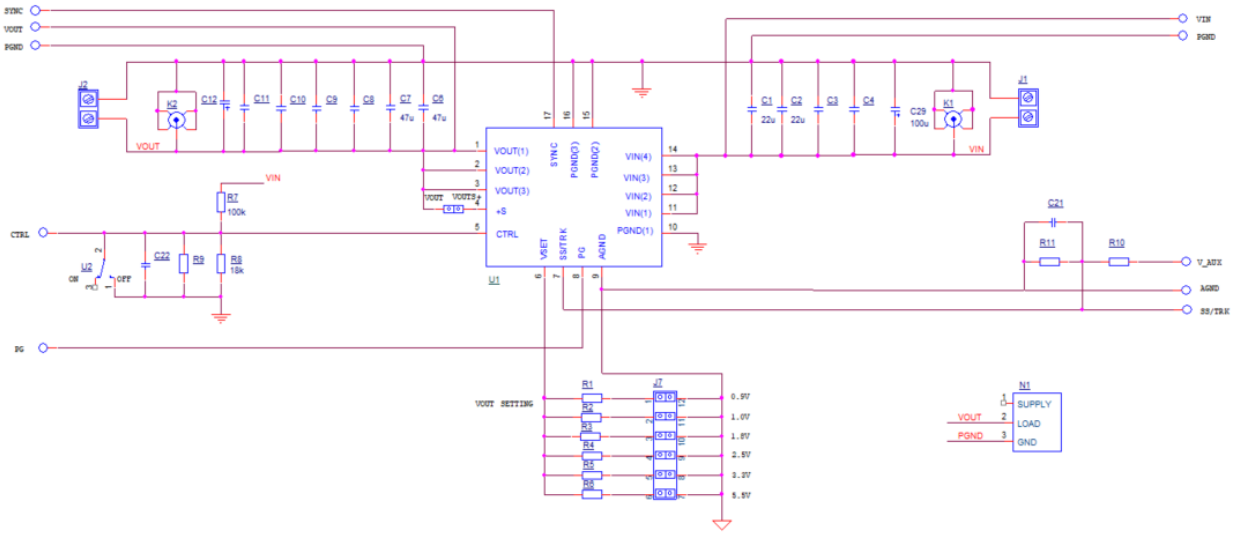
An external clock is allowed on point SYNC to realize synchronization feature. Power good signal could be measured at test point PG.

Soft start time setting is provided with C21 on pin SS/TRK. This pin also allows output voltage tracking with network C21, R10 and R11 applied. Please refer to PNA 2405S3S Technical Specification for more information.

Note: AGND and PGND is connected internally on device, please do not connect the two points on reference board.

5 Schematic

See schematic of Reference Board ROA 170 228 for more information.



6 Bill of Materials

Designator	Qty	Value	Description	Package Reference
C1, C2	2	4.7 µF	10% 50V X7R,CAPACITOR	1210
C6, C8	2	47 µF	20% 10V X5R, CAPACITOR	1210
C5	1	100 µF	100V, ELECTROLYTIC CAPACITOR	Through hole
C17, C18	2	10 µF	Tantalum Polymer, 20V, CAPACITOR	2917
C19, C20	2	100 nF	10% 50V X7R,CAPACITOR	0603
R1	1	80.6 K	1% 0.063W, RESISTOR	0402
R2	1	39.2 K	1% 0.063W, RESISTOR	0402
R3	1	8.2 K	1% 0.063W, RESISTOR	0402
R4	2	4.7 K	1% 0.063W, RESISTOR	0402
R5	1	3.24 K	1% 0.063W, RESISTOR	0402
R6	1	1.8 K	1% 0.063W, RESISTOR	0402
R7	1	100 K	1% 0.063W, RESISTOR	0603
R8	1	18 K	1% 0.063W, RESISTOR	0603
R9	1	OPEN	RESISTOR	0603
R12	1	0	+50mohm 1A, RESISTOR	0402
C3, C4，C9, C10, C11	5	OPEN	CAPACITOR	1210
C12	1	OPEN	Tantalum Polymer, CAPACITOR	2917
C22	1	OPEN	CAPACITOR	0805

7 Layout description

The following sections describe how the layout guidelines provided in the PNA 2405S3S Technical Specification have been applied to the reference board layout. The purpose is to give the reader a better understanding of the guidelines by examples. Please note that every system is different and that there may well be considerations to make which are not provided here, depending on the system requirements and limitations set in the end application.

7.1 PCB stack-up summary

Layer	Description	Thickness
Top layer	VIN, VOUT, PGND planes Component footprints, signal traces	2 oz
Layer 2	VIN, PGND plane	2 oz
Layer 3	VIN, VOUT, PGND planes Signal traces	2 oz
Bottom layer	VIN, VOUT, PGND planes Component footprints, signal traces	2 oz

7.2 Power pins

Refer to Figure 7.1. The power pins (VIN, VOUT and PGND) should connect with low impedance to internal power planes in order to:

- Provide effective heat spread from module to the application board.
- Provide low electrical impedance to input and output capacitors, minimizing the input and output ripple levels.
- Provide a low resistance path for input and output current of the module, lowering the resistive loss.

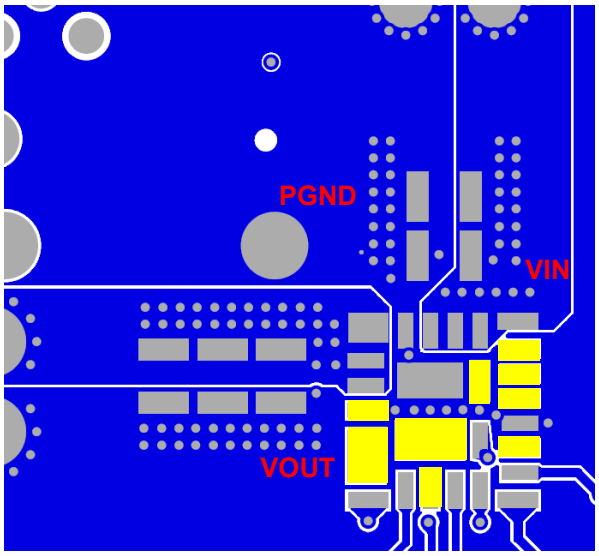


Figure 7.1 Connection of power pins on top layer

Note: Highlight pads are only for Flex internal measurement, please do not place or use these pads in end application. Please follow layout recommendations from PNA 2405S3S Technical Specification for details.

7.3 Input capacitance

The ceramic input capacitors should be placed as close as possible to the VIN/PGND pins to minimize the connection impedance. For the same reason, multiple vias are placed close to the capacitors' terminals, utilizing inner layers to connect to input pins of the module.

Note that input capacitors are also placed on the bottom side of the board, at the same locations as the capacitors shown in Figure 7.1.

Placement and connections of the larger bulk input capacitor (used mainly to hold up the input voltage during large load transients or changes in input voltage) follows the rules of the ceramics described above. However, in this case low impedance is not as critical due to the slower action, so the capacitor can be placed "behind" the ceramic input capacitors at a larger distance from the module.

7.4 Output capacitance

Ceramic output capacitors are placed close to VOUT pins of the module to handle the module's output ripple. A position for polymer capacitor is provided to take care of load transient, see Technical Specification for load transient performance. It is important to secure low impedance connections.

Note that extra positions for output capacitors are also placed on the bottom side of the board, at the same locations as the capacitors shown in Figure 7.1.

Further it is important to use planes to distribute the output current to the load in order to minimize losses and the effective output impedance, providing good conditions for the module's control loop to compensating for load transient.

See layout top view of ROA 170 228 for more information.

8 Layout top view

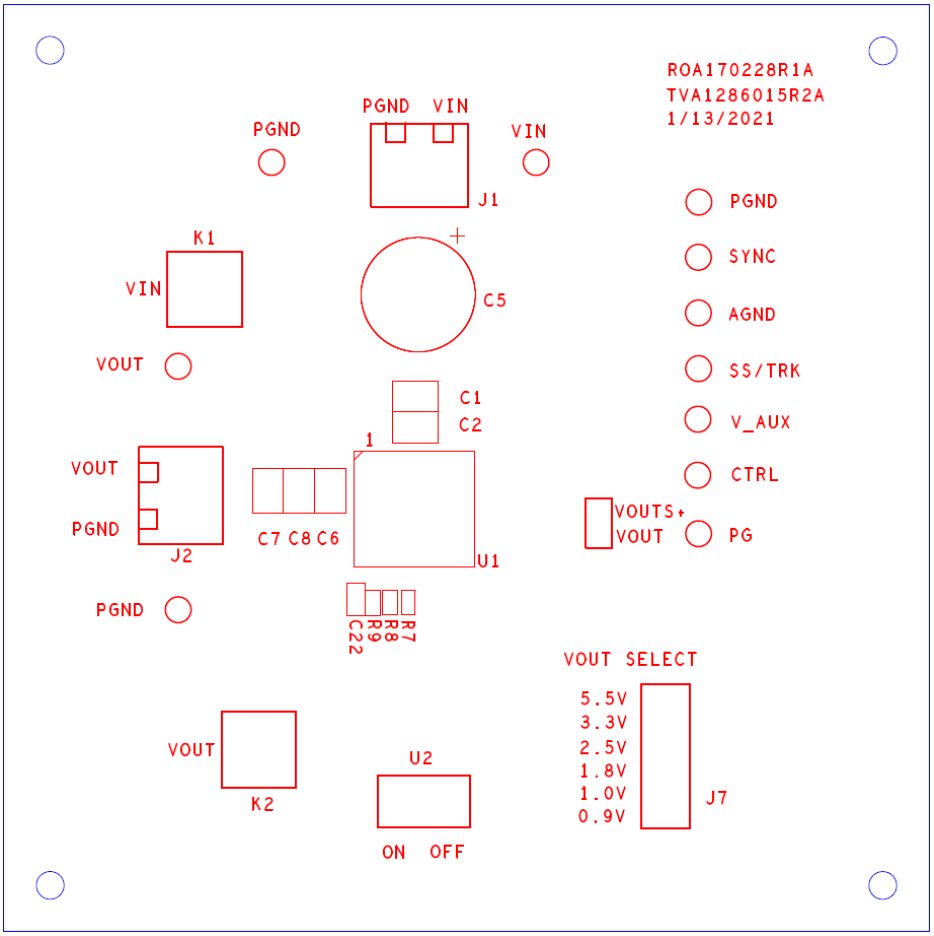


Figure 8.1 Top side component layout

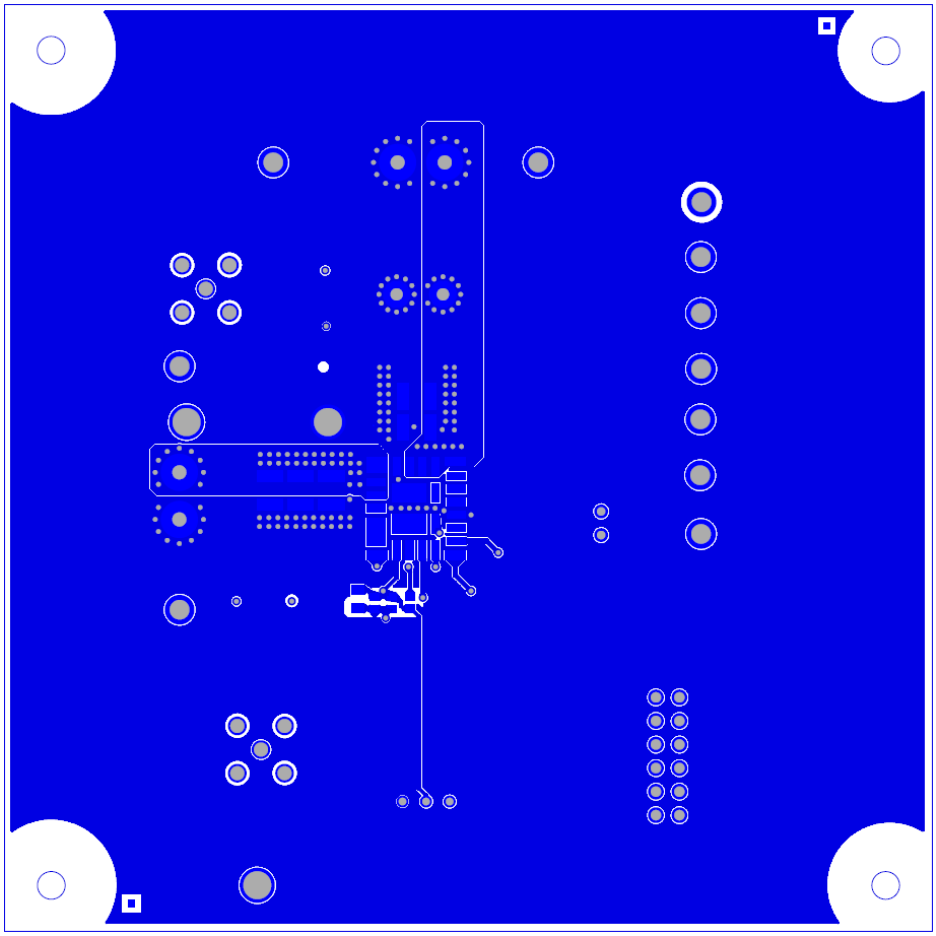


Figure 8.2 Top layer

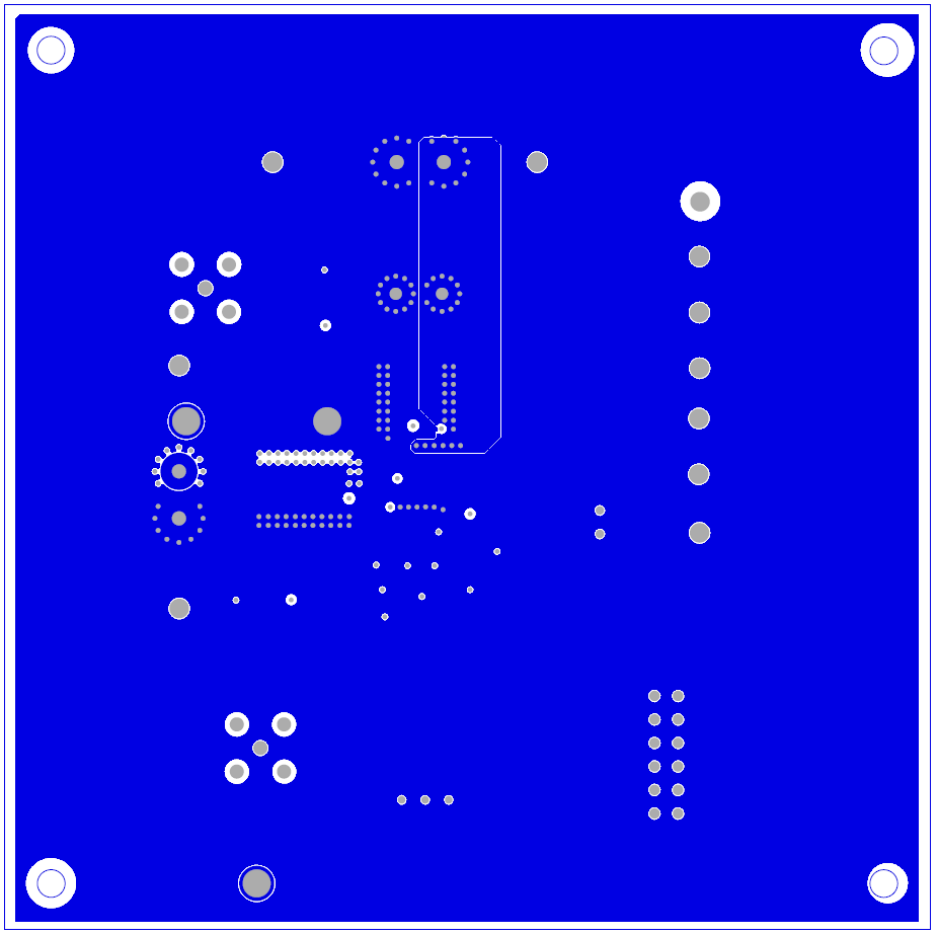


Figure 8.3 Layer 2

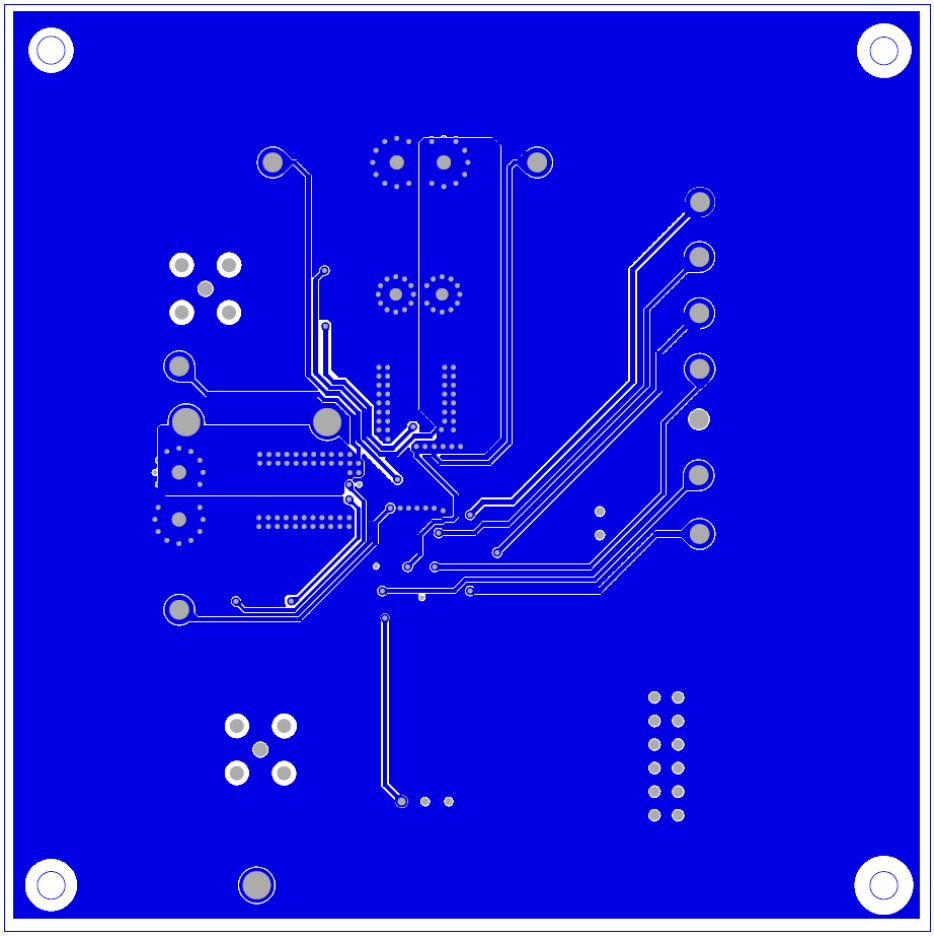


Figure 8.4 Layer 3

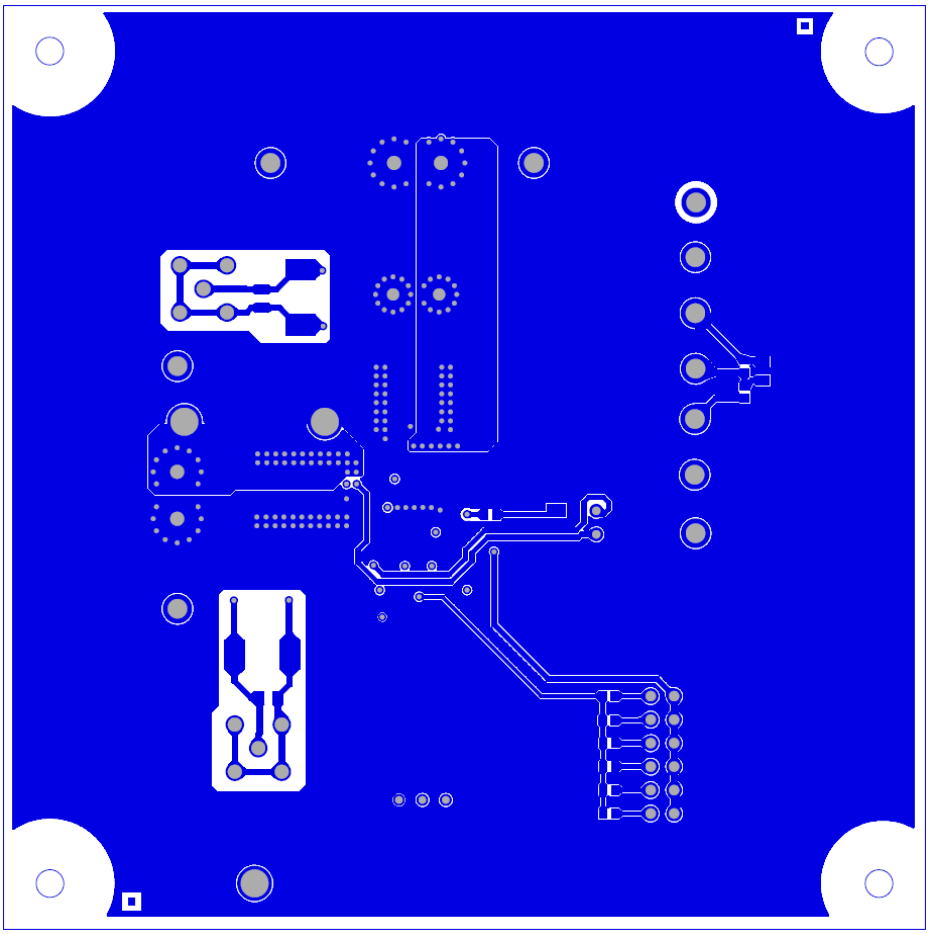


Figure 8.5 Bottom layer

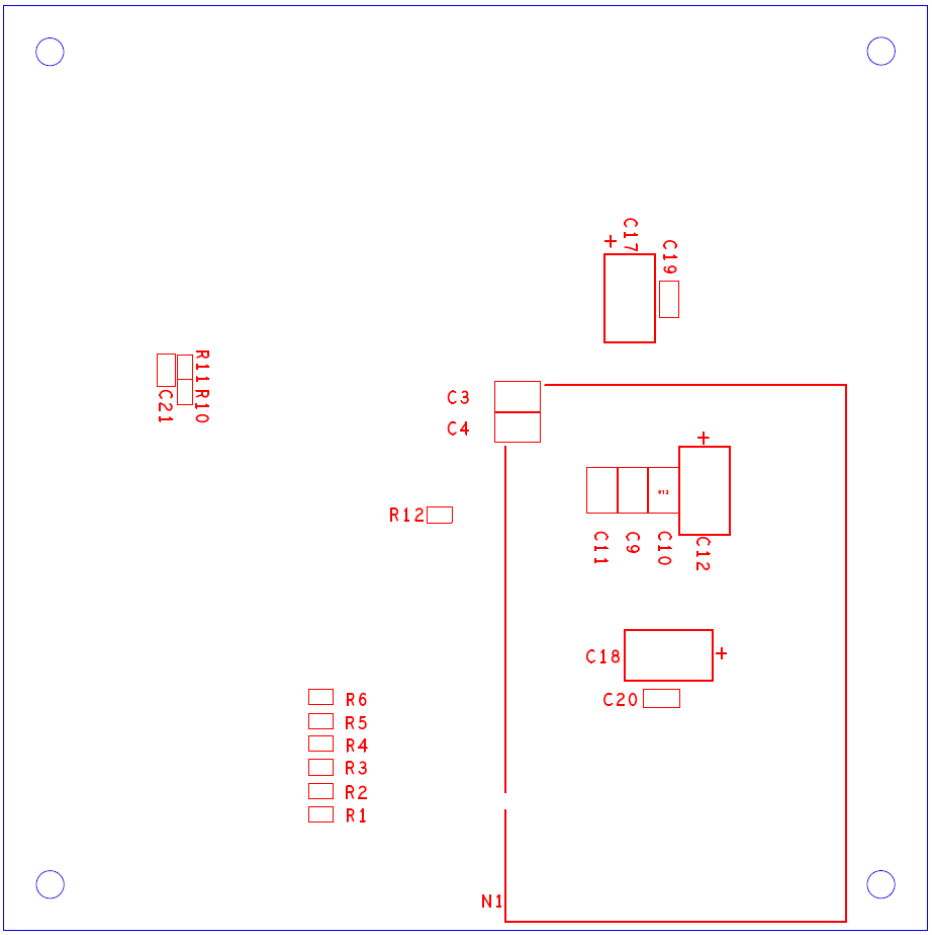


Figure 8.6 Bottom side component layout