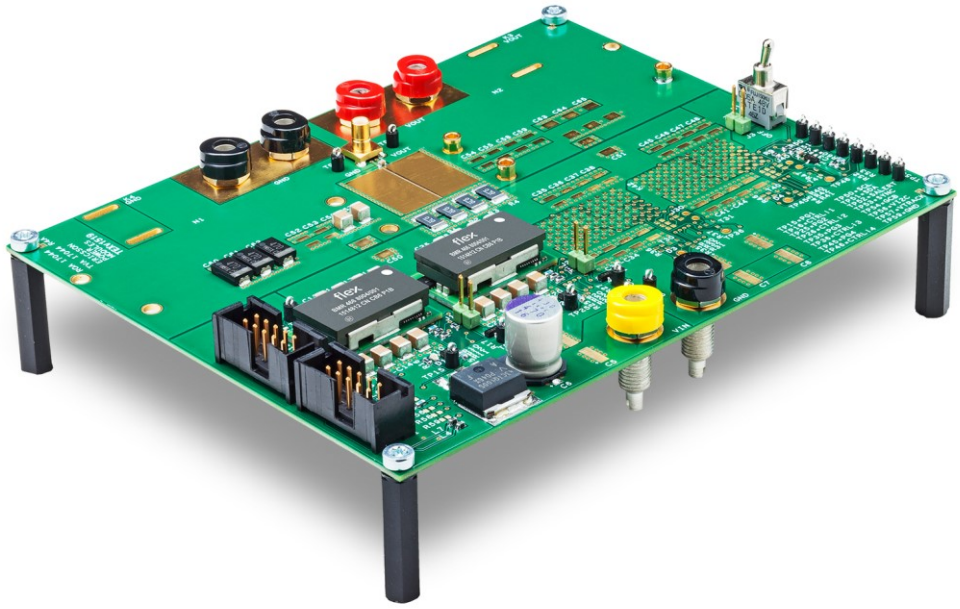
User Guide

ROA 170 44 POL BMR466 Paralleling Evaluation Board	1/28701-ROA 170 44 Rev A May 2018 © Flex

POL BMR466 Evaluation Board

ROA 170 44

User Guide



Contents

1 Introduction

This User Guide provides a brief introduction and instruction on how to use the Reference Board ROA 170 44. This board provides the possibility to evaluate the BMR 466 modules.

1.1 Prerequisites

In order to operate the ROA 170 44 board the following is needed:

- Power supply 5-14 V.
- One or more BMR 466 modules, the modules are soldered onto the board at delivery. Either 1, 2 or 4 modules are provided.
- PMBus-to-USB adaptor Flex Power KEP 910 17.
- The “Flex Power Power Designer” software package and a compatible Windows PC (see reference 1 for details). Users must be familiar with the Windows® operating system.

2 Reference Board ROA 170 44

Power the board by connecting 5-14V DC power to the “Vin” and “Gnd” connectors.

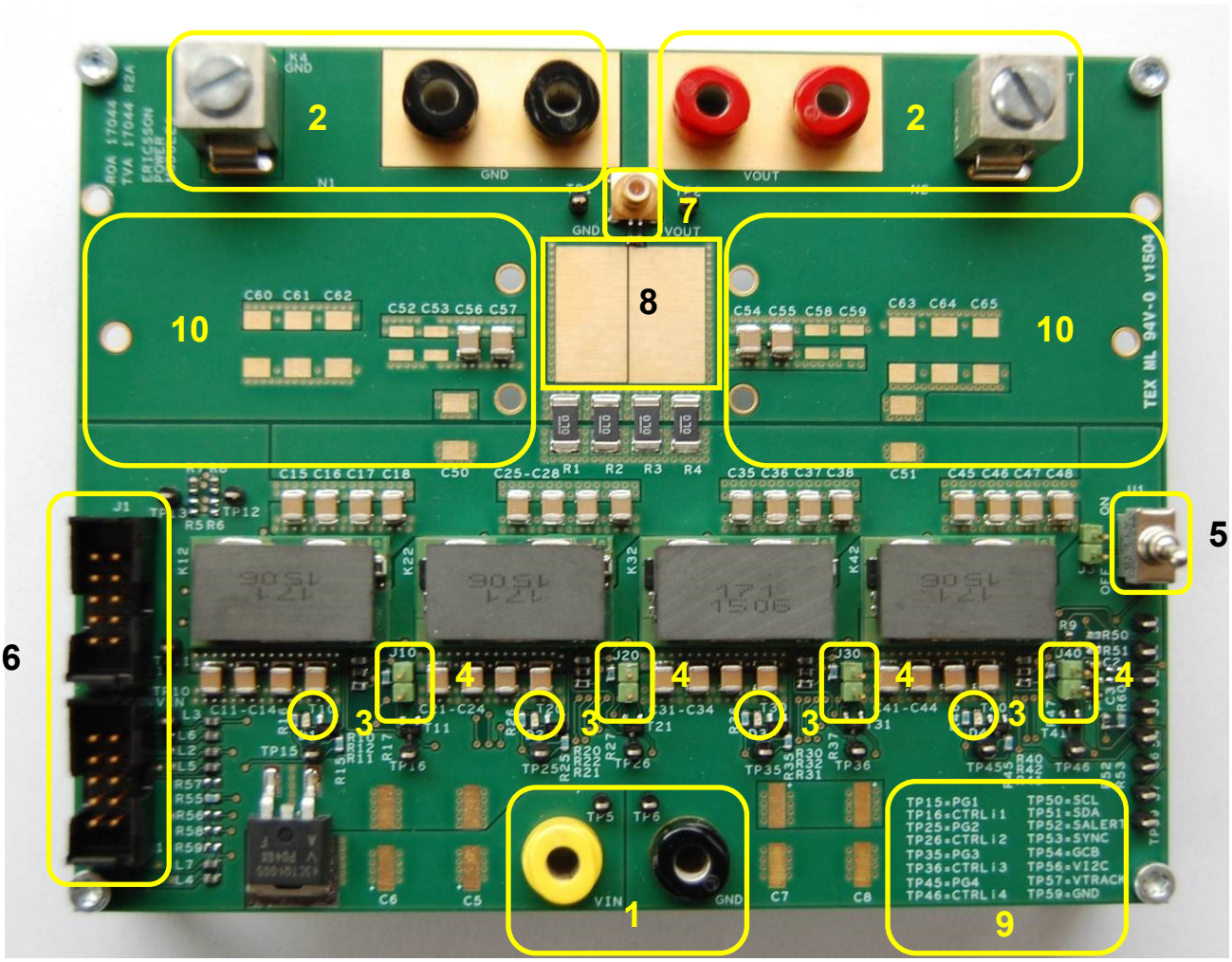


Figure 1. ROA 170 44 (top side).

Position Description

1	Input voltage connectors.
2	Output voltage connectors.
3	Power good LED:s.
4	Enable jumpers.
5	ENABLE switch.
6	Connectors for the Flex Power KEP 910 17 PMBus-to-USB adaptor.
7	SMB Oscilloscope connector.
8	Space for additional output capacitors.
9	Description of test points.
10	Positions for populating Flex Power electronic load module.

3 USB to PMBus adaptor

The USB to PMBus adaptor used with this board is the Flex Power KEP 910 17.

3.1 Connection of Flex Power KEP 910 17 USB to PMBus adaptor

Connect the Flex Power KEP 910 17 USB to PMBus adaptor, (6, Figure 1). Any of the two connectors can be used. The connector not used for the adaptor can be used to cascade several reference boards, or other Flex Power Power Modules test boards, to the same PMBus adaptor.

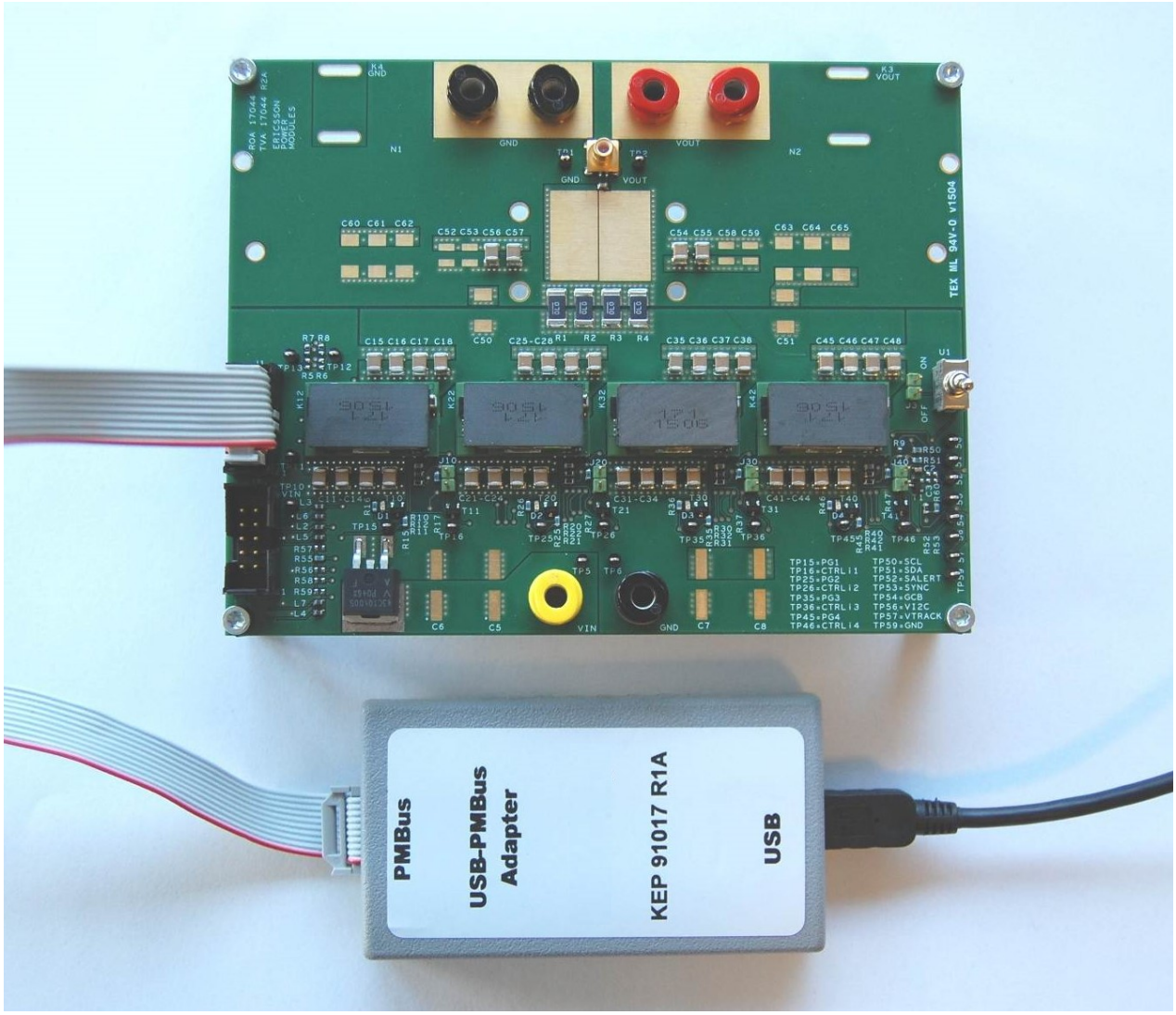


Figure 2. Connection of the Flex Power KEP 910 17 USB to PMBus adaptor.

4 Power-up and Power-down Instructions

4.1 Power-up instruction

- Make sure the enable jumpers are connected for each module position to be operated. More than one jumper shall only be populated at the same time if the modules are to be operated in current sharing mode, which requires special configurations using the Flex Power Power Designer.
- If a single module is to be operated in temperatures below ~ -10°C, the crowbar function must be disabled for those modules on the test board that will *not* be operated. This is made by setting the OVUV_CONFIG register to 0x0F, e.g. using the Flex Power Power Designer.
- Connect the PMBus Adapter/Cable to the board.
- Connect and turn on the 5-14 V supply.
- Turn the ENABLE switch in On position.
- Start the software program.
- The power good LED:s for each module should now give green light. The LED:s are controlled by PG output of each BMR 466 module, but supplied from PMBus Adapter/Cable. (For this reason the LED:s will also give green light if the PMBus Adaptor/Cable is connected, but Vin supply is not connected).

4.2 Power-down instruction

- Turn the ENABLE switch in Off position or turn Off the 5-14V supply.

5 Vset and address resistors

To change the output voltage change the resistor values as shown in fig. 5.1.

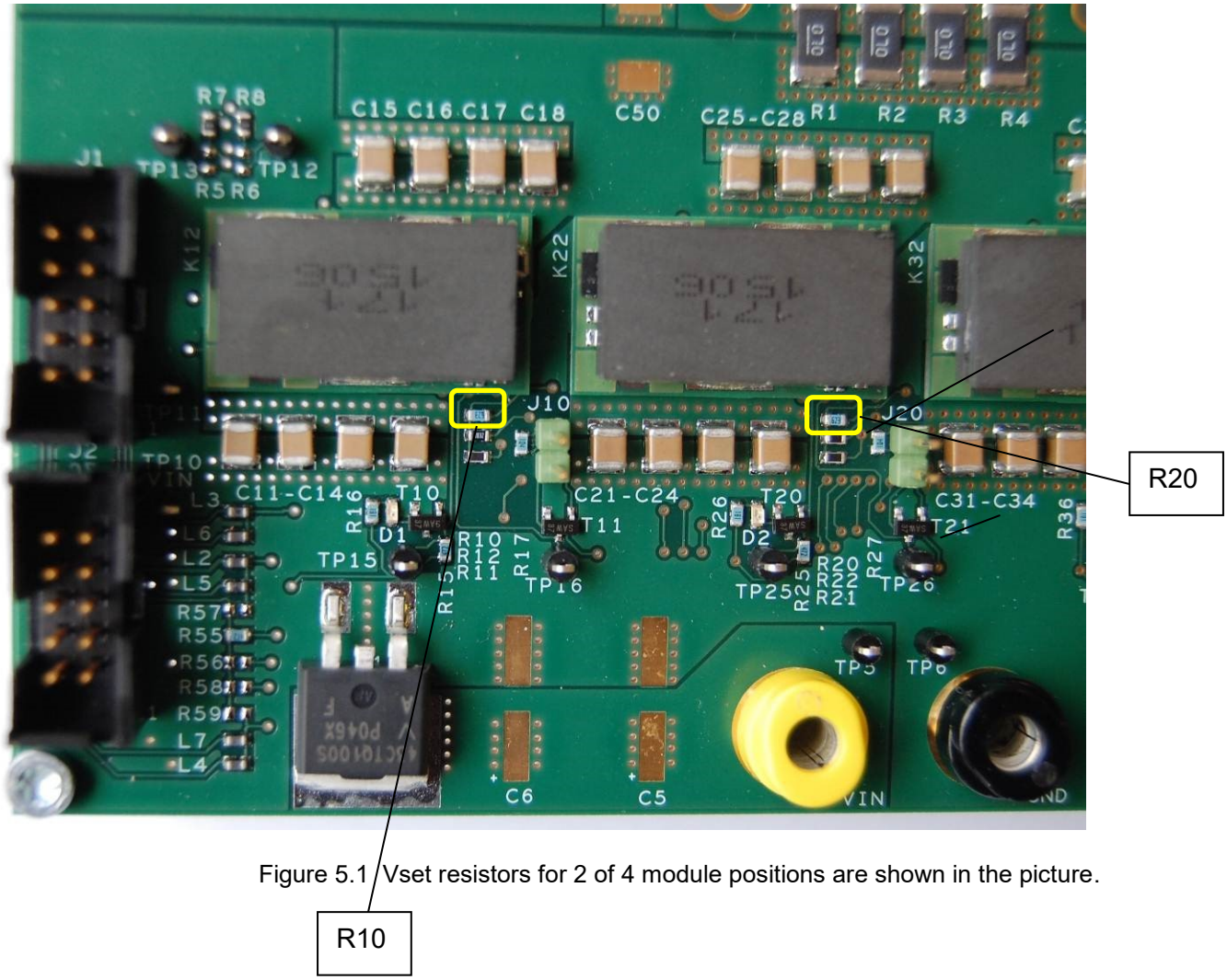


Figure 5.1 Vset resistors for 2 of 4 module positions are shown in the picture.

Resistors R10, R20, R30 and R40 can be replaced in order to change the predefined output voltage. Refer to the technical specification to select values.

5.1 Adjustment of address resistors

To change the addresses change the resistor values as shown in fig. 5.2.

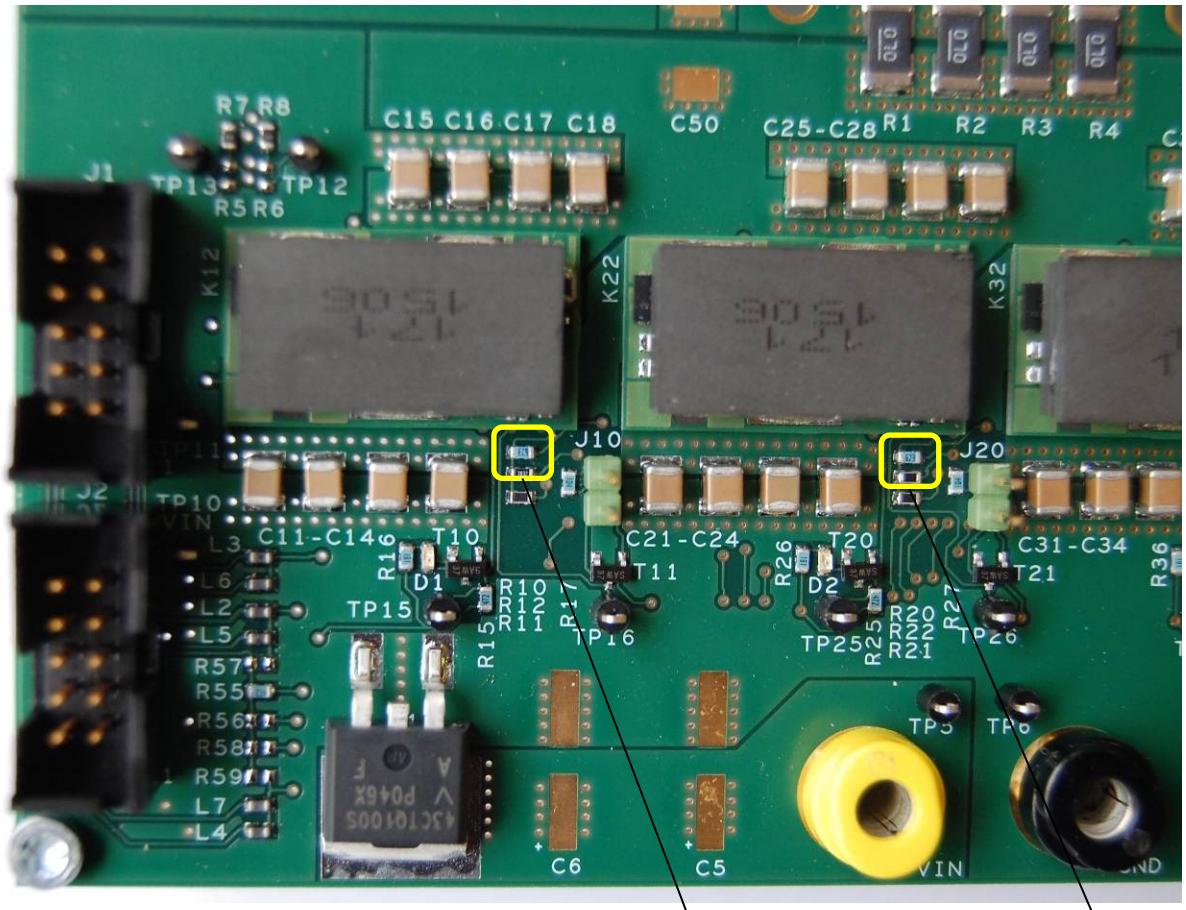


Fig 5.2 Address resistors for 2 of 4 module positions are shown in the picture.

R11/R12

R21/R22

Change resistors R11 (SA1 set) and R12 (SA0 set) to achieve the desired PMBus address for the module in the first position (K12) . Refer to chapter “PMBus addressing” in the technical specification to select the values of R11 and R12. In the same way PMBus adresses for modules in positions 2,3 and 4 (K22, K32 and K42) can be changed.

6 Test Points

Input voltage should be measured at test points TP5/TP6 which are connected directly to the VIN connectors of the board. Alternative test points for Vin close to module K12 are TP10/TP11.

Output voltage should be measured at test points TP1/TP2 which are connected to the default sense points of the modules (close to load at K5/K7 and K6/K8).

(Alternative sense points close to module K12 can be used by populating R5/R6 instead of R7/R8. Output voltage should then be measured at TP12/TP13. Refer to schematic for more details).

Test points are provided for most signals according to printing on the test board.

7 Additional output capacitance

If additional output capacitance is desired, the possibility exists to mount extra electrolytic and/or ceramic capacitors. See fig 7.

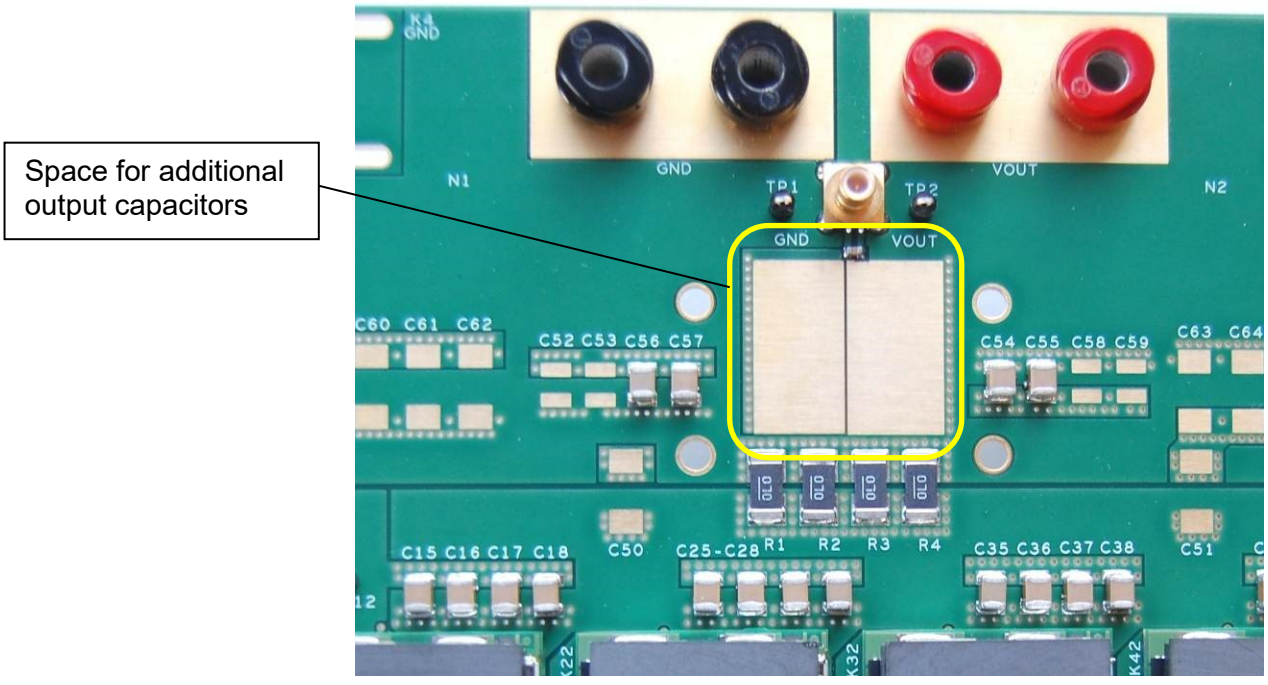


Fig 7 Space for additional output capacitors.

8 Electronic loads

In order to perform load transient tests on the modules two Puls loads can be connected to the output of the board. See fig 8.

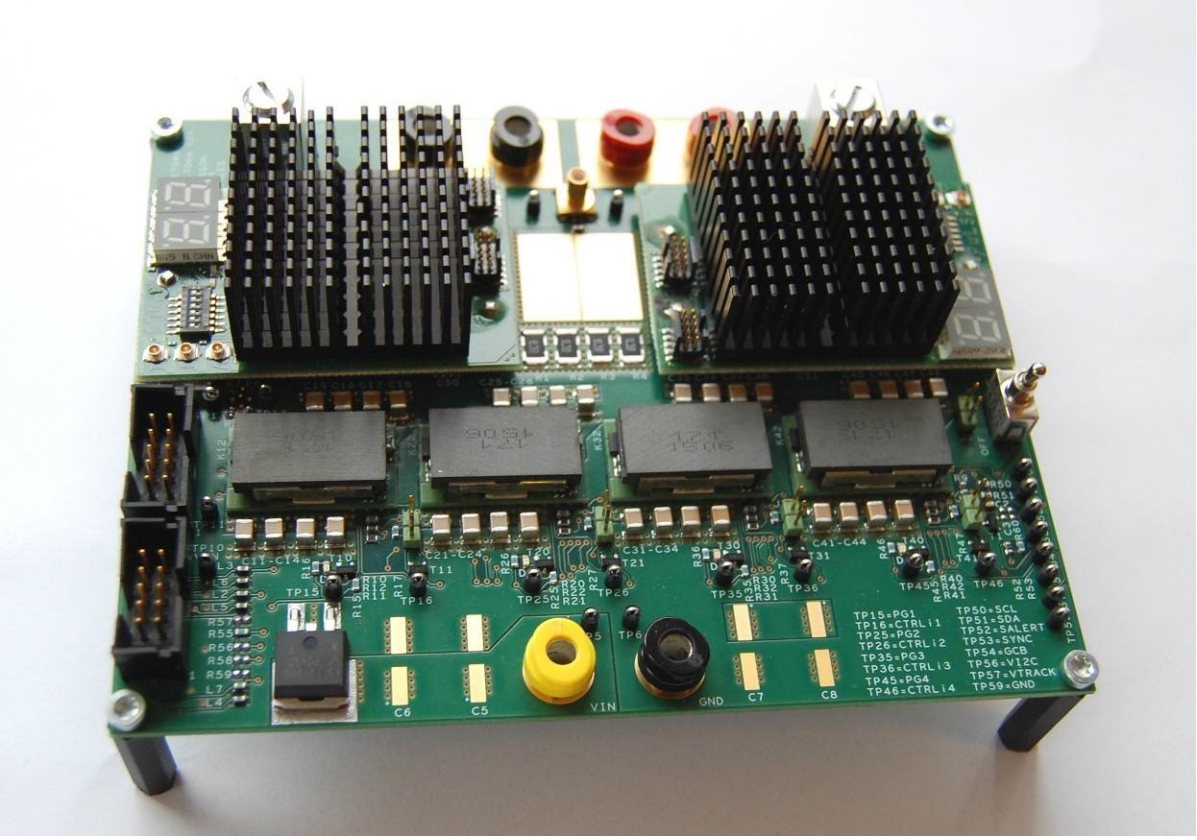


Fig 8 Puls loads connected to the board.

The Puls loads (ROA 128 5552/1) can be programmed for different transient loads and waveforms, see the technical specification for further information. They does not need to be soldered, the board is prepared for the use of sockets so the loads easily can be mounted.

9 Layout Description

9.1 Layout description

The following sections describe how the layout guidelines provided in the BMR 466 Technical Specification have been applied to the Reference Board layout. The purpose is to give the reader a better understanding of the guidelines by examples. Please note that every system is different and that there may well be considerations to make which are not provided here, depending on the system requirements and limitations set in the end application.

9.2 PCB stackup summary

Top layer	VOUT plane, component footprints, signal traces	35 um / 1 oz
Layer 2	GND plane	35 um / 1 oz
Layer 3	VOUT plane + VIN plane	35 um / 1 oz
Layer 4	GND plane	35 um / 1 oz
Layer 5	GND plane	35 um / 1 oz
Layer 6	VOUT plane + VIN plane	35 um / 1 oz
Layer 7	GND plane	35 um / 1 oz
Bottom layer	Signal traces (senses, digital signals etc), GND fill	35 um / 1 oz

9.3 Power pins

Refer to Figure 9.1. The power pins (VIN, VOUT, GND) should connect with low impedance to internal power planes in order to:

- Provide effective heat spread from module to the application board.
- Provide low electrical impedance to input and output capacitors, minimizing the input and output ripple levels.
- Provide a low resistance path for input and output current of the module, lowering the resistive losses.

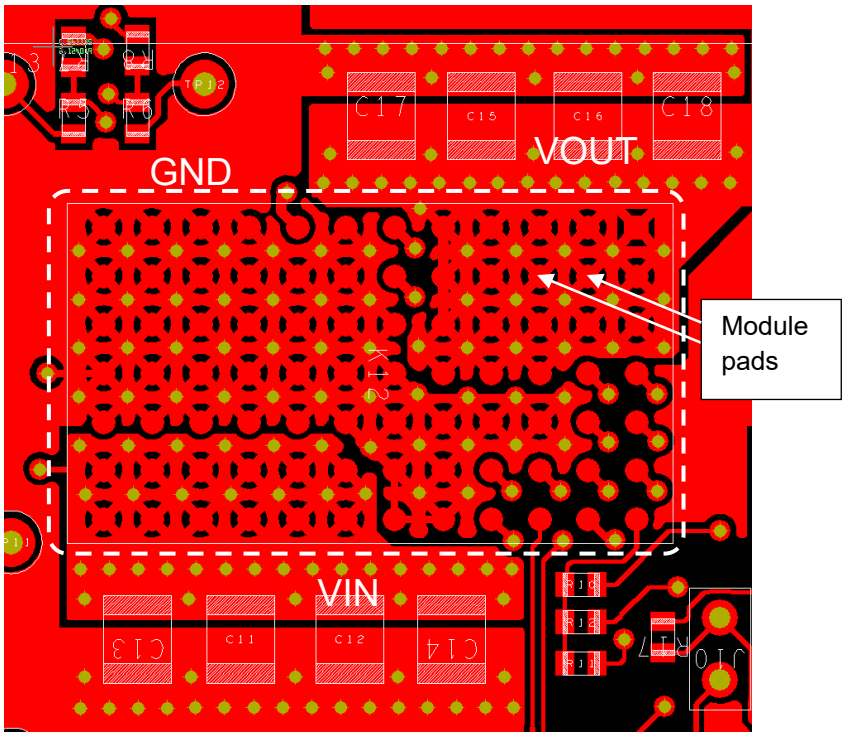


Fig 9.1. Top layer. Connection of power pins. BMR466 module in dashed area.

In this layout this is achieved by multiple vias in between and around the power pads and by wide connections between pads and vias. Too wide connections (or solder-mask defined pads) are not recommended however since this increase the risk of voids in the solder joints, potentially giving higher impedance instead of lower. If allowed, an even better alternative than vias in between the pads is to place vias directly in the module pads. In such case it is recommended that the vias are filled and overplated, in order to minimize the risk of voids in the solder joints.

See application note AN317 for further considerations regarding LGA pads.

9.4 Input capacitance

Refer to Figure 9.2. The smaller ceramic input capacitors (used mainly to lower the input voltage ripple level) are placed close to the VIN/GND pins of the module in order to minimize the connection impedance. For the same reason the terminals of the capacitors are embedded in planes with multiple vias close to the terminals, utilizing also the inner layers to connect the capacitors to the pins of the modules. An even better connection can be achieved by placing the vias directly in the terminal pads of the capacitors.

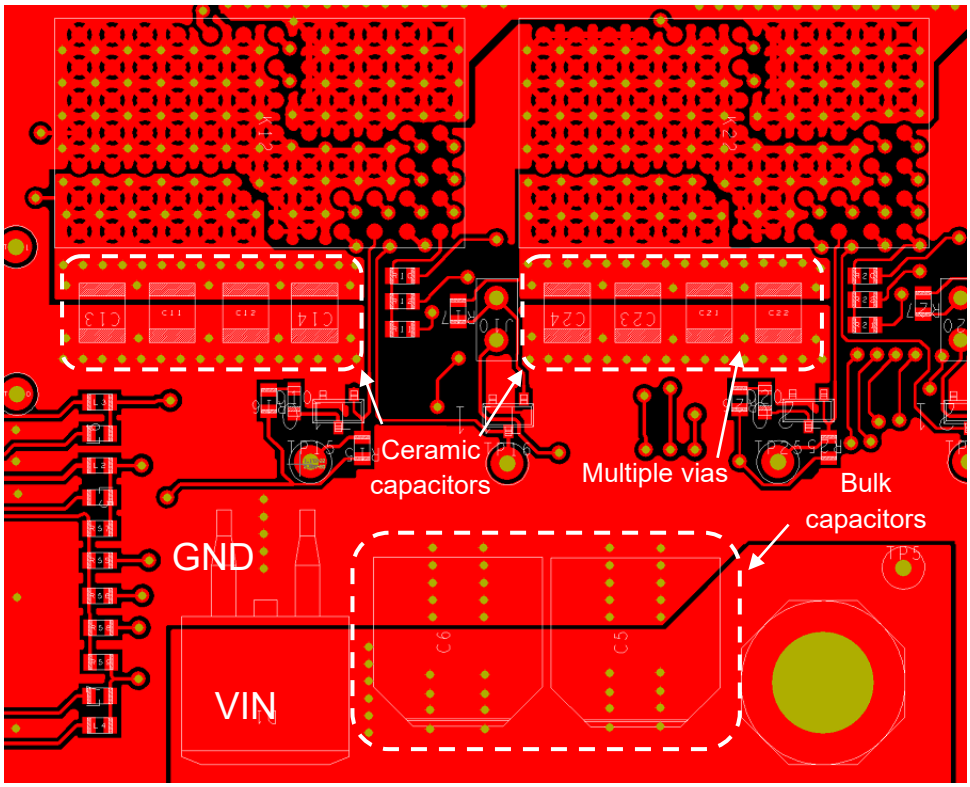


Fig 9.2 Top layer. Input capacitance in dashed areas.

Care should be taken when placing multiple vias regarding the fact that this could lead to large voids in the internal power planes, giving narrow passages for the large currents that may have to pass. This test board layout is not optimal when it comes to this detail as can be seen in Figure 9.3.

Placement and connections of the larger bulk input capacitor (used mainly to hold up the input voltage during large load transients or changes in input voltage) follows the rules of the ceramics described above. However in this case low impedance is not as critical due to the slower action, so the capacitor can be placed “behind” the ceramic input capacitors at a larger distance from the module.

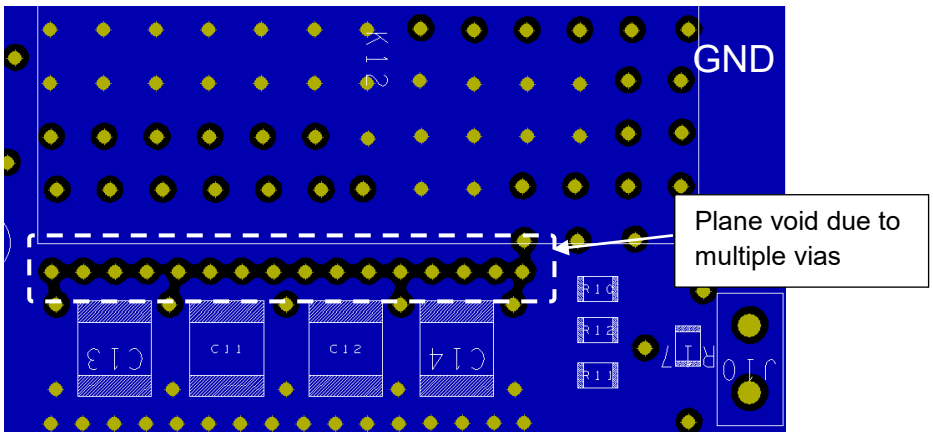


Figure 9.3 Layer 2. Gnd connections.

9.5 Output capacitance

Refer to Figure 9.4. Output capacitors are placed both close to module (to handle the module’s output ripple) and close to the load (to handle load transients), see application note AN321 for more details. In both cases it is important with low impedance connections (to module VOUT/GND pins or to the load’s VOUT/GND pins) and the guidelines described above for the input capacitors are applied.

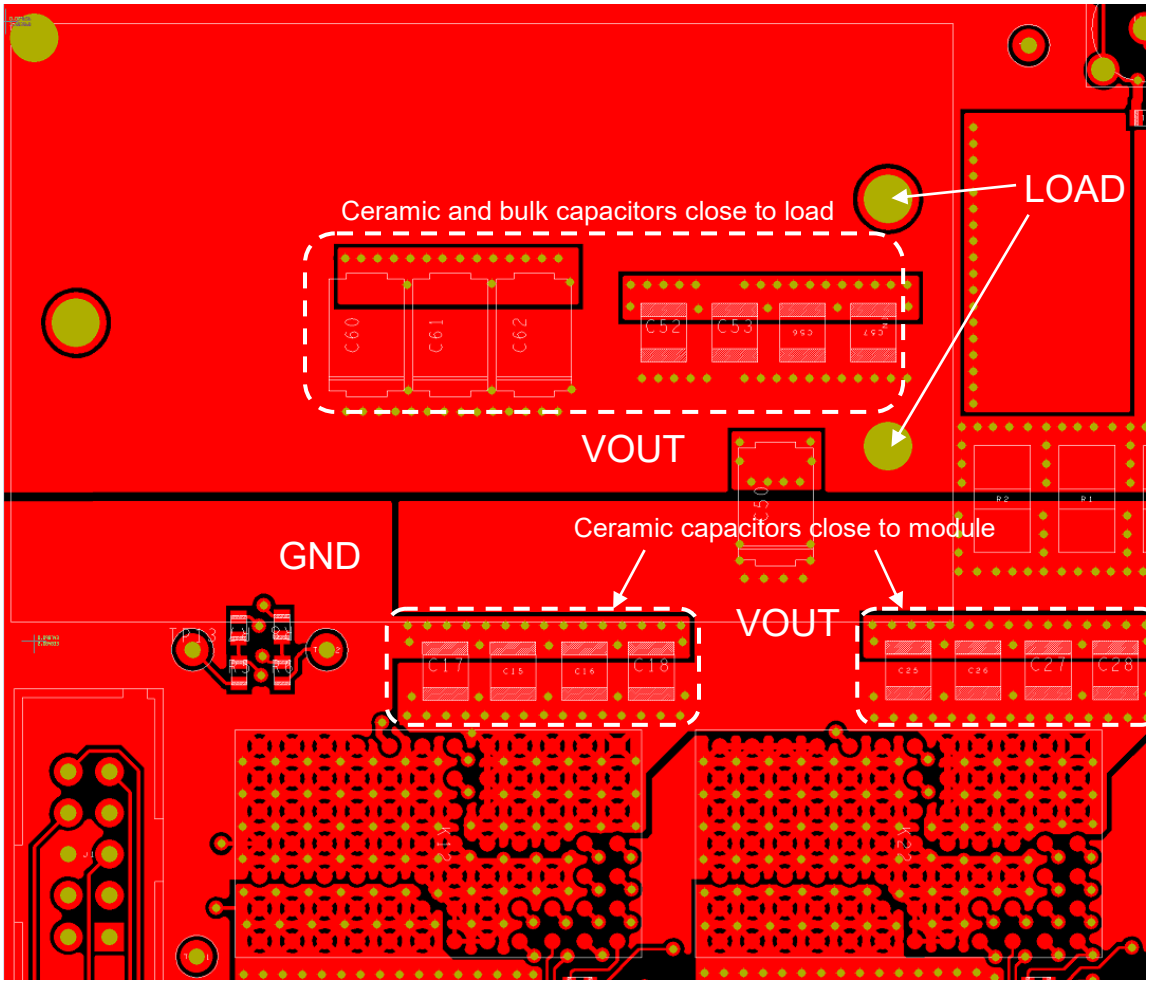


Fig 9.4 Top layer. Output capacitance in dashed areas.

Further it is important to use planes to distribute the output current to the load in order to minimize losses and the effective output impedance, providing good conditions for the module's control loop to compensate for load transient.

9.6 Sense traces

Refer to Figure 9.5 showing the sense traces routed on the bottom layer. The traces connect at VOUT/GND points close to the load in order to provide accurate regulation. Since regulation is sensitive to disturbances on the +S/-S inputs the wires are routed as a coupled pair all the way from load to the +S/-S pins. To further provide good signal integrity a solid ground follows the traces on an adjacent layer (layer 7 in this case). In this layout the sense signals are wired through resistors (R7/R8), in order to provide alternative sense points at the module pads instead of at the load. This is only for testing purposes however and is normally not recommended in an end application.

All modules on the test board sense at the same points, which must be the case when the modules are operated in current sharing mode.

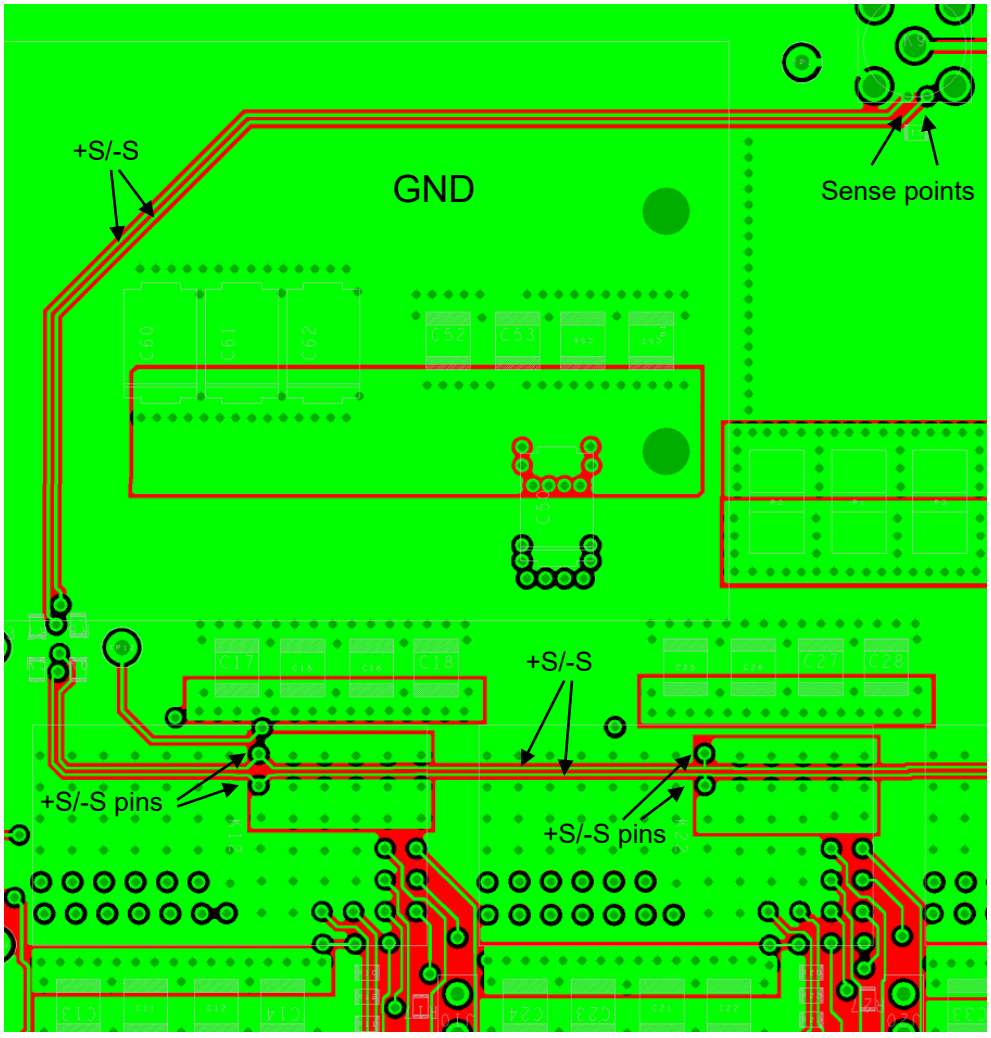


Fig 9.5 Bottom layer. Wiring of sense signals.

9.7 Pin-strap resistors

Refer to Figure 9.6 showing the wiring of the pin-strap resistors circuitry. To minimize capacitive load and provide good signal integrity, the resistors are placed with short traces close to the module and with a solid ground plane on an adjacent layer (layer 2 and 7 in this case).

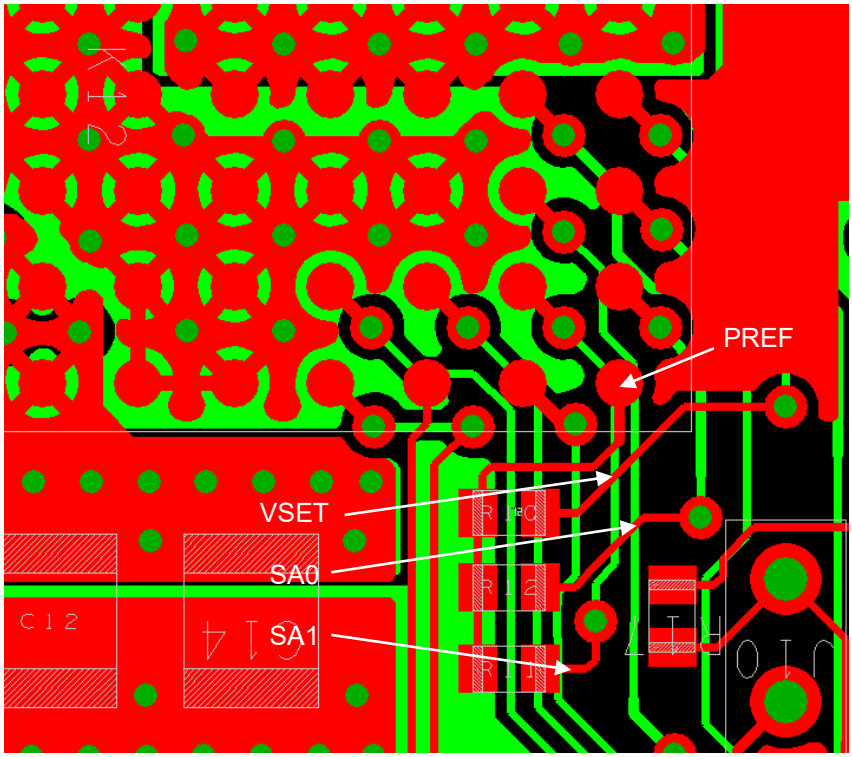


Fig 9.6 Top layer (red) and Bottom Layer (green). Pin-strap signals.